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# Core1588 v2.0 Release Notes

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Core1588 provides hardware support for the implementation of an IEEE 1588 Precision Time Protocol (PTP) capable system. The core maintains a Real Time Counter (RTC) and can detect and timestamp IEEE 1588 type frames in Reduced Media Independent Interface (RMII) MAC-PHY traffic. An APB interface allows a processor to control and monitor the core. The core can generate an interrupt and also supports trigger outputs and latch inputs.

## Features

- Real Time Clock (RTC) (32 bit seconds counter and 32 bit nanoseconds counter)
- Supports up to 3 latch inputs and up to 3 trigger outputs
- APB interface for processor access
- RTC value can be written directly
- RTC can be speeded up or slowed down
- Monitors RMII interface to detect IEEE 1588 frames
- Supports full duplex operation
- Can generate interrupt when IEEE 1588 frame detected or when latch/trigger event occurs
- Supports 100 Mbps operation only

## Interfaces

Core1588 has an APB (version 3) slave interface that typically will be connected to CoreAPB3. A system processor can use this interface to control and monitor the core.

Core1588 also takes in the signals present in an RMII connection between a MAC and a PHY. The core does not provide a functional RMII interface since all of the signals are inputs to the core. Core1588 simply monitors the RMII traffic.

## Delivery Types

Core1588 is licensed as Obfuscated or RTL.

### Obfuscated

Complete RTL code is provided for the core but the code describing the internal hardware features is obfuscated.

### RTL

Complete RTL source code is provided for the core.

## Supported Families

- SmartFusion™

## Supported Tool Flows

This version should be used with Libero IDE v9.1 SP2 or later.

## Installation Instructions

Core1588 is available through the Libero IDE IP Catalog. It can be downloaded from a remote web-based repository and installed into the user's local vault, ready for use. Once installed in Libero IDE, the core can be instantiated, configured, and generated within SmartDesign for inclusion in your Libero IDE project.

## Documentation

A copy of the Core1588 Handbook which describes the core functionality is included in this release. The handbook can be viewed by right-clicking on the core in the Catalog and selecting Open documentation > Core1588\_HB.pdf.

## Supported Test Environments

Verilog and VHDL testbenches are packaged with the core.

## Release History

**Table 1** Release History

<b>Version</b>	<b>Date</b>	<b>Description</b>
2.0	June 2011	First production release of Core1588





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