RN0053

CoreRSDEC v3.6 Release Notes

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

51300053-5/12.16

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 5.0

Updated changes related to CoreRSDEC v3.6.

1.2 Revision 4.0

Updated changes related to CoreRSDEC v3.5.

1.3 Revision 3.0

Updated changes related to CoreRSDEC v3.4.

1.4 Revision 2.0

Updated changes related to CoreRSDEC v3.1.

1.5 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreRSDEC v3.0.

Contents

2 Preface

2.1 Purpose

These release notes accompany the production release of CoreRSDEC v3.6. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Intended Audience

FPGA designers using Libero® System-on-Chip (SoC).

3 CoreRSDEC v3.6 Release Notes

3.1 Overview

These release notes accompany the production release of CoreRSDEC v3.6. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

3.2 Features

- Generation of the Reed-Solomon (RS) parameterizable decoder
- Code symbol width from 3 to 8 bits
- Codeword length up to 255 symbols
- User-defined finite field primitive polynomial
- Error correction capacity up to 16 symbols
- Shortened code support in conventional decoder mode
- Erasure support in conventional and CCSDS mode
- Conventional, CCSDS-8, and CCSDS-16

3.3 Interfaces

There is no standard advanced microcontroller bus architecture (AMBA®) interface available.

3.4 Delivery Types

CoreRSDEC requires a register transfer level (RTL) license to be used and instantiated. Complete source code is provided for the core.

3.5 Supported Families

- SmartFusion®2
- SmartFusion®
- Axcelerator®
- RTAX™-S
- ProASICPLUS®
- ProASIC®3
- ProASIC3E
- ProASIC3L
- Fusion®
- IGLOO®
- IGLOOe
- IGLOOPLUS
- IGLOO®2
- RTG4™
- PolarFire

3.6 Supported Tool Flows

- CoreRSDEC v3.6 requires Libero® System-on-Chip (SoC) software v9.2 or later.
- Supports Windows and Linux operating systems

Note: CoreRSDEC v3.6 is compatible with both Libero® integrated design environment (IDE) and Libero System-on-Chip (SoC). Unless specified.

3.7 Installation Instructions

The CoreRSDEC CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the Add Core catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

3.8 Documentation

This release contains a copy of the *CoreRSDEC Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

3.9 Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

3.10 Resolved History

Table 1 lists the release history for CoreRSDEC.

Table 1 • **Release History**

Version	Date	Changes
3.6	December 2016	As listed in Table 2.
3.5	September 2015	As listed in Table 3.
3.4	March 2015	Added support for RTG4 device. As listed in Table 4.
3.1	June 2013	As listed in Table 5.
3.0	March 2013	As listed in Table 6.

3.11 Resolved Issues in the v3.6 Release

Table 2 • **Resolved Issues in the v3.6 Release**

SAR Number	Changes
82564	RSDEC handbook correction and improvement for Table 2.
78094	Simulation waveforms for error flag were not proper
75898	Derive Constraints fail if CORERSDEC is used in the design for VHDL Flow

3.12 Resolved Issues in the v3.5 Release

Table 3 • **Resolved Issues in the v3.5 Release**

SAR Number	Changes
70990	Last code word missing in RSDEC.
70719	CoreRSDEC: CCSDS-8 first root must be 120.

3.13 Resolved Issues in the v3.4 Release

Table 4 • **Resolved Issues in the v3.4 Release**

SAR Number	Changes
62815	RAM generation simplified to use single clock.
57403	Added support for RTG4.

3.14 Resolved Issues in the v3.1 Release

Table 5 • **Resolved Issues in the v3.1 Release**

SAR Number	Changes

48438	In CCSDS mode, provided the optional conventional data on RSDecoder output interface using CCSDS_CONV parameter.
	if(CCSDS_CONV == 1)
	RSDecoder output is conventional data.
	else
	RSDecoder output is dual basis data.

48437	FLAGFAIL and ERRCOUNT detected issue fixed.
48209	In CCSDS-8/CCSDS-16, The core can detecting and correct the combination of errors and erasures. In case of CCSDS-8 maximum of 5 (6 > 2r + e) mixture of error and erasure can bea correctable. In case of CCSDS-16 maximum of 11 (12 > 2r + e) mixture of error and erasure can be correctable. In case of CCSDS-8 or CCSDS-16 and Erasure enable but no erasures found can correct tt number errors.

3.15 Resolved Issues in the v3.0 Release

Table 6 • **Resolved Issues in the v3.0 Release**

SAR Number	Changes
32668	Problem with CoreRSDEC when the start delay is power of 2. CoreRSDEC is fixed now and the arbitrary delay should be less than (NN-1). RFS_to_START_delay < (NN-1)
43831	Wrong data byte is outputted at the decoder output Fixed the RDY and CODRDY signals to be asserted when there is a valid data and the user has to follow SAR_32668 fix constraint. RFS_to_START_delay < (NN-1)
11936 11960 12215 14526 29024	CPZ supported, no need for Coreconsole.
12624 35638	Libero generates the memory on the run, memory issue fixed.
12753 43632	When CLKEN is toggled, two symbols are lost at outputs DATOUT and CODOUT. When CLKEN is inactive (LOW), the core is frozen. All inputs except NGRST are ignored, and the core retains its current state. Whenever the CLKEN is low we consider it as invalid received data on RECDIN (input DATA). Whenever the CLKEN is low the Decoder is frozen, DATOUT and CODOUT will contain invalid data and continues with valid sequence when the CLKEN is high.
14526	CoreRSDEC fixed and verified for t number of errors corrected.
43670	CoreRSDEC is a Libero smartdesign Component.
17224	CoreRSDEC is CCSD-8 and CCSDS-16 compatible.

3.16 Discontinued Features and Devices

There are no discontinued features or devices.

3.17 Known Limitations and Workarounds

There are no known limitations and workarounds.