RN0082

CoreJESD204BTX v3.1 Release Notes

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996
E-mail: sales.support@microsemi.com
www.microsemi.com

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

51300082-6/4.19

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 6.0

Updated changes related to CoreJESD204BTX v3.1.

1.2 Revision 5.0

Updated changes related to CoreJESD204BTX v3.0. SAR (83378): Add support for 8 lanes.

1.3 Revision 4.0

Updated changes related to CoreJESD204BTX v3.0.

1.4 Revision 3.0

Updated changes related to CoreJESD204BTX v2.3.

1.5 Revision 2.0

Updated changes related to CoreJESD204BTX v2.2.

1.6 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreJESD204BTX v2.0.

Contents

1 Revision History . . . 3
1.1 Revision 6.0 . . . 3
1.2 Revision 5.0 . . . 3
1.3 Revision 4.0 . . . 3
1.4 Revision 3.0 . . . 3
1.5 Revision 2.0 . . . 3
1.6 Revision 1.0 . . . 3
2 Preface . . . 5
2.1 Purpose . . . 5
2.2 Intended Audience . . . 5
3 CoreJESD204BTX v3.1 Release Notes . . . 6
3.1 Overview . . . 6
3.2 Features . . . 6
3.3 Delivery Types . . . 6
3.4 Supported Families . . . 6
3.5 Supported Tool Flows . . . 6
3.6 Installation Instructions . . . 6
3.7 Documentation . . . 7
3.8 Supported Test Environments . . . 7
3.9 Resolved History . . . 7
3.10 Resolved Issues in the v3.1 Release . . . 7
3.11 Resolved Issues in the v3.0 Release . . . 7
3.12 Resolved Issues in the v2.3 Release . . . 7
3.13 Resolved Issues in the v2.2 Release . . . 8
3.14 Resolved Issues in the v2.0 Release . . . 8
3.15 Discontinued Features and Devices . . . 8
3.16 Known Limitations and Workarounds . . . 8

2 Preface

2.1 Purpose

These release notes accompany the production release of CoreJESD204BTX v3.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Intended Audience

FPGA designers using Libero® System-on-Chip (SoC).

3 CoreJESD204BTX v3.1 Release Notes

3.1 Overview

These release notes accompany the production release of CoreJESD204BTX v3.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

3.2 Features

CoreJESD204BTX implements the transmitter interface of the JESD204B standard and has the following features:

- Supports 1 to 8 lanes
- Performs user-enabled scrambling
- Generates an initial lane alignment sequence
- Performs alignment character generation
- Sources link configuration data with user selected parameter values during initial lane synchronization sequence
- Performs the alignment character generation
- Performs user-enabled 8B/10B encoding
- Supports Subclasses 0, 1, and 2
- Internal clock generation
- Sync~ signal decoding
- Supports data width of 16, 32, or 64 bits

Note: Octet to Frame Stream conversion is not performed by the core.

3.3 Delivery Types

This core will support generation of un-obfuscated Verilog and VHDL versions of the core. The unobfuscated Verilog and VHDL versions will be license locked at the time of packaging. The core will be included in the Libero SoC IP bundle with Gold and Platinum licenses in clear RTL form. Refer to the IP DirectCore web page for more details.

3.4 Supported Families

- PolarFire®
- RTG4™
- SmartFusion®2
- IGLOO®2

3.5 Supported Tool Flows

- CoreJESD204BTX v3.1 requires Libero® System-on-Chip (SoC) software v11.0 or later.

3.6 Installation Instructions

The CoreJESD204BTX CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the Add Core catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

3.7 Documentation

This release contains a copy of the *CoreJESD204BTX Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

3.8 Supported Test Environments

The following test environments are supported:

- Verilog user testbench

3.9 Resolved History

Table 1 lists the release history for CoreJESD204BTX.

Table 1 • **Release History**

Version	Date	Changes
3.1	December 2017	Added RTL Enhancements.
3.0	November 2016	Added PolarFire support. Also added support of up to 8 lanes.
2.3	November 2014	Added RTG4 support.
2.2	December 2013	SAR fixes.
2.0	March 2013	Initial version of the core.

3.10 Resolved Issues in the v3.1 Release

Table 2 • **Resolved Issues in the v3.1 Release**

SAR Number	Changes
93938	RTL Enhancements Required.
94618	Updated the Table 8 CoreJESD204BTX I/O Signal Descriptions for the column: RESET_N.

3.11 Resolved Issues in the v3.0 Release

Table 3 • **Resolved Issues in the v3.0 Release**

SAR Number	Changes
83378	Add support for 8 lanes
65266	[CoreJESDTX]:CLogB2 input variable size is not sufficient

3.12 Resolved Issues in the v2.3 Release

No additional SARs were resolved in the v2.3 release.

3.13 Resolved Issues in the v2.2 Release

Table 4 • **Resolved Issues in the v2.2 Release**

SAR Number	Changes
50814	8B10B encoding incorrect!!
51085	Output data in reverse order
51848	Enhancement Request: Add 10bit EPCS mode

3.14 Resolved Issues in the v2.0 Release

As this is the initial version, there were no SARs resolved in the v2.0 release.

3.15 Discontinued Features and Devices

There are no discontinued features or devices.

3.16 Known Limitations and Workarounds

There are no known limitations and workarounds.