RN0086
Release Notes
CoreJESD204BRX v3.3

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Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 9.0

Updated changes related to CoreJESD204BRX v3.3.

1.2 Revision 8.0

Updated changes related to CoreJESD204BRX v3.2.

1.3 Revision 7.0

Updated changes related to CoreJESD204BRX v3.1.

1.4 Revision 6.0

Updated changes related to CoreJESD204BRX v3.0.

1.5 Revision 5.0

Updated changes related to CoreJESD204BRX v2.5.

1.6 Revision 4.0

Updated changes related to CoreJESD204BRX v2.4.

1.7 Revision 3.0

Updated changes related to CoreJESD204BRX v2.3.

1.8 Revision 2.0

Updated changes related to CoreJESD204BRX v2.2.

1.9 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreJESD204BRX v2.0.

2 CoreJESD204BRX v3.3 Release Notes

2.1 Overview

These release notes accompany the production release of CoreJESD204BRX v3.3. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CoreJESD204BRX implements the receiver interface of the JESD204B standard and has the following features:

- Supports 1 to 8 lanes
- Supports Subclasses 0, 1, and 2
- Performs word alignment
- Sync~ signal encoding
- Performs user-enabled 8B/10B decoding
- Recovers link configuration parameters
- Performs lane alignment buffering, monitoring and correction
- Performs user-enabled frame alignment, monitoring, and correction
- Performs octet reconstruction
- Performs user-enabled descrambling
- Error detection
- Supports data width of 16, 32, or 64 bits

Note: Octet to Frame Stream conversion is not performed by the core.

2.3 Delivery Types

This core will support generation of un-obfuscated Verilog and VHDL versions of the core. The unobfuscated Verilog and VHDL versions will be license locked at the time of packaging. The core will be included in the Libero SoC IP bundle with Gold and Platinum licenses in clear RTL form. Please refer the **IP DirectCore** webpage for more details.

2.4 Supported Families

- PolarFire®
- RTG4™
- SmartFusion®2
- IGLOO®2

2.5 Supported Tool Flows

- CoreJESD204BRX v3.3 requires Libero® System-on-Chip (SoC) software v11.0 or later.

2.6 Installation Instructions

The CoreJESD204BRX CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the Add Core catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *CoreJESD204BRX Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.8 Supported Test Environments

The following test environments are supported:

- Verilog user testbench

2.9 Resolved History

Table 1, page 3 lists the release history for CoreJESD204BRX.

Table 1 • **Release History**

Version	Date	Changes
3.3	March 2019	Fixed SARs and Updated Handbook.
3.2	September 2018	Fixed known SARs and added and updated RAMINDEX parameter for RAM instances.
3.1	January 2018	Added RTL Enhancements.
3.0	November 2016	Added PolarFire support. Also added support of up to 8 lanes.
2.5	January 2015	Added RTG4 support, LCD_EN parameter/generic and a EPCS_RX_VAL input signal per lane.
2.4	March 2014	Improved Maximum Operating Frequency.
2.3	December 2013	Fixed known SARs.
2.2	October 2013	Fixed known SARs and added support for the IGLOO2 product family. Also added support for 10-bit EPCS Interface.
2.0	March 2013	Initial version of the core.

2.10 Resolved Issues in the v3.3 Release

Table 2 • **Resolved Issues in the v3.3 Release**

SAR Number	Changes
104332	CoreJESD204BRX for RTG4 family is not SET mitigated.
104489	More description required for CF,HD parameters in the Handbook.

2.11 Resolved Issues in the v3.2 Release

Table 3 • **Resolved Issues in the v3.2 Release**

SAR Number	Changes
98389	Multi-lane design needs to monitor all lanes for successful SYNC assertion.
98390	RX_RESET_N should assert periodically until synchronization achieve.
95379	RAMINDEX: Incorrect row and column index values.

2.12 Resolved Issues in the v3.1 Release

Table 4 • **Resolved Issues in the v3.1 Release**

SAR Number	Changes
93939	RTL Enhancements Required.

2.13 Resolved Issues in the v3.0 Release

Table 5 • **Resolved Issues in the v3.0 Release**

SAR Number	Changes
83377	Add support for 8 lanes.
67151	RTG4: CoreJESD204BRX Timing issue-HB to updated for Clock Over constraining needed for STD speed grade devices.
67042	Modify elastic buffer to absorb variable latency.

2.14 Resolved Issues in the v2.5 Release

Table 6 • **Resolved Issues in the v2.5 Release**

SAR Number	Changes
63095	JESDRX SoftIP must include EPCS_RX_VALID i/p port for SERDES RX Data handling.
63732	Timing Closure fails due to Large number Logic Levels between registers.

2.15 Resolved Issues in the v2.4 Release

Table 7 • **Resolved Issues in the v2.4 Release**

SAR Number	Changes
54242	Enhance fmax to achieve 160 MHz (3.2 Gbps).

2.16 Resolved Issues in the v2.3 Release

Table 8 • **Resolved Issues in the v2.3 Release**

SAR Number	Changes
53593	Parameter ranges in HB does not match with configurator values.
53510	Wrong DEC_WA.v file in CPZ causing issues.

2.17 Resolved Issues in the v2.2 Release

Table 9 • **Resolved Issues in the v2.2 Release**

SAR Number	Changes
47391	Data is being shifted into the word aligner buffer in the wrong direction.
50813	8B10B decoding incorrect.
51084	Input data in reverse bit order.
51683	Add support for 10-bit EPCS Interface.

2.18 Resolved Issues in the v2.0 Release

As this was the initial version, there were no SARs resolved in the v2.0 release.

2.19 Discontinued Features and Devices

There are no discontinued features or devices.

2.20 Known Limitations and Workarounds

There are no known limitations and workarounds.