RN0110

CoreTSE v3.1 Release Notes

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Updated changes related to CoreTSE v3.1.

1.2 Revision 2.0

Updated changes related to CoreTSE v3.0.

1.3 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreTSE v2.0.

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2 CoreTSE v3.1 Release Notes

2.1 Overview

These release notes accompany the production release of CoreTSE v3.1. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

CoreTSE has the following features:

- 10/100/1000 Mbps Operation
- Full-duplex support at 10/100/1000 Mbps
- Half-duplex support at 10/100 Mbps
- Standard G/MII interface
- MDIO management interface for PHY register access
- Ten-bit interface(TBI)
- Wake on LAN (WoL) with Magic Packet Detection
- Frame Statistics Counters
- Destination Address Based Frame Filtering

2.3 Interfaces

Advanced peripheral bus (APB)-slave interface for MAC configuration registers and status counters access.

2.4 Delivery Types

CoreTSE requires an obfuscated register transfer level (RTL) license to be used and instantiated. Complete obfuscated RTL source code is provided for the core.

2.5 Supported Families

- PolarFire
- RTG4™
- IGLOO®2
- SmartFusion®2

2.6 Supported Tool Flows

- CoreTSE v3.1 requires Libero® System-on-Chip (SoC) software v11.7.3 and later releases.
- Microsemi® SoC Products Group Libero software v11.7.3 can be used with CoreTSE.

2.7 Installation Instructions

The CoreTSE CPZ file must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the **Add Core** catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the *Libero SoC Online Help* for further instructions on core installation, licensing, and general use.

2.8 Documentation

This release contains a copy of the *CoreTSE Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the *Libero SoC Online Help* for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores.

2.9 Supported Test Environments

- Verilog user testbench

2.10 Resolved History

Table 1 lists the release history for CoreTSE .

Table 1 • **Release History**

Version	Date	Changes
3.1	February 2017	Added RX_SLIP functionality for PolarFire Family.
3.0	March 2016	Updated for single 125 MHz TBI CLK and the new PolarFire family.
2.0	April 2015	Initial release supports windows and Linux.

2.10.1 Resolved Issues in the v3.1 Release

Table 2 • **Resolved Issues in the v3.1 Release**

SAR Number	Changes
79751	Typo in HB utilization table content.
83041	The default value of MAC-FIFO Configuration Register 5 in handbook is mismatched with actual default value.
77385	Add RX_SLIP output port and remove the barrel shift word aligner for PolarFire.

2.10.2 Resolved Issues in the v3.0 Release

Table 3 • **Resolved Issues in the v3.0 Release**

SAR Number	Changes
75227	Support for a single 125MHz TBI receive clock.
75236	To add support for PolarFire.
75072	CoreTSE GMII Mode , pins showing as unused after synthesis.
71541	Simulation error when using CoreTSE and CoreTSE_AHB in single design.

2.10.3 Resolved Issues in the v2.0 Release

There is no software action request (SAR) resolved as this the first release.

2.11 Discontinued Features and Devices

62.5MHz PMA clocks are replaced with single 125MHz PMA clock.

2.12 Known Limitations and Workarounds

There are no known limitations and workarounds for CoreTSE v3.1.