

RN0071

CoreFFT v7.0 Release Notes





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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 9.0

Updated changes related to CoreFFT v7.0.

1.2 Revision 8.0

Updated changes related to CoreFFT v6.4.

1.3 Revision 7.0

Updated changes related to CoreFFT v6.3.

1.4 Revision 6.0

Updated changes related to CoreFFT v6.2.

1.5 Revision 5.0

Updated changes related to CoreFFT v6.1.

1.6 Revision 4.0

Updated changes related to CoreFFT v5.0.

1.7 Revision 3.0

Updated changes related to CoreFFT v4.0.

1.8 Revision 2.0

Updated changes related to CoreFFT v3.0.

1.9 Revision 1.0

Revision 1.0 was the first publication of this document. Created for CoreFFT v2.0.

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2 CoreFFT v7.0 Release Notes

2.1 Overview

These release notes accompany the production release of CoreFFT v7.0. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds.

2.2 Features

- Highly configurable DirectCore register transfer level (RTL) generator
- Choice of Radix-2 In-place architecture or Radix-22 Streaming Fast Fourier Transform (FFT)
- Forward and inverse complex FFT
- Transform sizes: 32-, 64-, 128-, 256-, 512-, 1,024-, 2,048-, 4,096-, 8,192-, and 16384-point (in-place architecture), 16-, 32-, 64-, 128-, 256-, 512-, and 1,024-point (streaming architecture)
- 8- to 32-bits I/O real and imaginary data and twiddle coefficients
- Two's complementary I/O data
- Natural input and output sample order
- Selection of conditional or unconditional block floating point scaling (in-place architecture), pre-defined scaling schedule (streaming architecture)
- Embedded RAM-block based twiddle look-up table (LUT)
- Built-in memory buffers
- Handshake signals to facilitate easy interface to the user circuitry

2.3 Delivery Types

CoreFFT is freely distributed with Microsemi Libero SoC. Complete HDL source code is provided for the core and testbenches.

2.4 Supported Families

- PolarFire
- RTG4™
- SmartFusion®2
- IGLOO®2

2.5 Supported Tool Flows

- CoreFFT v7.0 requires Libero® System-on-Chip (SoC) software v11.7 or later.
- Supports Windows® and Linux operating systems

2.6 Installation Instructions

The CoreFFT CPZ must be installed into Libero software. This is done automatically through the Catalog update function in Libero, or the CPZ file can be manually added using the Add Core catalog feature. Once the CPZ file is installed in Libero, the core can be configured, generated, and instantiated within SmartDesign for inclusion in the Libero project.

Refer to the [Libero SoC Online Help](#) for further instructions on core installation, licensing, and general use.

2.7 Documentation

This release contains a copy of the *CoreFFT Handbook*. The handbook, describes the core functionality and gives step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and also implementation suggestions. Refer to the [Liberio SoC Online Help](#) for instructions on obtaining IP documentation.

For updates and additional information about the software, devices, and hardware, visit the Intellectual Property pages on the Microsemi SoC Products Group website: visit:

<http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores>.

2.8 Supported Test Environments

The following test environments are supported:

- VHDL user testbench
- Verilog user testbench

2.9 Resolved History

Table 1 lists the release history for CoreFFT.

Table 1 • Release History

Version	Date	Changes
7.0	November 2016	Support for PolarFire family and In-place FFT size of 16384 is added. The Unscaled Streaming architecture option is added.
6.4	February 2015	Support for RTG4 family is added.
6.3	September 2013	Support for Linux and new devices is added.
6.2	June 2013	Support for IGLOO2 family is added.
6.1	March 2013	Support for SmartFusion2 family is added.
5.0	May 2011	Streaming FFT architecture is added. The v5.0 release supports RTAX-DSP family only.
4.0	May 2010	As listed in the Table 8. The v4.0 release supports RTAX-DSP family only.
3.0	May 2007	Configurable 8- to 16-bit data precision.
2.0	September 2005	Initial release.

2.10 Resolved Issues in the v7.0 Release

Table 2 • Resolved Issues in the v7.0 Release

SAR Number	Changes
64614	Remove unnecessary ordering info from handbook.
75800	Add support for PolarFire devices.
75982	Clarify Streaming FFT bit resolution.
76070	Add streaming FFT support for Full precision (Unscaled mode) and Controlled Scale Schedule modes.
77985	Add support for 16K-pt FFT on In-Place implementation.

2.11 Resolved Issues in the v6.4 Release

Table 3 • Resolved Issues in the v6.4 Release

SAR Number	Changes
43888	Provide support for all devices of supported families.
47549	Indicate device type used for utilization and performance data of the handbook.
59864	Fix VHDL code causing synthesis failure.
62324	Add RTG4 support.

2.12 Resolved Issues in the v6.3 Release

Table 4 • Resolved Issues in the v6.3 Release

SAR Number	Changes
50390	Eliminate REN signal toggling on RTAX-DSP devices.
50391	Improve Streaming FFT performance.

2.13 Resolved Issues in the v6.2 Release

Table 5 • Resolved Issues in the v6.2 Release

SAR Number	Changes
48056	Support for IGLOO2 family.

2.14 Resolved Issues in the v6.1 Release

Table 6 • Resolved Issues in the v6.1 Release

SAR Number	Changes
38287	Support for SmartFusion2 family.
29129	Support for multiple FFT instances.

2.15 Resolved Issues in the v5.0 Release

Table 7 • Resolved Issues in the v5.0 Release

SAR Number	Changes
32053	Add streaming architecture.

2.16 Resolved Issues in the v4.0 Release

Table 8 • Resolved Issues in the v4.0 Release

SAR Number	Changes
11570	Eliminate module names reserved by Libero IDE for other purposes.
11732	Resolve the core installation issues.
13857	Indicate in documentation the core output latency.

2.17 Resolved Issues in the v3.0 Release

There were no SARs resolved in the v3.0 release.

2.18 Resolved Issues in the v2.0 Release

As this is the initial version, there were no SARs resolved in the v2.0 release.

2.19 Discontinued Features and Devices

CoreFFT v7.0 does not support RTAX-DSP (RTAX2000D, RTAX4000D) devices. These devices are supported in CoreFFT v6.3 or earlier versions.

2.20 Known Limitations and Workarounds

There are no known limitations and workarounds.

3 Product Support

Microsemi SoC Products Group backs its products with various support services, including Customer Service, Customer Technical Support Center, a website, electronic mail, and worldwide sales offices. This appendix contains information about contacting Microsemi SoC Products Group and using these support services.

3.1 Customer Service

Contact Customer Service for non-technical product support, such as product pricing, product upgrades, update information, order status, and authorization.

From North America, call **800.262.1060**

From the rest of the world, call **650.318.4460**

Fax, from anywhere in the world, **408.643.6913**

3.2 Customer Technical Support Center

Microsemi SoC Products Group staffs its Customer Technical Support Center with highly skilled engineers who can help answer your hardware, software, and design questions about Microsemi SoC Products. The Customer Technical Support Center spends a great deal of time creating application notes, answers to common design cycle questions, documentation of known issues, and various FAQs. So, before you contact us, please visit our online resources. It is very likely we have already answered your questions.

3.3 Technical Support

For Microsemi SoC Products Support, visit

<http://www.microsemi.com/products/fpga-soc/design-support/fpga-soc-support>.

3.4 Website

You can browse a variety of technical and non-technical information on the Microsemi SoC Products Group home page, at <http://www.microsemi.com/products/fpga-soc/fpga-and-soc>.

3.5 Contacting the Customer Technical Support Center

Highly skilled engineers staff the Technical Support Center. The Technical Support Center can be contacted by email or through the Microsemi SoC Products Group website.

3.5.1 Email

You can communicate your technical questions to our email address and receive answers back by email, fax, or phone. Also, if you have design problems, you can email your design files to receive assistance. We constantly monitor the email account throughout the day. When sending your request to us, please be sure to include your full name, company name, and your contact information for efficient processing of your request.

The technical support email address is soc_tech@microsemi.com.

3.5.2 My Cases

Microsemi SoC Products Group customers may submit and track technical cases online by going to [My Cases](#).

3.5.3 Outside the U.S.

Customers needing assistance outside the US time zones can either contact technical support via email (soc_tech@microsemi.com) or contact a local sales office. Visit [About Us](#) for [sales office listings](#) and [corporate contacts](#).

3.6 ITAR Technical Support

For technical support on RH and RT FPGAs that are regulated by International Traffic in Arms Regulations (ITAR), contact us via soc_tech@microsemi.com. Alternatively, within My Cases, select **Yes** in the ITAR drop-down list. For a complete list of ITAR-regulated Microsemi FPGAs, visit the ITAR web page.