Core1553BRT_APB v4.3 Release Notes

This document accompanies the production release of the Core1553BRT_APB IP core. It describes the features and enhancements, system requirements, supported families, implementations, known issues, and workarounds.

Key Features

- APB3 compliant host interface
- MIL-STD-1553B compliant remote terminal
- Supports 12, 16, 20, and 24 MHz operation
- Fail-safe state machines
- Base core 1553BRT function
- Support for mode code 2
- Support for mode code 19

Core Versions

The built-in test register (BIT) indicates the version of the core. The core will transmit this in response to the Transmit BIT mode code. Table 1 shows how the versions are encoded.

Table 1 • **Encoding of Version Number**

Version	BitWord[4:0]
v4.3	14(5'b01110)

Interfaces

The Core1553BRT_APB core supports an APB3 compliant host interface.

Delivery Types

The Core1553BRT_APB core is licensed in three ways:

- Evaluation
- Obfuscated
- RTL

Evaluation

Precompiled simulation libraries are provided, allowing the core to be instantiated and simulated within the Libero® Integrated Design Environment (IDE) or System-on-Chip (SoC). The design may not be synthesized, as source code is not provided.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign.

Simulation, synthesis, and layout can be performed with Libero. The RTL code for the core is obfuscated and the some of the testbench source files are not provided. Instead, they are precompiled into the compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- PolarFire®
- RTG4™
- IGLOO®2
- SmartFusion®2
- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- SmartFusion®
- Fusion
- ProASIC PLUS®
- Axcelerator®
- RTAX-S

Supported Tool Flows

Use Libero IDE v9.2 or SoCv11.6 and use SoCv12.1 specially for RTG4, SmartFusion2, IGLOO2, and PolarFire with this Core1553BRT_APB release.

Installation Instructions

Within Libero, click the **Add Core** button in the Catalog to locate and install a local CPZ file, or use the automatic web update feature in Libero. Once the CPZ file is installed in Libero, the core can be instantiated, configured, and generated within SmartDesign for inclusion in the Libero project.

For more information about core installation, licensing, and general use, refer to the *Libero SoC Online Help*.

Documentation

For more information about Microsemi® Intellectual Property, visit *http://www.microsemi.com/products/fpga-soc/design-resources/ip-cores*. For updates and additional information about Microsemi software, FPGAs, and hardware, visit *http://www.microsemi.com*.

Supported Test Environments

Core1553BRT_APB supports the following test environments:

- VHDL user testbench
- Verilog user testbench

Precompiled Libraries

Core1553BRT_APB supports the following precompiled libraries:

- **IDE**
  - Precompiled libraries are built with ModelSim 10.2c for v4.3
- **SoC**
  - Precompiled libraries are built with ModelSim 10.7c for v4.3

Release History

Table 2 shows the release history of the core.

Table 2 • **Release History**

Version	Date
v4.3	May 2019
v4.1	December 2015
v3.3	September 2012
v3.2	June 2010

This document reflects the release and revision history for Core155BRT_APB. The associated release notes for Core1553BRT contain a full release and revision history for the base 1553B function of this core.

Resolved Issues in the v4.3 Release

Table 3 shows the resolved SARs in the Core1553BRT_APB v4.3 release.

Table 3 • **Resolved SARs in the Core1553BRT_APB v4.3 Release**

SAR	Description
103990	Adding support for SmartFusion2/IGLOO2
71040	RTG4 implementation to use ECC

Resolved Issues in the v4.1 Release

Table 4 shows the resolved SARs in the Core1553BRT_APB v4.1 release.

Table 4 • **Resolved SARs in the Core1553BRT_APB v4.1 Release**

SAR	Description
21778	CCZ verification: Obfuscated license not available for core
29254	BUSAOUTINH must be BUSAOUTIN
29255	Confusion about verification testbench support
32639	Update VHDL files for SmartFusion
69313	Syntax error in ram2k16_pa3l.vhd
69521	Reset required for back-end signals
69526	Different BFM versions packaged for VHDL (# Version 2.1, 10th Oct 08) and Verilog (Version 2.1, 22nd Dec 08)

Discontinued Features and Devices

There are no discontinued features or devices.

Known Issues and Workarounds

There are no known limitations and workarounds.

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