Core1553BRT v4.2 Release Notes

These release notes accompany the production release for Core1553BRT. This document provides details about the features, enhancements, system requirements, supported families, implementations, and known issues and workarounds associated with the respective releases.

Features

Core1553BRT has the following features.

- MIL-STD-1553B compliant remote terminal
- Supports 12, 16, 20, and 24 MHz operation
- Fail-safe state machines
- Tested according to RT Validation Test Plan MIL-HDBK-1553, Appendix A
- Modify mode code 2, adding configurable functionality
- Modify mode code 19, adding configurable functionality

Interfaces

Core1553BRT supports a simple synchronous backend interface.

Delivery Types

Core1553BRT is licensed in three ways: Evaluation, Obfuscated, and register transfer level (RTL).

Evaluation

Precompiled simulation libraries provided in Core1553BRT allow the core to be instantiated in SmartDesign and simulated within Libero® System-on-Chip (SoC) software. The design may not be synthesized, as source code is not provided.

Obfuscated

Complete RTL code is provided for the core, enabling the core to be instantiated with SmartDesign. Simulation, synthesis, and layout can be performed with the Libero SoC software. The RTL code for the core is obfuscated and some of the testbench source files are not provided. Instead, they are precompiled into the compiled simulation library.

RTL

Complete RTL source code is provided for the core and testbenches.

Supported Families

- RTG4™
- SmartFusion®2
- IGLOO®2
- SmartFusion®
- Fusion
- IGLOO®
- IGLOOe
- IGLOO PLUS
- ProASIC®3
- ProASIC3E
- ProASIC3L
- ProASIC PLUS®
- Axcelerator®
- RTAX™-S
- SX-A
- RTSX-S

Supported Tool Flows

Use Libero SoC v11.6 or Libero IDE v9.2 or later with this Core1553BRT release.

Precompiled Libraries

Core1553BRT supports the following precompiled libraries.

- IDE

  Precompiled libraries are built with ModelSim 10.2c for v4.2
- SoC

  Precompiled libraries are built with ModelSim 10.3c for v4.2

Installation Instructions

Core1553BRT is available through the Libero SoC IP Catalog. Within Libero SoC software, locate a local Core1553BRT cpz file and click **Add Core** to install it in the catalog, or install using the automatic web update feature. After the CPZ file is installed in the Libero SoC software, instantiate, configure, and generate the core within the SmartDesign to include it in the Libero SoC project.

For RTL and obfuscated versions of the core, install the FlexLM license and restart the SmartDesign before exporting the core. Consult the Libero SoC online help for instructions on core installation and licensing.

Documentation

This release contains a copy of the *Core1553BRT Handbook*, which describes the core functionality, step-by-step instructions on how to simulate, synthesize, and place-and-route this core, and provides implementation suggestions.

For updates and additional information about the software, devices, and hardware, see the Intellectual Property pages on the Microsemi website at www.microsemi.com/soc.

Supported Test Environments

The following test environments are supported.

- VHDL verification testbench
- VHDL user testbench
- Verilog user testbench

Discontinued Features and Devices

No features have been discontinued in the v4.2 Core1553BRT release.

New Features and Devices

No new features were added in Core1553BRT v4.2 release.

Core Versions

The built-in test (BIT) register indicates the version of the core. The core transmits this in response to the Transmit BIT mode code. The following table shows how the versions are encoded.

Table 1. Encoding of Version Number

Version	Bit[4:0]
v2.0	1
v2.1	2
v2.12	3
v2.2	4
v2.21	5
v3.0	8
v3.1	9
v3.2	10
v3.3	11
v3.4	12
v4.0	13
v4.1/v4.2	14

Release History

The following table provides the release history of the core.

Table 2. Release History

Version	Date
v4.2	March 2017
v4.1	December 2015
v4.0	January 2014
v3.4	May 2013
v3.3	August 2010
v3.2	February 2009
v3.1	March 2007
v3.0	August 2005
v2.2	January 2005
v2.13	September 2004
v2.12	September 2004
v2.11	May 2004
v2.1	February 2003
v2.0	August 2002

Resolved Issues in the v4.2 Release

The following table lists the SARs that were resolved in Core1553BRT v4.2.

Table 3. Resolved SARs in the Core1553BRT v4.2 Release

SAR No.	Description
83265	The BRT requests more than 32 data words from the back-end of the transmission shutdown.

Resolved Issues in the v4.1 Release

The following table lists the SARs that were resolved in Core1553BRT v4.1.

Table 4. Resolved SARs in the Core1553BRT v4.1 Release

SAR No.	Description
57407	Add RTG4 Support.

Resolved Issues in the v4.0 Release

The following table lists the SARs that were resolved in Core1553BRT v4.0.

Table 5. Resolved SARs in the Core1553BRT v4.0 Release

SAR No.	Description
49647	Document inputs which have and which have not got metastability synchronizers on them.
34109	Wrong timing diagram of Memory Read Timing - Synchronous Mode in 1553BRT -
42771	Core1553BRT IP core questions
45657	Wrong waveform in Figure 4-4
31613	Test case 7 of Core1553BRT - State Machine lock up always fails
48803	Core1553BRT doc bug.
17286	CCZ Verification: Obfuscated License option not available on Linux.
24477	Double resynchronization to avoid metastability issues
29798	Transmit Last command and RTBUSY behaviour
14645	RT does not handle CW-CW-DW error sequence on RTRT
45161	Customer wants to have hamming-2 state machine coding
48533	Core1553BRT Generic Range Issue (VHDL)
50875	PURSTN, BITIN, BITINEN ports & INITLASTSW, EXTERNAL_BIST parameters added
14285	Obfuscation of VHDL source files removes syn_preserves

Resolved Issues in the v3.4 Release

The following table lists the software action requests (SARs) that were resolved in Core1553BRT v3.4.

Table 6. Resolved SARs in the Core1553BRT v3.4 Release

SAR No.	Description
36209	Add option to have state machine with Hamming-2 protection
46840	VHDL: Add underflow/overflow protection to counters
46841	VHDL: Incomplete sensitivity list
46839	VHDL: Use when others instead of explicit unused states
46837	VHDL: syn_encoding typographical error in code

Resolved Issues in the v3.3 Release

The following table lists the SARs that were resolved in Core1553BRT v3.3.

Table 7. Resolved SARs in the Core1553BRT v3.3 Release

SAR	Description
14909	Single-clock-cycle pulse that indicates CMDVAL has changed
15029	RT address can be set to ‘11111’ for normal operation only when BCASTEN is set to 0.

Resolved Issues in the v3.2 Release

The following table lists the SARs that were resolved in Core1553BRT v3.2.

Table 8. Resolved SARs in the Core1553BRT v3.2 Release

SAR	Description
11374	Additional tests have been added to the verification environment with INTENBBR tied low.
11646	Bus controller in user testbench (VHDL) updated to prevent incorrect operation.
12093	Verification TB test selection has been updated to prevent failures when test plan tests enabled and option 9 used.
13678	VHDL testbench has been updated to use VHDL-93 syntax rather than VHDL-87 syntax on file IO commands
13628 13661	When WRTCMD = 1 and a broadcast mode code without data command is received, the command word was not written to memory. This has been fixed and the verification environments updated to cover this case.
13821	Latest qualification reports are now included with the core along with updated code coverage data.
14285	Obfuscated VHDL version of core was missing the Synplify® preserve attributes to preserve the FSM_ERROR logic. This has been fixed.
14645	When processing RT-RT messages, the RX RT will ignore any additional words that may be appended to the two command words while waiting for the status word from the transmitting RT. If a data word is corrupted to look like a legal command word, a corrupted RT receive message could be interpreted as the RT-RT message sequence. If a RT receive message sequence is detected on the bus within a normal RT-RT timeout period, depending on the command word value, this data may be interpreted as the status and data words associated to the RT-RT message and could be incorrectly written to the RT memory. The RTL code has been updated so that RT- RT messages detect any additional words while waiting for the status word and immediately set the message error bit.

Resolved Issues in the v3.1 Release

There are no functional changes from the previous v3.0 release. Minor changes have been made:

1. A hardwired constant, which was set to false in the command word legality module, is now a generic, defaulted to false on the top level of v3.1 core. This enables testing of the legality logic in the verification environment.
2. The version number encoding in the BIT word has been updated (Table 1 on page 4).
3. The new top-level wrapper converts some core inputs to parameters. The CoreConsole flow allows this use of parameterized configurable RTL code so the user does not need to tie these inputs to GND or VCC. This simplifies using the core in the user's design.
4. The old top-level RT1553B is still available once the core has been exported to Libero SoC.

Resolved Issues in the v3.0 Release

The following table lists the SARs that were resolved in the Core1553BRT v3.0 release.

Table 9. Resolved SARs in the Core1553BRT v3.0 Release

SAR No.	Description
46571	The verification testbench does not verify the transmit timer timeout at all frequencies if the all tests option is used. The verification testbench has been updated to call these tests when the all tests option is selected.
47719	If the RTBUSY input becomes active after the status word has been transmitted, when the RT is transmitting data, the core stops requesting data from the backend and completes the 1553B message on the bus using the last data read from the backend for the remaining data words. This leads to the transmission of incorrect data. The protocol state machine has been updated so that when RTBUSY is asserted during a transmit data message, the core simply aborts the message. The bus controller detects an incomplete message and retries the message. Receive messages function correctly. When RTBUSY is asserted, the core stops accessing memory and will set the BUSY bit. The status word sent at the end of the message indicates that the message was incorrectly received.
47720	All the state machines in the core have been updated to include illegal state detection logic and an FSM_ERROR output that will pulse active for a single cycle, should any state machine enter an illegal state.
47875/48194	The TEXTIO package used in the testbench does not format integers correctly when printed as bit values, and an internal loop generates a simulation fatal error if the coverage option is enabled in Model*Sim* v6.0. Both issues have been fixed.
48197	The verification testbench does not thoroughly test for a loopback failure. Additional tests have been added to check for loopback errors in each data word. Tests have also been added to verify that the core can handle up to 2.4 µs of delay in the loopback path.
48234	The core does not detect a loopback error in the last word of a message; the loopback failure is reported on the following message instead. The core has been updated to resolve this issue and the datasheet now specifies a maximum loopback delay.
48433	The core release structure and user's guide has been updated to simplify the installation into the Libero IDE environment.
48434	The transceiver and backend models used in the VHDL user testbench have been simplified.

Resolved Issues in the v2.2 Release

The following table lists the SARs that have been resolved in the Core 1553BRT v2.2 release.

Table 10. Resolved Issues in v2.2

SAR No.	Description
34405	The core may generate erroneous SYNCOUT pulses if a TX message to a different TX is transmitted on the bus, after the synchronize mode code. This is corrected in the v2.2 release.
34555	A new top-level output port, CMDSTB, was added. It pulses high for a single cycle when the CMDVAL output changes.
43045	Compiled simulation library name was changed to Core1553BRT for consistency with other IP cores.

Resolved Issues in the v2.13 Release

The following table lists the SARs that have been resolved in the Core 1553BRT v2.13 release.

Table 11. Resolved Issues in v2.13

SAR No.	Description
42196	The simulation libraries included in the v2.12 release are not compatible with Model*Sim* v5.8 and above. The simulation libraries have been recompiled with the latest version of Model*Sim*.

Resolved Issues in the v2.12 Release

The following table lists the SARs that have been resolved in the Core 1553BRT v2.12 release.

Table 12. Resolved Issues in v2.12

SAR No.	Description
38813	False 1533B loopback failures may be detected when the core is operated at 12 MHz. This may happen when extra delay is inserted between Core1553BRT and the transceiver, due to pipelining within the FPGA or external buffers. The core has been modified to increase the time period the core allows for data to be looped back from the transceiver. The loopback time allowance has been increased to 500 ns.

Resolved Issues in the v2.11 Release

The following table lists the SARs that have been resolved in the Core 1553BRT 2.11 release.

Table 13. Resolved Issues in v2.11

SAR No.	Description
37325	The Verilog source code used incorrect *always* statements. A complete new set of Verilog source files has been provided. The VHDL versions of the core are unaffected by this change.

Resolved Issues in the v2.1 Release

The following table lists the SARs that have been resolved in the Core1553BRT v2.1 release.

Table 14. Resolved Issues in v2.1

SAR No.	Description
24740	The datasheet describes an MSGSTART output. This was omitted from v2.0 of the core. The CMDSYNC output behaves as the MSGSTART signal, not as described in the datasheet. Neither of these outputs will function as described in the datasheet.
24741	CMDOKOUT output added. Indicates whether the legality checker has detected a legal command word. This is useful when core USEEXTOK is high; it allows the user to logic to know whether a received command word is legal.
25206	The Verilog backend model used in the user testbench did not declare enough memory for operation when CMODE = 1.
25269	The core loopback logic only verifies the data bits; an inverted SYNC pattern is not detected. The core now checks the SYNC pattern and data bits in the loopback logic.

Known Issues and Workarounds

There are no known issues in the current release.

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