PCN20005: RTG4 SET Filter Delay Calibration Update

May 6, 2020

Description of Change

RTG4 devices employ Single Event Transient (SET) filters for SET mitigation. These filters are optionally available for flip-flops in Fabric Logic Elements (LEs), IOFF, Mathblocks, and SRAM blocks through Libero SoC's global SET mitigation setting or the NDC set_mitigation constraint. SET mitigation is built-in to the SerDes and FDDR flip-flops. SpaceWire clock and data recovery circuits embedded in the clock conditioning circuits (CCCs) also include a similar, delay-based, glitch filter. Libero SoC v12.4 and v11.9 SP6 will include an update to ensure SET filters use the intended Process, Voltage, and Temperature (PVT) compensated delay values (600 ps typical) from the built-in Delay Calibration (DELCAL) circuits located at the SE and NE device corners.

Using delay calibration (DELCAL) circuits produces a filter delay closer to 600 ps (typical) regardless of the device process, voltage and temperature variation.

In all prior Libero releases, the SET filter delay could use either of the two unintended values below:

1. **Without Dynamic CCC in SE/NE corner:** Device might use uncalibrated mid-range default DELCAL value (600 ps typical) pre-programmed in flash configuration bits.
2. **With Dynamic CCC in SE/NE corner:** Device might use a smaller delay derived by calibrating to the smallest glitch-width target allowed by DELCAL.

This issue is caused by:

1. Libero SoC incorrectly tying DELCAL APB PSEL input high so that, the DELCAL APB slave interface is always selected whenever APB transactions occur at the respective device corner's shared APB interface.
2. An unintended early DELCAL start during power-up/DEVRST_N release, prior to the intended glitch-width target (600 ps typical) being loaded into the DELCAL configuration registers to over-write the power-on reset values (of all zeroes).

Libero SoC v12.4 and v11.9 SP6 will correctly tie-off DELCAL APB PSEL input to '0' and re-run the filter delay calibration near the end of the device power-up to functional sequence to obtain the desired, PVT compensated, SET filter delay.

Application Impact

- There is no impact to designs that have successfully completed functional and environmental qualification testing without errors, such as SB_CORRECT/DB_DETECT LSRAM flag assertion.
- There is no functionality impact if design does not use LSRAMs configured for non-pipelined ECC with SET mitigation.
- There is no impact to the SET mitigation level provided by RTG4 SET filters because all DELCAL delay values allow RTG4 SET filters in all device flip-flops to meet the RTG4 STMR-FF SET mitigation targets.
    - Even with the existence of unintended SET filter delay values, the radiation test reports published on the Microsemi *website* demonstrate a significant reduction in FF SEU cross-sections and error rates. For example, see the *2017 Space Forum Update* and the *2016 NASA MAPLD RTG4 Radiation Update*.
- LSRAMs using non-pipelined ECC mode (requires SET mitigation be enabled) could exhibit an ECC bit write error which causes SB_CORRECT flag assertion during read-back.
    - User data is written and read correctly but in some data words, a single-bit ECC error may occur that requires the use of the single-bit error correction capability, leaving only double-bit error detection for flight.
    - Affected LSRAM words have reduced radiation upset tolerance.

- The update to Libero SoC also reduces the total number of available 36-bit uPROM words from 10,400 to 10,370 so that space can be reserved for the instructions required to re-calibrate the filter delay.

Action Required

- Upgrade existing designs to Libero SoC v12.4 (or v11.9 SP6, once released, for designs completed with v11.x tools) and re-run the tool flow, including 'Generate FPGA Array Data' and 'Generate Bitstream' steps.
- Reprogram device with updated bitstream.
  - Completed designs that do not use the uPROM do not require re-running Place and Route, unless that step is invalidated due to other required updates as per the Libero SoC log window.
  - Completed designs containing uPROM instance require a uPROM core version upgrade and will revert to a pre-synthesis/pre-compile state.
- If design already passed functional/environmental qualification tests without SB_CORRECT flag errors, customer may fly the device as-is.
- If SB_CORRECT flags are observed, customer must assess whether flying with reduced ECC mitigation is acceptable to the mission's radiation performance goals.
- New designs must be upgraded to Libero SoC v12.4 or later.

Products Affected

The following table lists the affected products.

Table 1 • Affected Devices

Microsemi Part Number	DLA SMD Number
RT4G150-CG1657B	5962-1620801QXF
RT4G150-1CG1657B	5962-1620802QXF
RT4G150-LG1657B	5962-1620803QZC
RT4G150-1LG1657B	5962-1620804QZC
RT4G150-CG1657E	5962-1620805QXF
RT4G150-1CG1657E	5962-1620806QXF
RT4G150-LG1657E	5962-1620807QZC
RT4G150-1LG1657E	5962-1620808QZC
RT4G150-CG1657V	5962-1620809VXF
RT4G150-1CG1657V	5962-1620810VXF
RT4G150-LG1657V	5962-1620811VZC
RT4G150-1LG1657V	5962-1620812VZC
RT4G150-CQ352B	5962-1620813QYC
RT4G150-1CQ352B	5962-1620814QYC
RT4G150L-CG1657B	5962-1620815QXF
RT4G150L-LG1657B	5962-1620816QZC
RT4G150L-CQ352B	5962-1620817QYC
RT4G150L-CG1657E	5962-1620818QXF
RT4G150L-LG1657E	5962-1620819QZC

Microsemi Part Number	DLA SMD Number
RT4G150L-CG1657V	5962-1620820VXF
RT4G150L-LG1657V	5962-1620821VZC
RT4G150-1CB1657PROTO	
RT4G150-1CG1657PROTO	
RT4G150-1CQ352PROTO	
RT4G150-1LG1657PROTO	
RT4G150-CB1657PROTO	
RT4G150-CG1657PROTO	
RT4G150-CQ352PROTO	
RT4G150-LG1657PROTO	
RT4G150-1CG1657R	
RT4G150-1CQ352R	
RT4G150-1LG1657R	
RT4G150-CG1657R	
RT4G150-CQ352R	
RT4G150-LG1657R	
RT4G150-1CG1657M	
RT4G150-1CQ352M	
RT4G150-1LG1657M	
RT4G150-CG1657M	
RT4G150-CQ352M	
RT4G150-LG1657M	
RT4G150-FCG1657M	
RT4G150-FCG1657M	
RT4G150-FCG1657ES	
RT4G150-1FCG1657ES	

Contact Information

If you have any questions about this subject, contact Microsemi Technical Support department by using the support portal at *https://soc.microsemi.com/Portal/Default.aspx*.

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