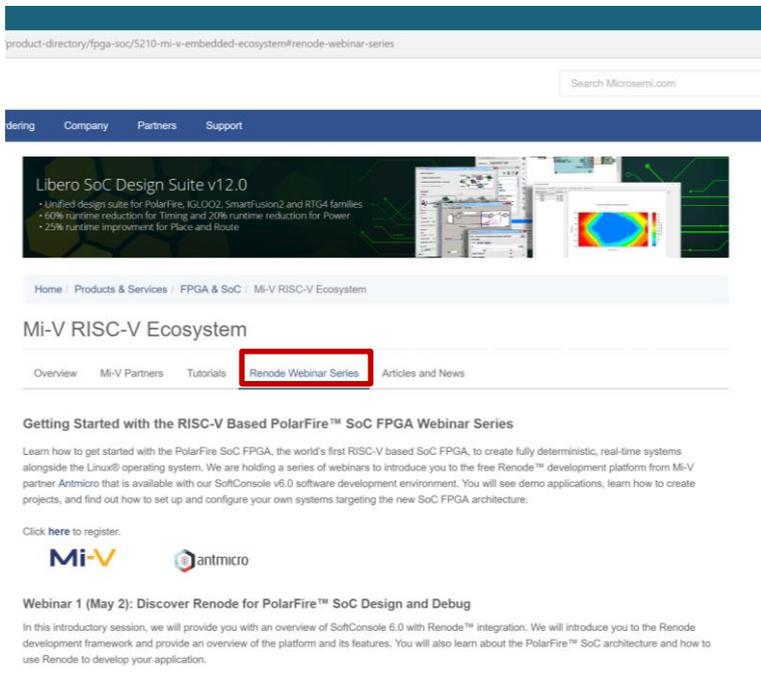




First / Second Thursdays

- Jan. 9 - Webinar 9: Getting Started with PolarFire® SoC**
- Feb. 13 - Webinar 10: Introduction to the PolarFire SoC Baremetal Library**
- Mar. 12 - Webinar 11: Handling Binaries**
- April 9 - Webinar 12: Two Baremetal Applications on PolarFire SoC**
- May 14 - Webinar 13: Linux on Renode**
- June 11 - Webinar 14: Building Applications for Linux on PolarFire SoC**
- July 9 - Webinar 15: Real-Time (AMP Mode) on PolarFire SoC**

www.microsemi.com/Mi-V “Renode Webinar Series”



The screenshot shows the Microsemi website's navigation and content for the Renode Webinar Series. At the top, there is a search bar and navigation links for "Ordering", "Company", "Partners", and "Support". Below this is a banner for "Libero SoC Design Suite v12.0" with bullet points: "Unified design suite for PolarFire, IGLOO2, SmartFusion2 and RTG4 families", "100% runtime reduction for Timing and 20% runtime reduction for Power", and "25% runtime improvement for Place and Route". A breadcrumb trail reads "Home > Products & Services > FPGA & SoC > Mi-V RISC-V Ecosystem". The "Mi-V RISC-V Ecosystem" section has a menu with "Overview", "Mi-V Partners", "Tutorials", "Renode Webinar Series" (highlighted with a red box), and "Articles and News". Below this is the heading "Getting Started with the RISC-V Based PolarFire™ SoC FPGA Webinar Series" and a paragraph of introductory text. At the bottom, there is a "Click here to register." link and logos for "Mi-V" and "antmicro".

Webinar 1: Discover Renode for PolarFire® SoC Design and Debug

Webinar 2: How to Get Started with Renode for PolarFire SoC

Webinar 3: Learn to Debug a Bare-Metal PolarFire SoC Application with Renode

Webinar 4: Tips and Tricks for Even Easier PolarFire SoC Debug with Renode

Webinar 5: Add and Debug PolarFire SoC models with Renode

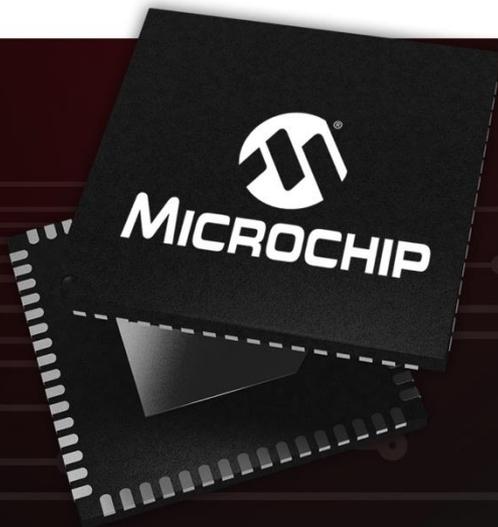
Webinar 6: Add and Debug Pre-Existing model in PolarFire SoC

Webinar 7: How to Write Custom Models

Webinar 8: What's New in SoftConsole v6.2



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Mixed-Signal, Analog & Flash-IP Solutions



Getting Started with the RISC-V Based PolarFire® SoC FPGA Webinar Series
Session 9: Getting Started with PolarFire® SoC

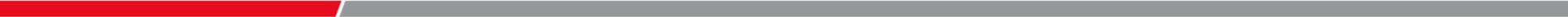
Hugh Breslin, Design Engineer
Thursday Jan. 9, 2019

Agenda

- **Getting Started with Libero SoC v12.3**
- **Creating a PolarFire SoC Design in Libero SoC v12.3**
- **Modifying the Renode Model and MPFS Blinky**



Getting Started with Libero SoC v12.3



Getting Started with Libero SoC v12.3

- www.microsemi.com/liberosoc
- Create a PolarFire SoC Project with an EAP license
- Libero SoC v12.3 released December 10th
- Libero SoC v12.0:
Software Tool of the Year – 2019 WEAA
- www.microsemi.com/polarfiresoc
- polarfiresoc@microchip.com



Getting Started with Libero SoC v12.3



The screenshot displays the Libero SoC v12.3 software interface. The window title is "Libero". The menu bar includes "Project", "File", "Edit", "View", "Design", "Tools", and "Help". The toolbar contains icons for file operations and design actions. The "StartPage" tab is active, showing a "Projects" sidebar with "New...", "Open...", "Recent Projects", and "Links" sections. The main content area features a "Welcome to Microsemi's Libero® SoC v12.3" message, followed by a detailed description of the design suite's capabilities and supported hardware. A "What's New in Libero SoC v12.3" section is also visible. The bottom of the interface includes a "Message" pane with filters for "Messages", "Errors", "Warnings", "Info", and "Manage suppressed messages", and a "Log" pane with a "Message" tab.

Welcome to Microsemi's Libero® SoC v12.3

Microsemi Libero® System-on-Chip (SoC) design suite offers high productivity with its comprehensive, easy to learn, easy to adopt development tools for designing with Microsemi's power efficient flash [FPGAs](#), [SoC FPGAs](#), and [Rad-Tolerant FPGAs](#). The suite integrates industry standard Synopsys [Synplify Pro®](#) synthesis and Mentor Graphics [ModelSim®](#) simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v12.3 for designing with Microsemi's [RTG4](#) Rad-Tolerant FPGAs, [SmartFusion®2](#) and [IGLOO® 2](#) SoC FPGAs, and [PolarFire](#) FPGAs.

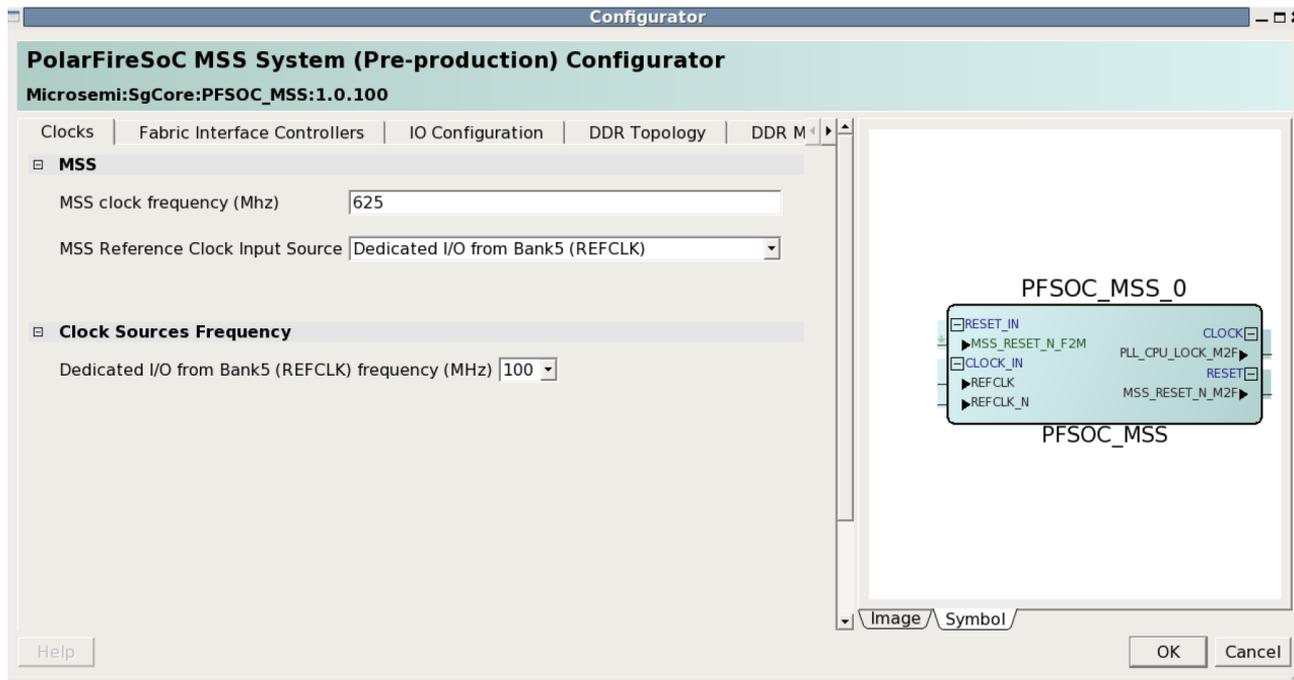
To design with Microsemi's older Flash FPGA families, use Libero SoC v11.9 and subsequent service packs.

What's New in Libero SoC v12.3

Getting Started with Libero SoC v12.3

Clocks tab:

- Set MSS clock frequency
- Select clock source
- Set reference frequency



The screenshot shows the "Configurator" window for the "PolarFireSoC MSS System (Pre-production) Configurator". The "Microsemi:SgCore:PFSOC_MSS:1.0.100" is selected. The "Clocks" tab is active, showing the following settings:

- MSS**
 - MSS clock frequency (Mhz): 625
 - MSS Reference Clock Input Source: Dedicated I/O from Bank5 (REFCLK)
- Clock Sources Frequency**
 - Dedicated I/O from Bank5 (REFCLK) frequency (MHz): 100

The right side of the window displays a block diagram of the "PFSOC_MSS" component. The diagram shows the component's ports and internal connections:

- RESET_IN** (input) connects to **MSS_RESET_N_F2M** (input) and **PLL_CPU_LOCK_M2F** (input).
- CLOCK_IN** (input) connects to **REFCLK** (input) and **REFCLK_N** (input).
- RESET** (output) connects to **MSS_RESET_N_M2F** (output).
- CLOCK** (output) connects to **MSS_RESET_N_M2F** (output).

The diagram is labeled "PFSOC_MSS_0" and "PFSOC_MSS".

Getting Started with Libero SoC v12.3

Fabric Interface Controllers:

FIC 0 AXI4

- Master
- Slave

FIC 1 AXI4

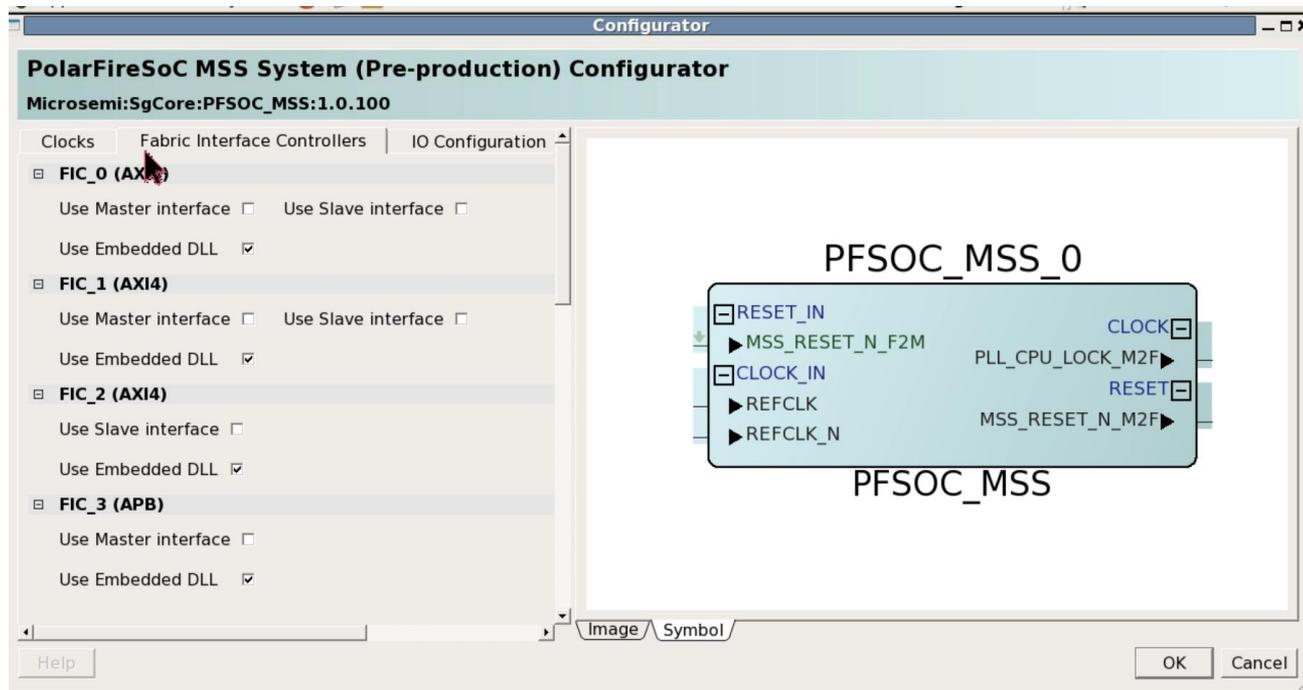
- Master
- Slave

FIC 2 AXI4

- Slave

FIC 3 APB

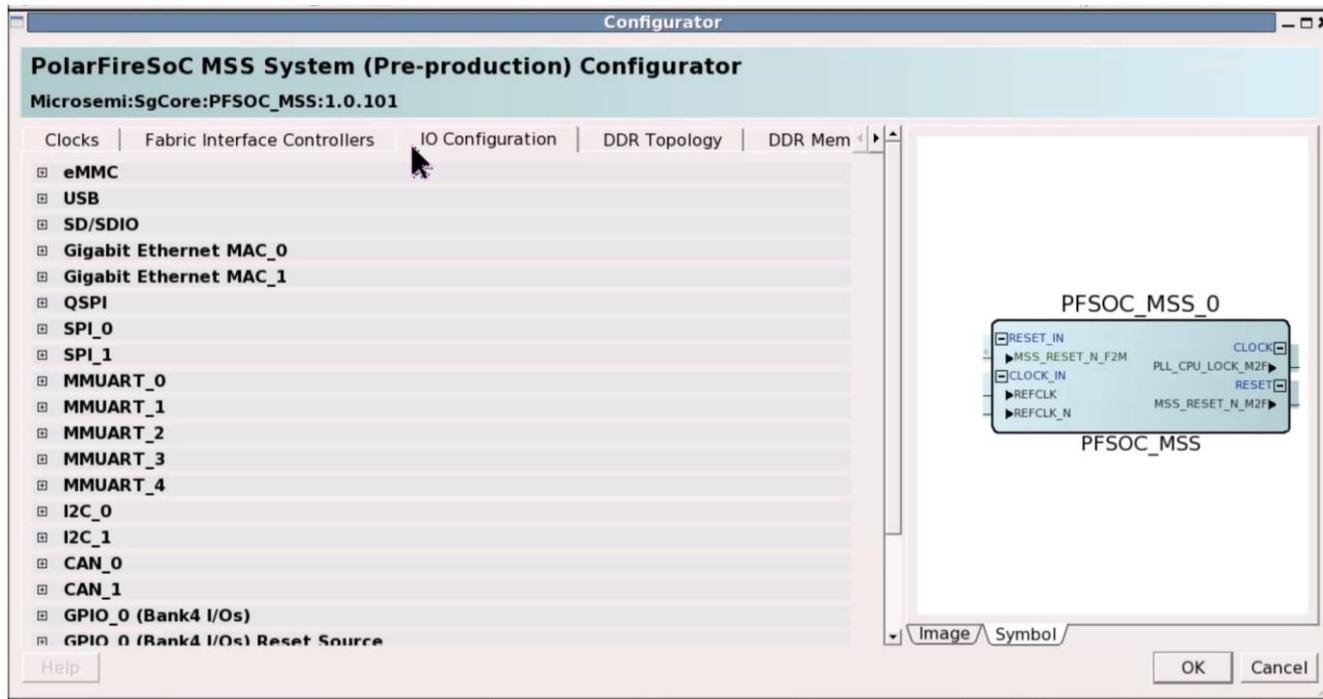
- Master



Getting Started with Libero SoC v12.3

IO Configurations Available:

- eMMC
- USB
- SD/SDIO
- GEM0 / 1
- QSPI
- SPI_0
- SPI_1
- MMUART_0
- MMUART_1
- MMUART_2
- MMUART_3
- MMUART_4
- I2C_0
- I2C_1
- CAN_0
- CAN_1
- GPIO_0 (Bank4 I/Os)
- GPIO_0 (Bank4 I/Os) Reset Source



Getting Started with Libero SoC v12.3

The “Image” tab highlights IOs in use and their configurations

Configurator

PolarFireSoC MSS System (Pre-production) Configurator
 Microsemi:SGCore:PFSoC_MSS:1.0.100

Clocks | Fabric Interface Controllers | **IO Configuration** | DDR Topology | DDR Memory

| BANK | IO MUX | Package Pin | eMMC | USB | SD | MAC | OSPI | SPI | MMUART | I2C | CAN | GPIO | |
|--------|--------|-------------|------------|-----------------|-----------------|---------------|-------------|--------------|-----------------|-------------------|-------------------|-------------------|-----------|
| BANK 0 | 0 | AA8 | EMMC_CLK | | SD_CLK | | OSPI_CLK | SPI_0_CLK | | | | GPIO_0_0 | |
| | 1 | AA9 | EMMC_CMD | | SD_CMD | | | | MMUART_3_RXD | I2C_0_SCL | | GPIO_0_1 | |
| | 2 | AA7 | EMMC_DATA0 | | SD_DATA0 | | | | MMUART_3_TXD | I2C_0_SDA | | GPIO_0_2 | |
| | 3 | V6 | EMMC_DATA1 | | SD_DATA1 | | | | MMUART_4_RXD | | CAN_0_TXBUS | GPIO_0_3 | |
| | 4 | AA10 | EMMC_DATA2 | | SD_DATA2 | | | | MMUART_4_TXD | | CAN_0_RXBUS | GPIO_0_4 | |
| | 5 | AA12 | EMMC_DATA3 | | SD_DATA3 | | | | MMUART_0_RXD(A) | | CAN_0_TX_EBL_N | GPIO_0_5 | |
| | 6 | V10 | EMMC_STRB | | SD_CD | | | | MMUART_0_TXD(A) | | | GPIO_0_6 | |
| | 7 | V7 | EMMC_RSTN | | SD_WP | MAC_1_MDC | | | MMUART_2_RXD | I2C_1_SCL | | GPIO_0_7 | |
| | 8 | V14 | EMMC_DATA4 | | SD_P0W | MAC_1_MDIO | OSPI_SS0 | | MMUART_2_TXD | I2C_1_SDA | | GPIO_0_8 | |
| | 9 | V13 | EMMC_DATA5 | | SD_VOLT_SEL | MAC_0_MDC | OSPI_DATA0 | | MMUART_0_RXD(B) | | | GPIO_0_9 | |
| | 10 | V8 | EMMC_DATA6 | | SD_VOLT_EN | MAC_0_MDIO | OSPI_DATA1 | | MMUART_0_TXD(B) | | | GPIO_0_10 | |
| | 11 | V11 | EMMC_DATA7 | | SD_VOLT_CMD_DIR | | OSPI_DATA2 | SPI_0_DO | MMUART_1_RXD | | CAN_1_TXBUS | GPIO_0_11 | |
| | 12 | AA12 | | | SD_VOLT_DIR_0 | | OSPI_DATA3 | SPI_0_DI | MMUART_1_TXD | | CAN_1_RXBUS | GPIO_0_12 | |
| 13 | V12 | | | SD_VOLT_DIR_1_3 | | | SPI_0_SS0 | | | CAN_1_TX_EBL_N | GPIO_0_13 | | |
| BANK 1 | 14 | W6 | | USB_CLK | | | OSPI_CLK(A) | SPI_1_CLK(A) | | | | GPIO_1_0 | |
| | 15 | V6 | | USB_DIR | | MAC_1_MDC(A) | | SPI_1_DO(A) | MMUART_4_RXD | | | GPIO_1_1 | |
| | 16 | W8 | | USB_NXT | | MAC_1_MDIO(A) | | SPI_1_DI(A) | MMUART_4_TXD | | | GPIO_1_2 | |
| | 17 | V8 | | USB_STP | | | | SPI_1_SS0(A) | MMUART_0_RXD(A) | | | GPIO_1_3 | |
| | 18 | V4 | | USB_DATA0 | | | | | MMUART_0_TXD(A) | | | GPIO_1_4 | |
| | 19 | U5 | | USB_DATA1 | | | | | MMUART_1_RXD | | | GPIO_1_5 | |
| | 20 | W9 | | USB_DATA2 | | | | | MMUART_1_TXD | I2C_0_SCL(A) | | GPIO_1_6 | |
| | 21 | U7 | | USB_DATA3 | | | | | MMUART_2_RXD | I2C_0_SDA(A) | CAN_0_TX_EBL_N(A) | GPIO_1_7 | |
| | 22 | U6 | | USB_DATA4 | | | | | MMUART_2_TXD | | CAN_0_TXBUS(A) | GPIO_1_8 | |
| | 23 | V7 | | USB_DATA5 | | | | SPI_0_SS0 | MMUART_3_RXD | | CAN_0_RXBUS(A) | GPIO_1_9 | |
| | 24 | V9 | | USB_DATA6 | | MAC_0_MDC(A) | | SPI_0_DI | MMUART_2_TXD | I2C_1_SCL(A) | | GPIO_1_10 | |
| | 25 | U9 | | USB_DATA7 | | MAC_0_MDIO(A) | | SPI_0_DO | | I2C_1_SDA(A) | | GPIO_1_11 | |
| | 26 | V14 | | SD_LED(A) | | | | | | I2C_1_SCL(B) | | GPIO_1_12 | |
| BANK 2 | 27 | V13 | | SD_VOLT_0(A) | | | | | I2C_1_SDA(B) | CAN_1_TX_EBL_N(A) | | GPIO_1_13 | |
| | 28 | W10 | | SD_VOLT_1(A) | | MAC_1_MDC(B) | | | MMUART_0_RXD(B) | | CAN_1_TXBUS(A) | GPIO_1_14 | |
| | 29 | W11 | | SD_VOLT_2(A) | | MAC_1_MDIO(B) | | | MMUART_0_TXD(B) | | CAN_1_RXBUS(A) | GPIO_1_15 | |
| | 30 | W14 | | | | | OSPI_CLK(B) | SPI_1_CLK(B) | | | | GPIO_1_16 | |
| | 31 | W13 | | | | | OSPI_SS0 | SPI_1_SS0(B) | | | CAN_0_TXBUS(B) | GPIO_1_17 | |
| | 32 | U11 | | | SD_CLE | | OSPI_DATA0 | SPI_1_DO(B) | | | CAN_0_RXBUS(B) | GPIO_1_18 | |
| | 33 | U12 | | | SD_LED(B) | | OSPI_DATA1 | SPI_1_DI(B) | | | CAN_0_TX_EBL_N(B) | GPIO_1_19 | |
| | 34 | V11 | | | SD_VOLT_0(B) | | OSPI_DATA2 | | | | CAN_1_TXBUS(B) | GPIO_1_20 | |
| | 35 | U10 | | | SD_VOLT_1(B) | MAC_0_MDC(B) | OSPI_DATA3 | | | MMUART_0_RXD(C) | I2C_0_SCL(B) | GPIO_1_21 | |
| | 36 | U14 | | | SD_VOLT_2(B) | MAC_0_MDIO(B) | | | | MMUART_0_TXD(C) | I2C_0_SDA(B) | GPIO_1_22 | |
| | 37 | V12 | | | | | | OSPI_CLK(C) | SPI_0_CLK | | | CAN_1_TX_EBL_N(B) | GPIO_1_23 |

Image / Symbol

Help OK Cancel



Getting Started with Libero SoC v12.3

PolarFireSoC MSS System (Pre-production) Configurator

Microsemi:SgCore:PFSOC_MSS:1.0.100

Clocks | Fabric Interface Controllers | IO Configuration | DDR Topology | DDR Memory Initialization | DDR Memory Timing | DDR Controller | Misc |



Getting Started with Libero SoC v12.3

Debug Trace:

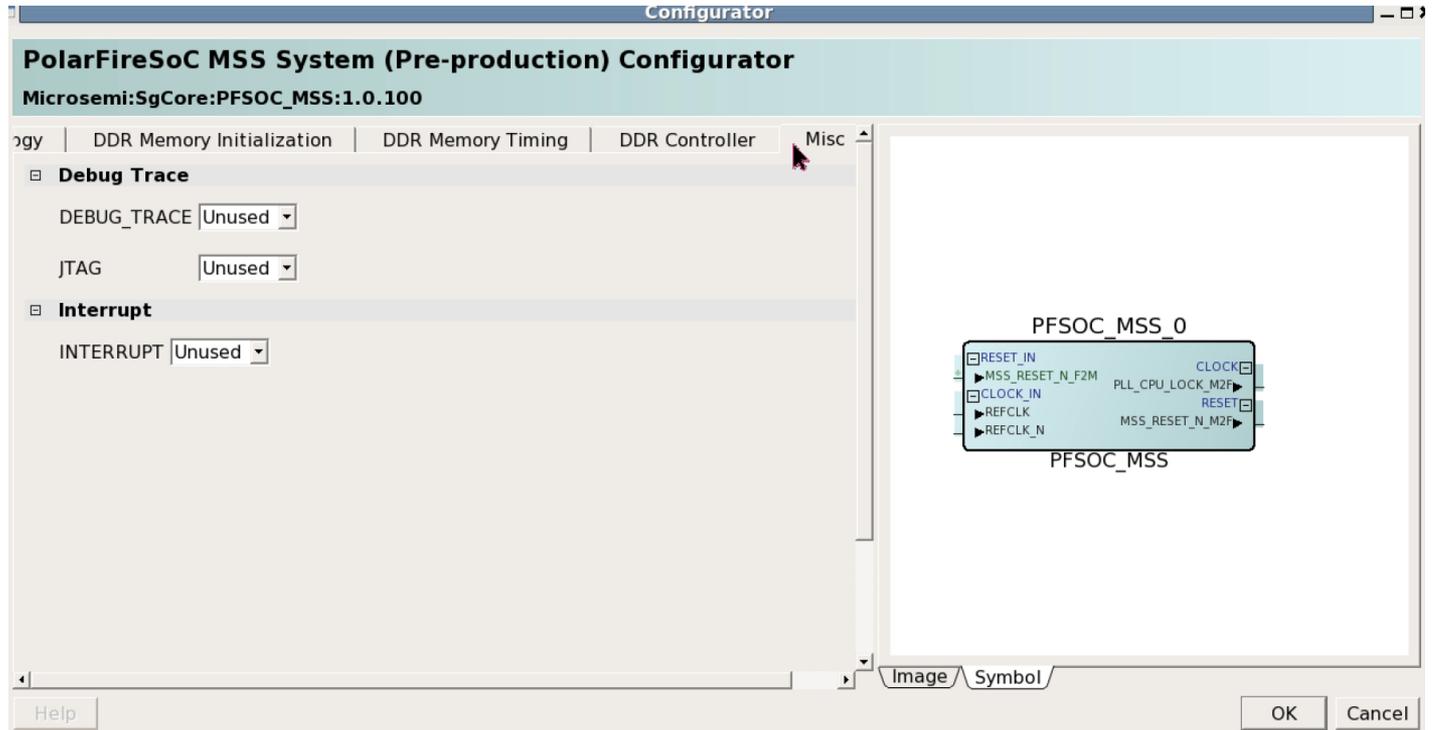
Expose UltraSoC
Debug pins to the
fabric

JTAG:

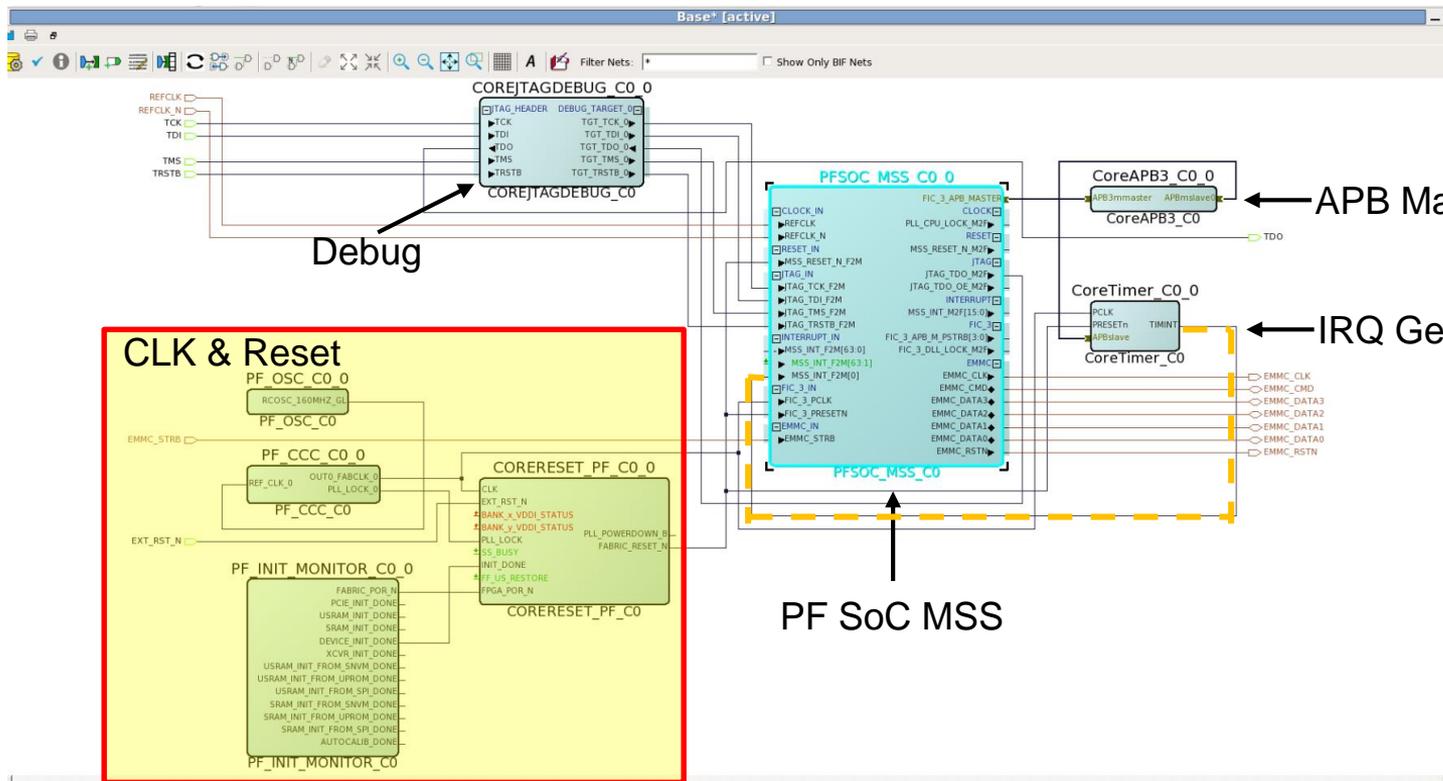
Expose fabric JTAG
debug pins

Interrupt:

Expose 64 interrupt
pins to the fabric



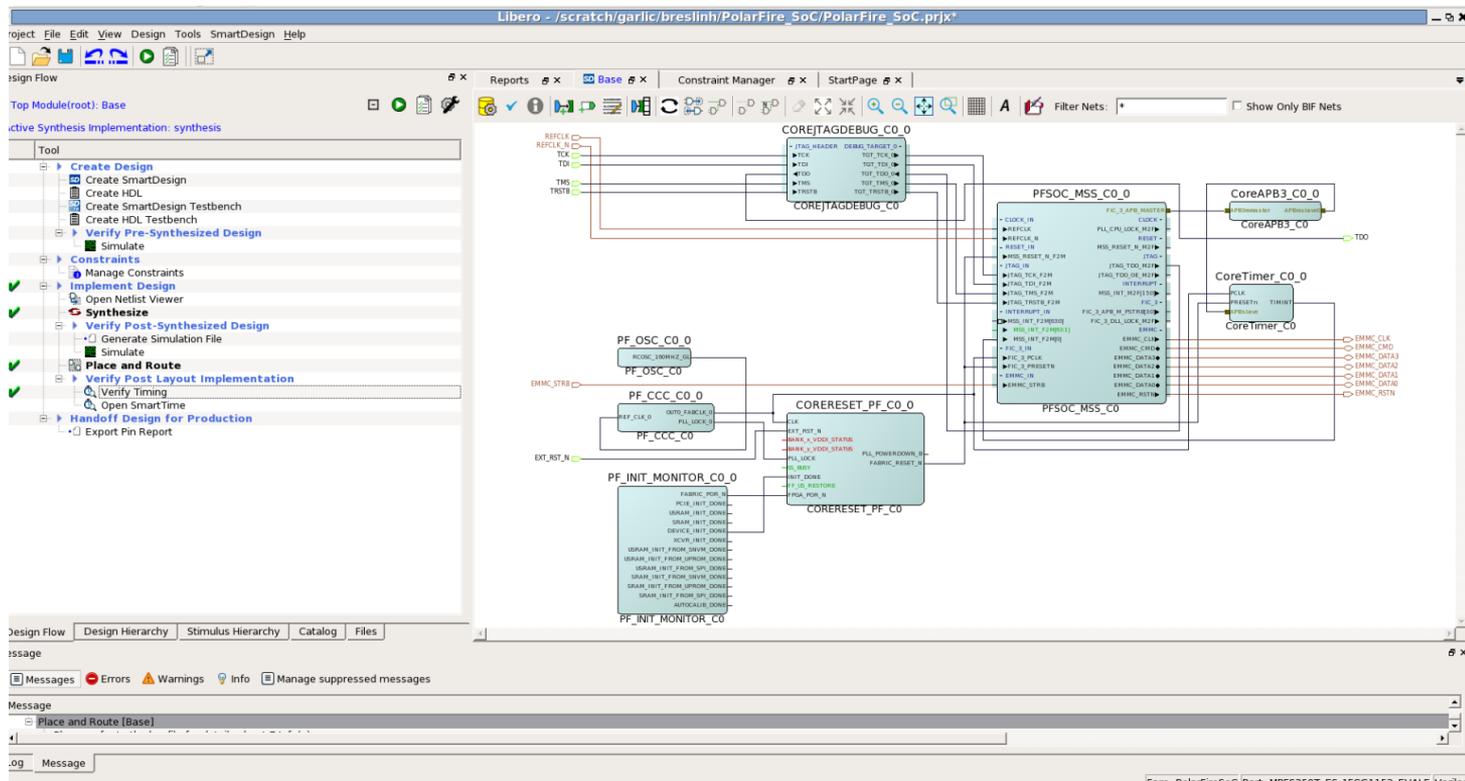
Getting Started with Libero SoC v12.3



Getting Started with Libero SoC v12.3

Currently Available:

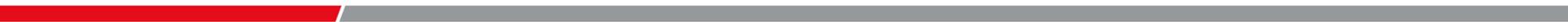
- Synthesis
- Place and Route
- Timing Verification



The screenshot shows the Libero SoC v12.3 interface. The top menu bar includes Project, File, Edit, View, Design, Tools, and SmartDesign. The main workspace displays a block diagram of the SoC with various components and their interconnections. The left sidebar shows the project flow, with 'Place and Route' highlighted. The bottom status bar shows 'Place and Route (Base)'. The interface is titled 'Libero - /scratch/garlic/breslinh/PolarFire_SoC/PolarFire_SoC.prjx*'. The main window shows a block diagram with components like COREJTAGDEBUG_CO_0, PFSOC_MSS_CO_0, CoreAPB3_CO_0, CoreTimer_CO_0, PF_OSC_CO_0, PF_CCC_CO_0, CORERESET_PF_CO_0, and PF_INIT_MONITOR_CO_0. The diagram shows various signals and connections between these components.



Creating a PolarFire SoC Design in Liberio SoC v12.3

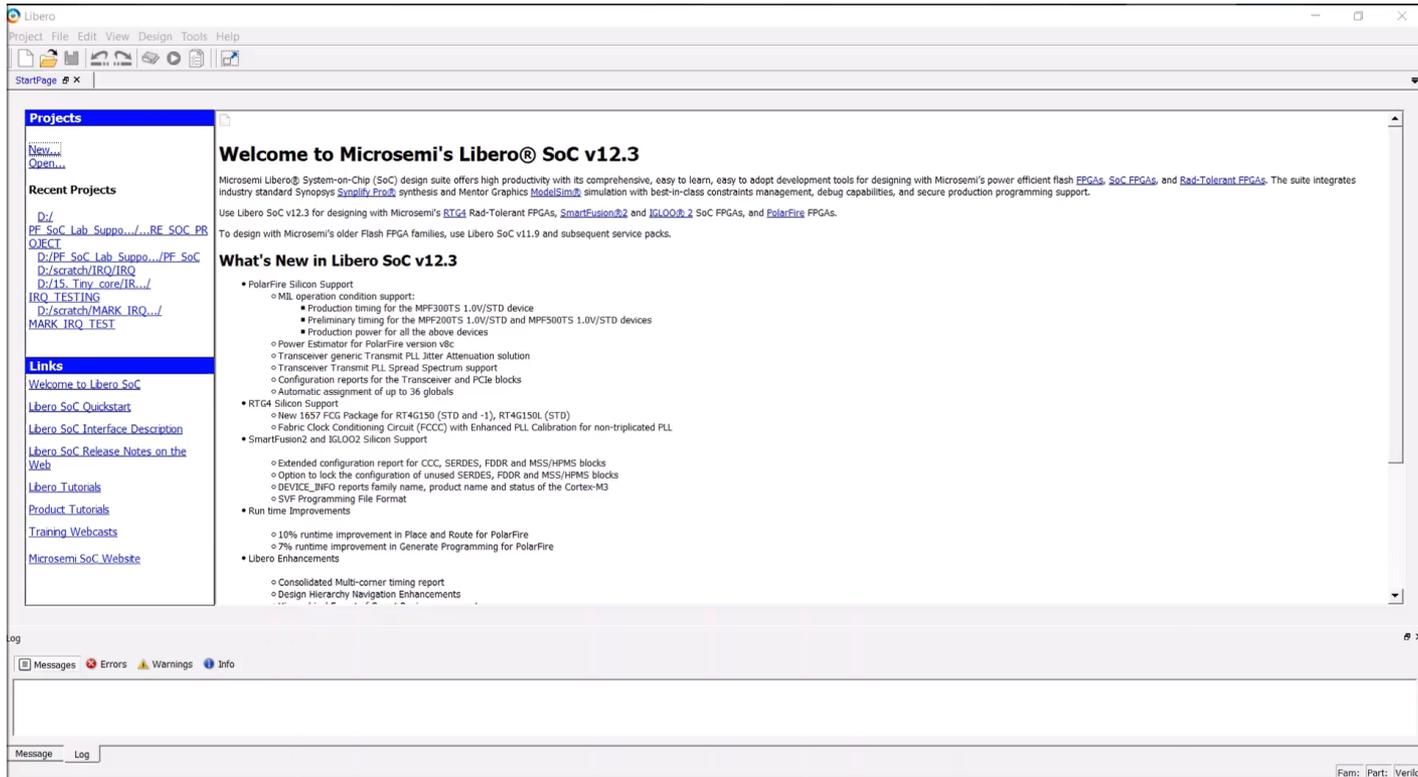




Creating a PolarFire SoC Design in Libero SoC v12.3

- **Create the Project**
- **Configure the MSS**
- **Configure Fabric Clock and Reset**
- **Add Debug**
- **Add an Interrupt Generating Timer**

Creating a PolarFire SoC Design in Libero SoC v12.3



Libero

Project File Edit View Design Tools Help

StartPage # x

Projects

New...
Open...

Recent Projects

D:/
PF_SoC_Lab_Suppo.../RE_SoC_PR
OJECT
D:/PF_SoC_Lab_Suppo.../PF_SoC
D:/scratch/IRQ/IRQ
D/15_Tiny_core/IR.../
IRQ_TESTING
D:/scratch/MARK_IRQ.../
MARK_IRQ_TEST

Links

Welcome to Libero SoC
Libero SoC Quickstart
Libero SoC Interface Description
Libero SoC Release Notes on the
Web
Libero Tutorials
Product Tutorials
Training Webcasts
Microsemi SoC Website

Welcome to Microsemi's Libero® SoC v12.3

Microsemi Libero® System-on-Chip (SoC) design suite offers high productivity with its comprehensive, easy to learn, easy to adopt development tools for designing with Microsemi's power efficient flash [FPGAs](#), [SoC FPGAs](#), and [Rad-Tolerant FPGAs](#). The suite integrates industry standard Synopsys [Simplify Front](#), synthesis and Mentor Graphics [ModelSim](#) simulation with best-in-class constraints management, debug capabilities, and secure production programming support.

Use Libero SoC v12.3 for designing with Microsemi's [RTG4](#) Rad-Tolerant FPGAs, [SmartFusion2](#) and [IGLOO2](#) SoC FPGAs, and [PolarFire](#) FPGAs.

To design with Microsemi's older Flash FPGA families, use Libero SoC v11.9 and subsequent service packs.

What's New in Libero SoC v12.3

- PolarFire Silicon Support
 - Mill operation condition support:
 - Production timing for the MPF300TS 1.0V/STD device
 - Preliminary timing for the MPF200TS 1.0V/STD and MPF500TS 1.0V/STD devices
 - Production power for all the above devices
 - Power Estimator for PolarFire version v1c
 - Transceiver generic Transmit PLL Jitter Attenuation solution
 - Transceiver Transmit PLL Spread Spectrum support
 - Configuration reports for the Transceiver and PCIe blocks
 - Automatic assignment of up to 36 globals
- RTG4 Silicon Support
 - New 1657 FCG Package for RT4G150 (STD and -1), RT4G150L (STD)
 - Fabric Clock Conditioning Circuit (FCCC) with Enhanced PLL Calibration for non-triplicated PLL
- SmartFusion2 and IGLOO2 Silicon Support
 - Extended configuration report for CCC, SERDES, FDDR and MSS/HPMS blocks
 - Option to lock the configuration of unused SERDES, FDDR and MSS/HPMS blocks
 - DEVICE_INFO reports family name, product name and status of the Cortex-M3
 - SVF Programming File Format
- Run time Improvements
 - 10% runtime improvement in Place and Route for PolarFire
 - 7% runtime improvement in Generate Programming for PolarFire
- Libero Enhancements
 - Consolidated Multi-corner timing report
 - Design Hierarchy Navigation Enhancements

log # x

Messages Errors Warnings Info

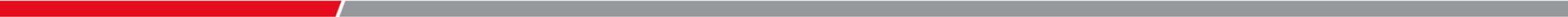
Message Log

Fam: Part: IVerilog

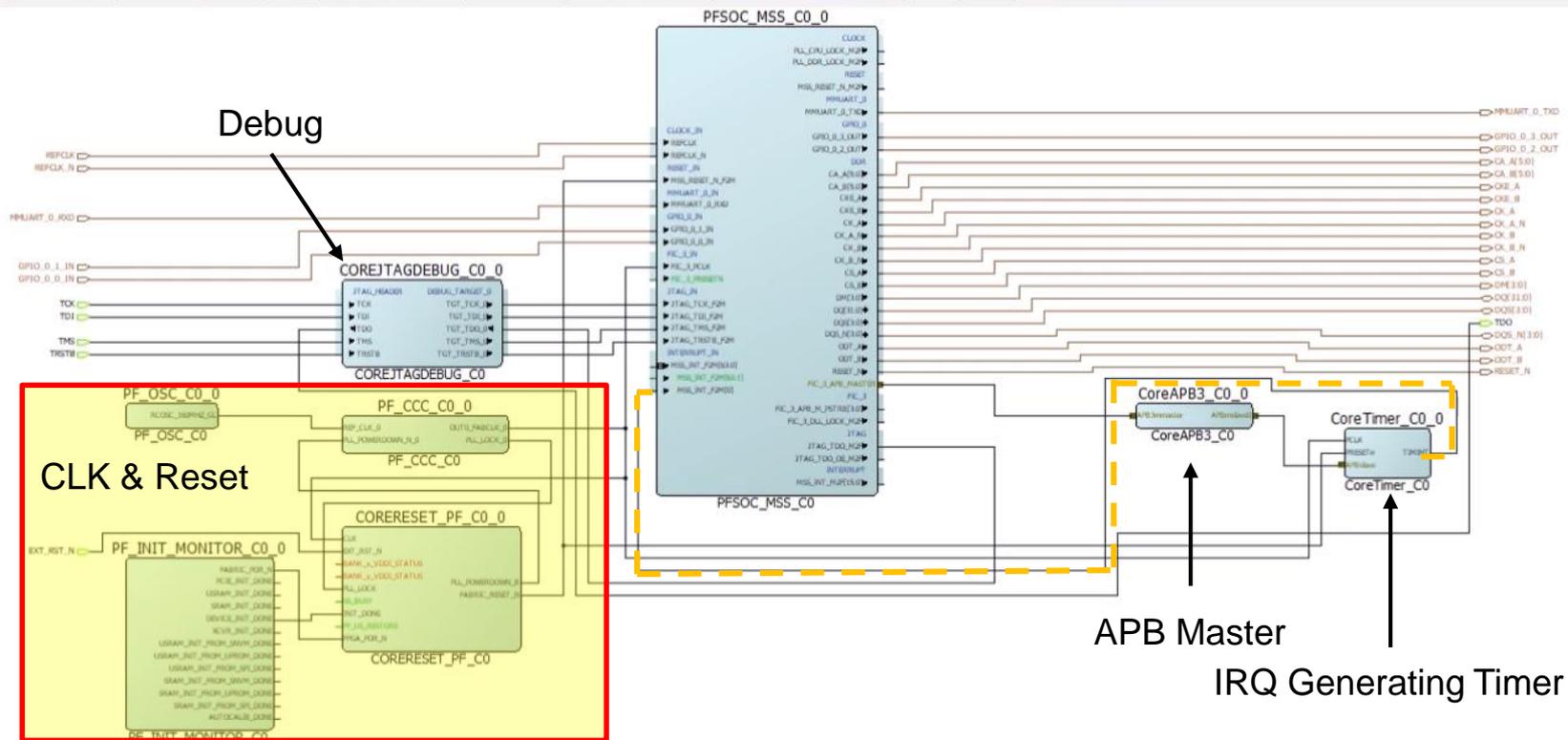


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Modifying the Renode Model and MPFS Blinky



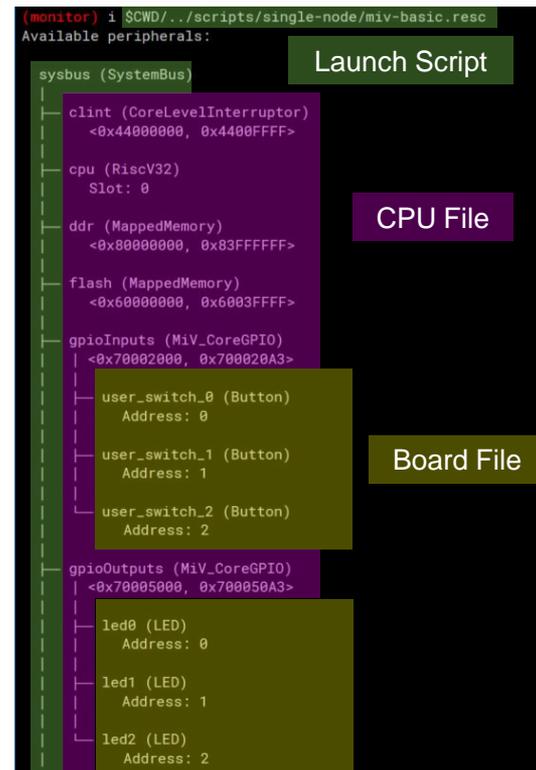
Modifying the Renode Model and MPFS Blinky



Modifying the Renode Model and MPFS Blinky

- The timer needs to be added to the CPU file
- It connects to sysbus directly – there is no need for an apb master
- The FIC3 address is 0x40_0000_0000
- The timer interrupt needs to be connected to the fabric interrupts

```
(monitor) 1 $CWD/./scripts/single-node/miv-basic.resc
Available peripherals:
```



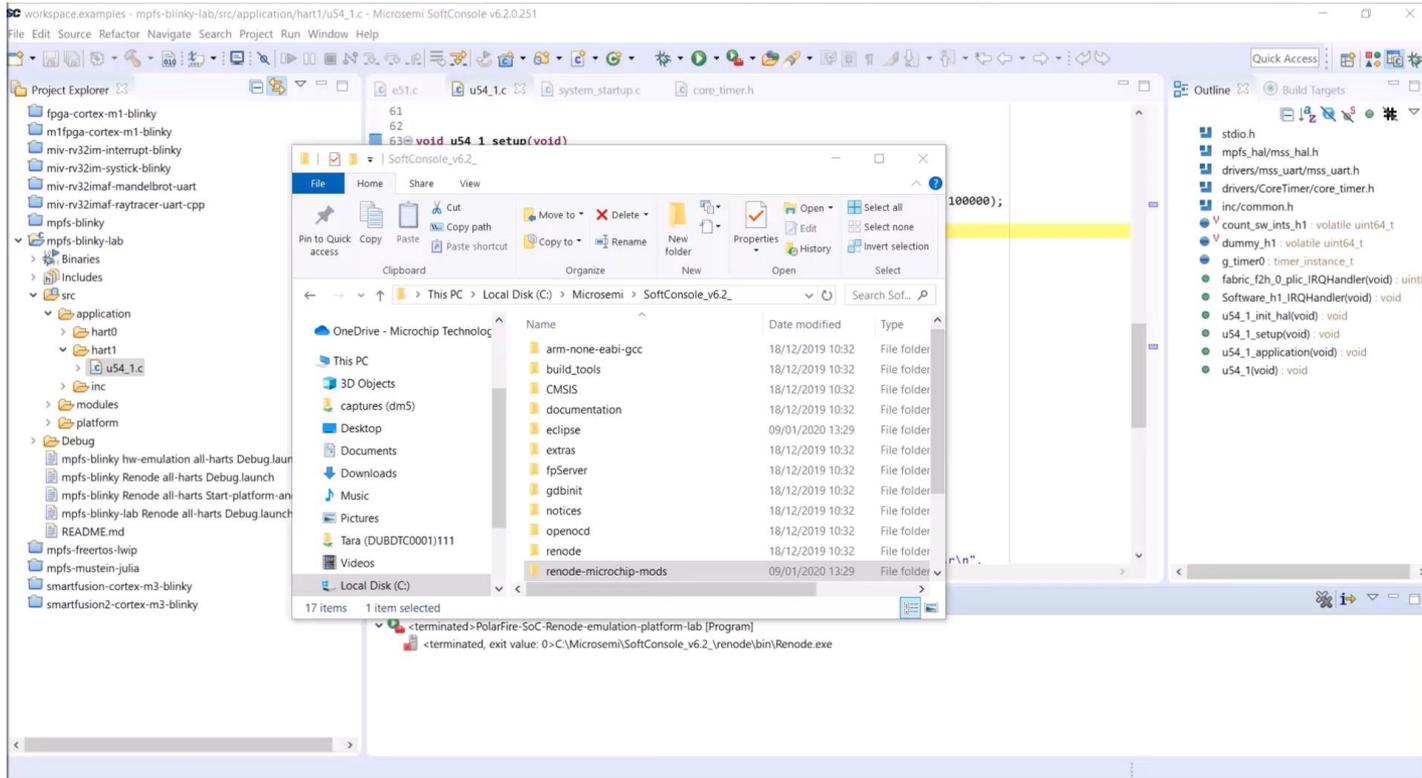
```
sysbus (SystemBus)
├── clint (CoreLevelInterruptor)
│   ├── <0x44000000, 0x4400FFFF>
├── cpu (RiscV32)
│   └── Slot: 0
├── ddr (MappedMemory)
│   └── <0x80000000, 0x83FFFFFF>
├── flash (MappedMemory)
│   └── <0x60000000, 0x6003FFFF>
├── gpioInputs (MiV_CoreGPIO)
│   ├── <0x70002000, 0x700020A3>
│   ├── user_switch_0 (Button)
│   │   └── Address: 0
│   ├── user_switch_1 (Button)
│   │   └── Address: 1
│   └── user_switch_2 (Button)
│       └── Address: 2
├── gpioOutputs (MiV_CoreGPIO)
│   ├── <0x70005000, 0x700050A3>
│   ├── led0 (LED)
│   │   └── Address: 0
│   ├── led1 (LED)
│   │   └── Address: 1
│   └── led2 (LED)
│       └── Address: 2
```



Modifying the Renode Model and MPFS Blinky

- **Drivers for the timer need to be added to the software project**
- **The timer needs to be configured and started**
- **The handler for the external interrupt to be used needs to be added to the software**

Modifying the Renode Model and MPFS Blinky



The screenshot displays an IDE environment with a code editor and a file explorer window. The code editor shows a C function `void u54_1_setup(void)` with a yellow highlight on the line `0x00000000);`. The file explorer window shows the directory structure of `SoftConsole_v6_2`, listing various folders and files.

File Explorer Window:

| Name | Date modified | Type |
|-----------------------|------------------|-------------|
| arm-none-eabi-gcc | 18/12/2019 10:32 | File folder |
| build_tools | 18/12/2019 10:32 | File folder |
| CMSIS | 18/12/2019 10:32 | File folder |
| documentation | 18/12/2019 10:32 | File folder |
| eclipse | 09/01/2020 13:29 | File folder |
| extras | 18/12/2019 10:32 | File folder |
| fpServer | 18/12/2019 10:32 | File folder |
| gdbinit | 18/12/2019 10:32 | File folder |
| notices | 18/12/2019 10:32 | File folder |
| openocd | 18/12/2019 10:32 | File folder |
| renode | 18/12/2019 10:32 | File folder |
| renode-microchip-mods | 09/01/2020 13:29 | File folder |

Code Editor Content:

```
void u54_1_setup(void)
{
    // ...
    0x00000000);
    // ...
}
```

Agenda

- **Getting Started with Libero SoC v12.3**
- **Creating a PolarFire SoC Design in Libero SoC v12.3**
- **Modifying the Renode Model and MPFS Blinky**



MICROCHIP

Thank You

Any Questions?

