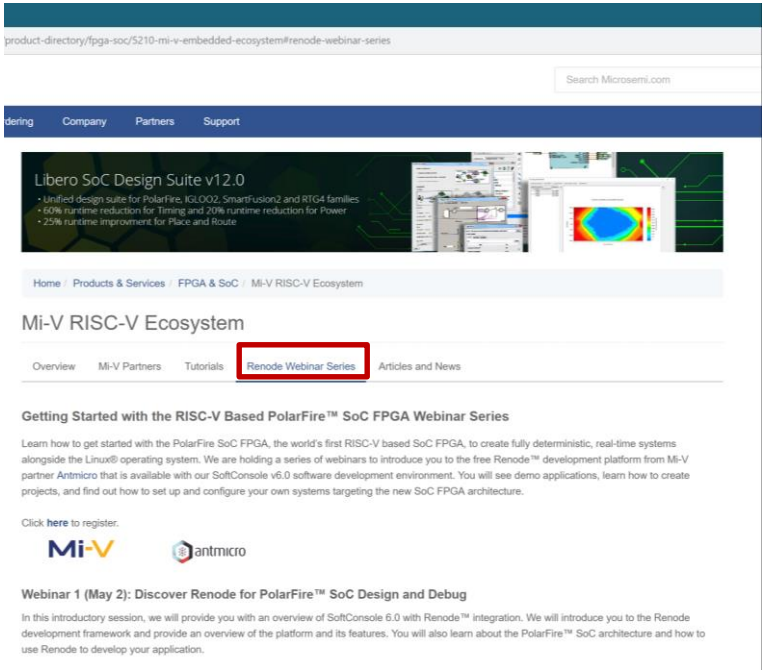
First / Second Thursdays

Jan. 9	-	Webinar 9: Getting Started with PolarFire®SoC
Feb. 13	-	Webinar 10: Introduction to the PolarFire SoC Baremetal Library
Mar. 12	-	Webinar 11: Handling Binaries
April 9	-	Webinar 12: Two Baremetal Applications on PolarFire SoC
May 14	-	Webinar 13: Linux on Renode
June 11	-	Webinar 14: Building Applications for Linux on PolarFire SoC
July 9	-	Webinar 15: Real-Time (AMP Mode) on PolarFire SoC

Supporting Content

www.microsemi.com/Mi-V “Renode Webinar Series”



Webinar 1: Discover Renode for PolarFire® SoC Design and Debug

Webinar 2: How to Get Started with Renode for PolarFire SoC

Webinar 3: Learn to Debug a Bare-Metal PolarFire SoC Application with Renode

Webinar 4: Tips and Tricks for Even Easier PolarFire SoC Debug with Renode

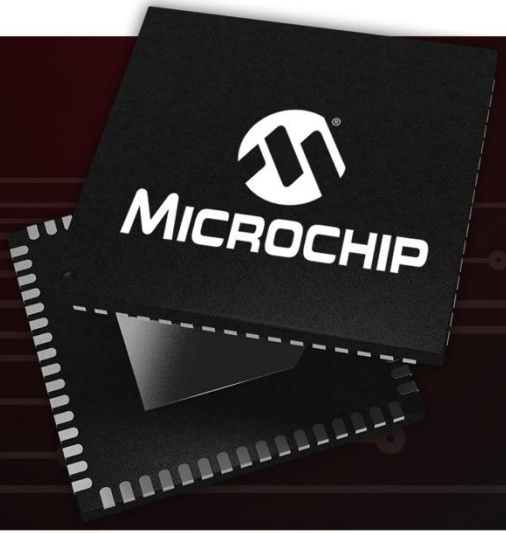
Webinar 5: Add and Debug PolarFire SoC models with Renode

Webinar 6: Add and Debug Pre-Existing model in PolarFire SoC

Webinar 7: How to Write Custom Models

Webinar 8: What’s New in SoftConsole v6.2

MICROCHIP



A Leading Provider of Microcontroller, Security, Mixed-Signal, Analog & Flash-IP Solutions




Getting Started with the RISC-V Based PolarFire® SoC FPGA Webinar Series
Session 9: Getting Started with PolarFire® SoC

Hugh Breslin, Design Engineer

Thursday Jan. 9, 2019

Agenda

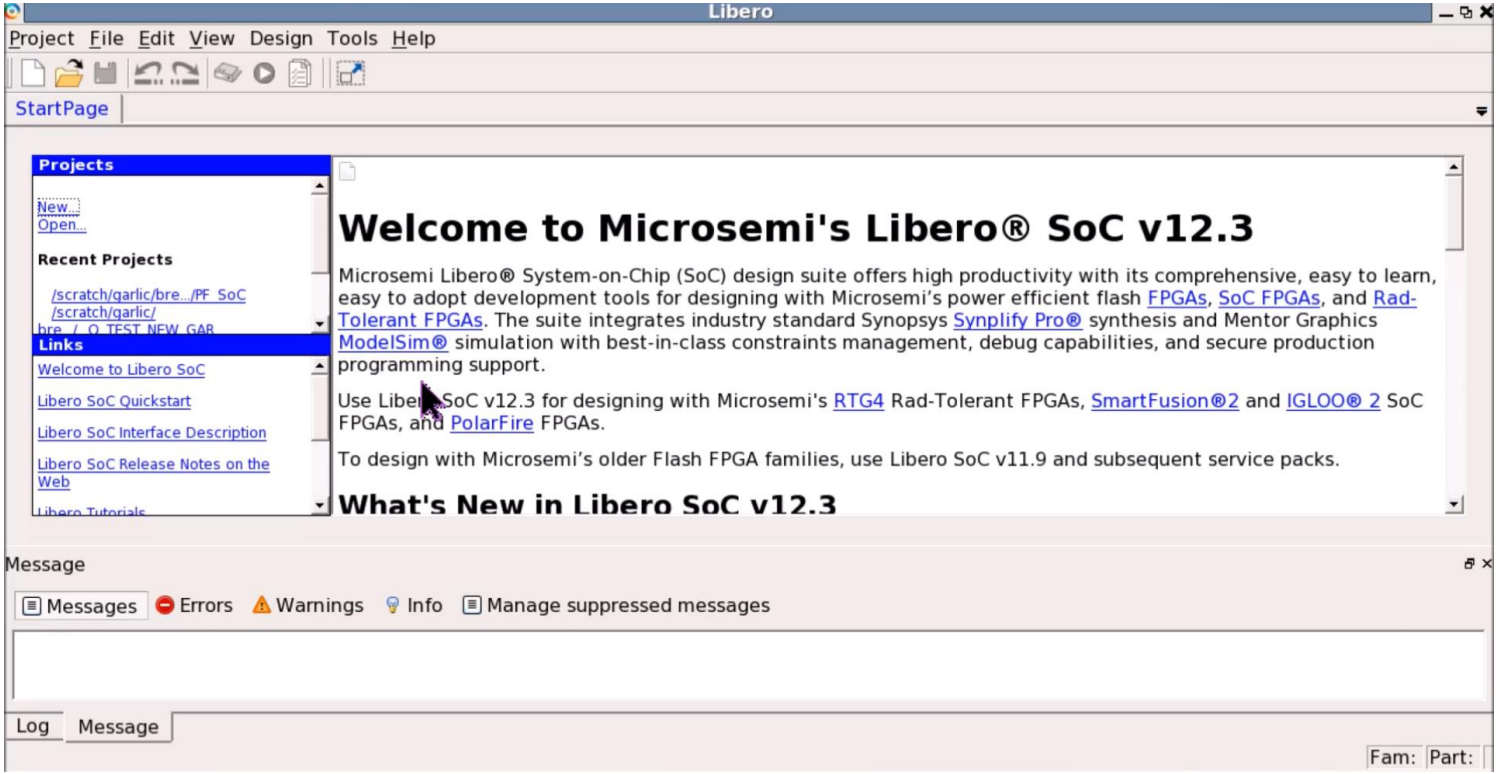
- Getting Started with Libero SoC v12.3
- Creating a PolarFire SoC Design in Libero SoC v12.3
- Modifying the Renode Model and MPFS Blinky

Getting Started with Libero SoC v12.3

Getting Started with Libero SoC v12.3

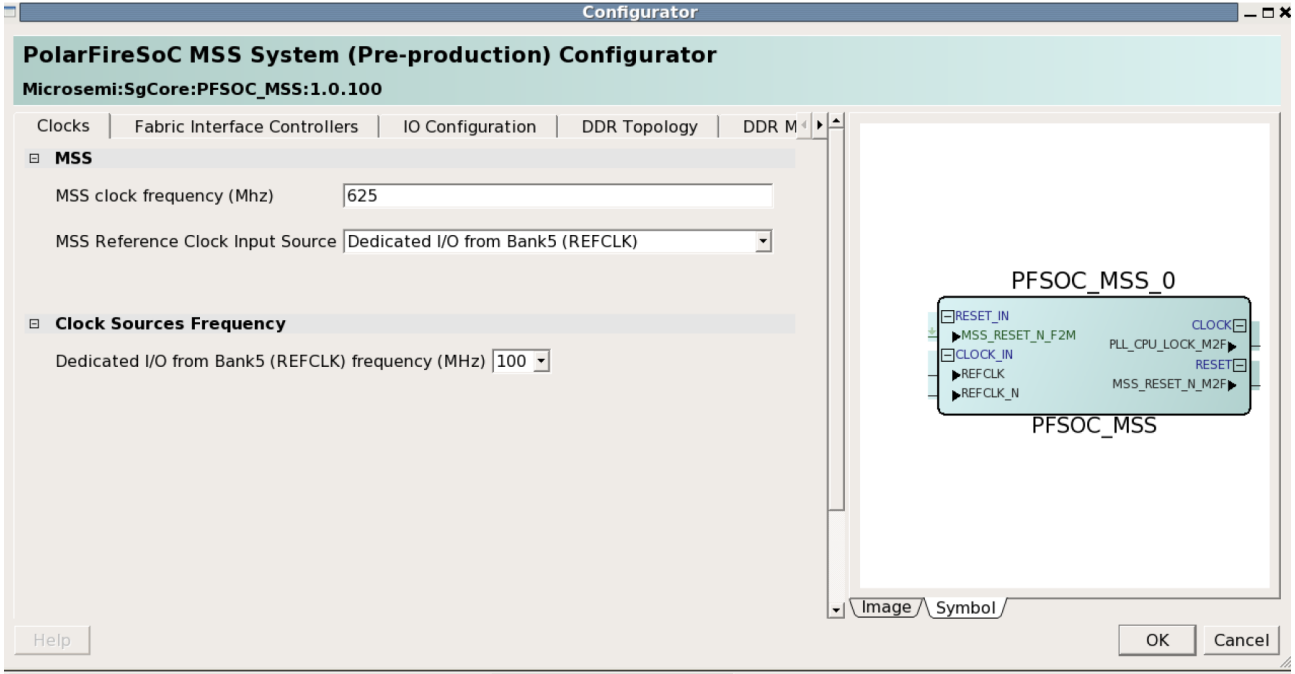
- www.microsemi.com/liberosoc
- Create a PolarFire SoC Project with an EAP license
- Libero SoC v12.3 released December 10th
- Libero SoC v12.0:
  Software Tool of the Year – 2019 WEAA
- www.microsemi.com/polarfiresoc
- polarfiresoc@microchip.com

Getting Started with Libero SoC v12.3



Getting Started with Libero SoC v12.3

Clocks tab:
Set MSS clock frequency
Select clock source
Set reference frequency



Getting Started with Libero SoC v12.3

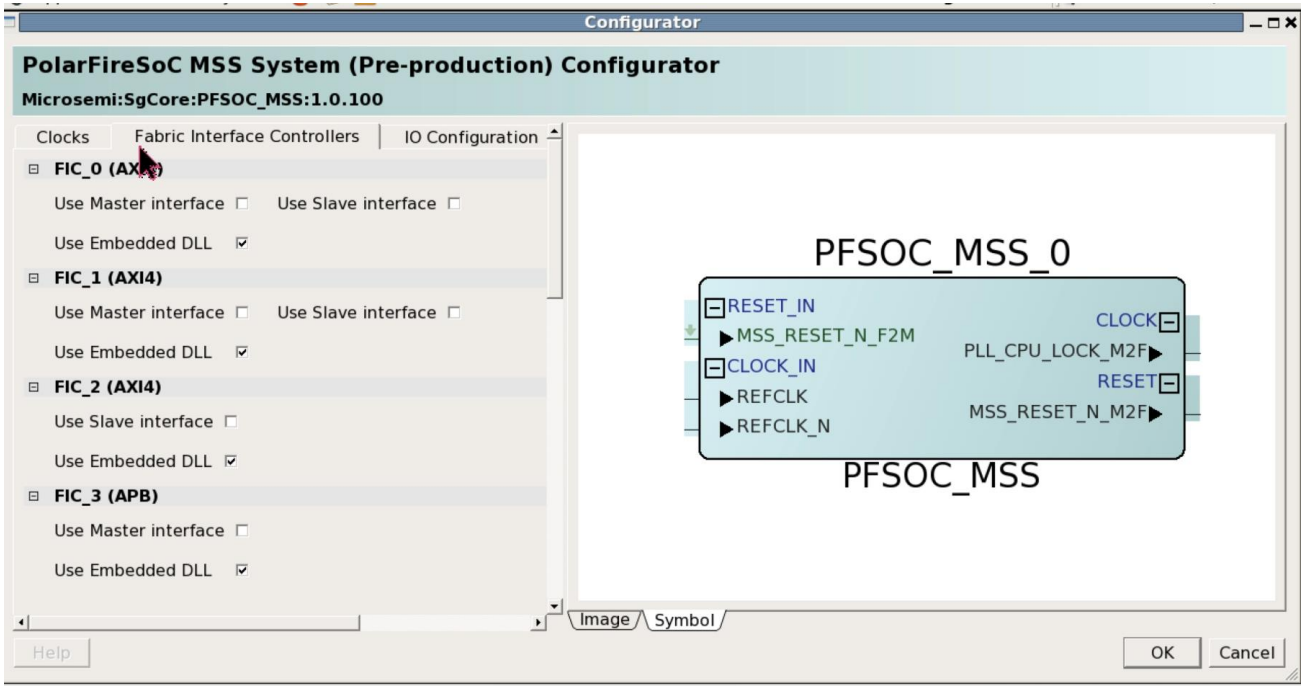
Fabric Interface Controllers:

FIC 0 AXI4
- Master
- Slave

FIC 1 AXI4
- Master
- Slave

FIC 2 AXI4
- Slave

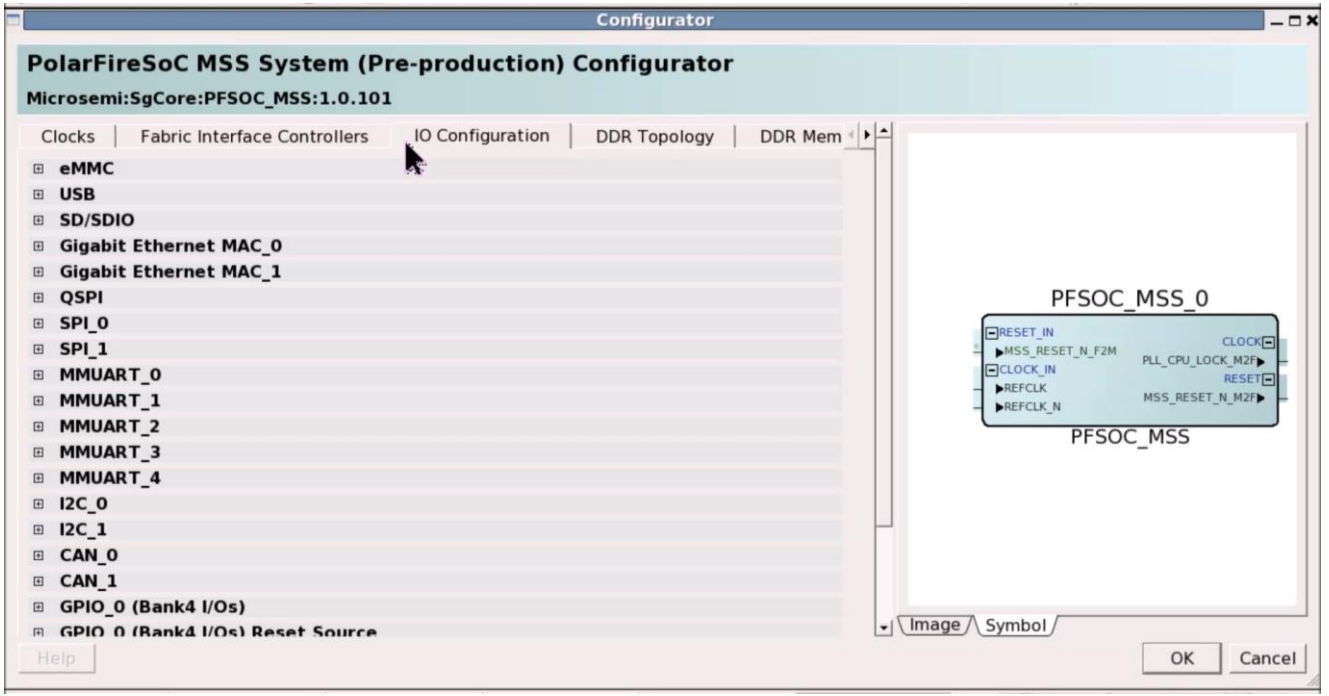
FIC 3 APB
- Master



Getting Started with Libero SoC v12.3

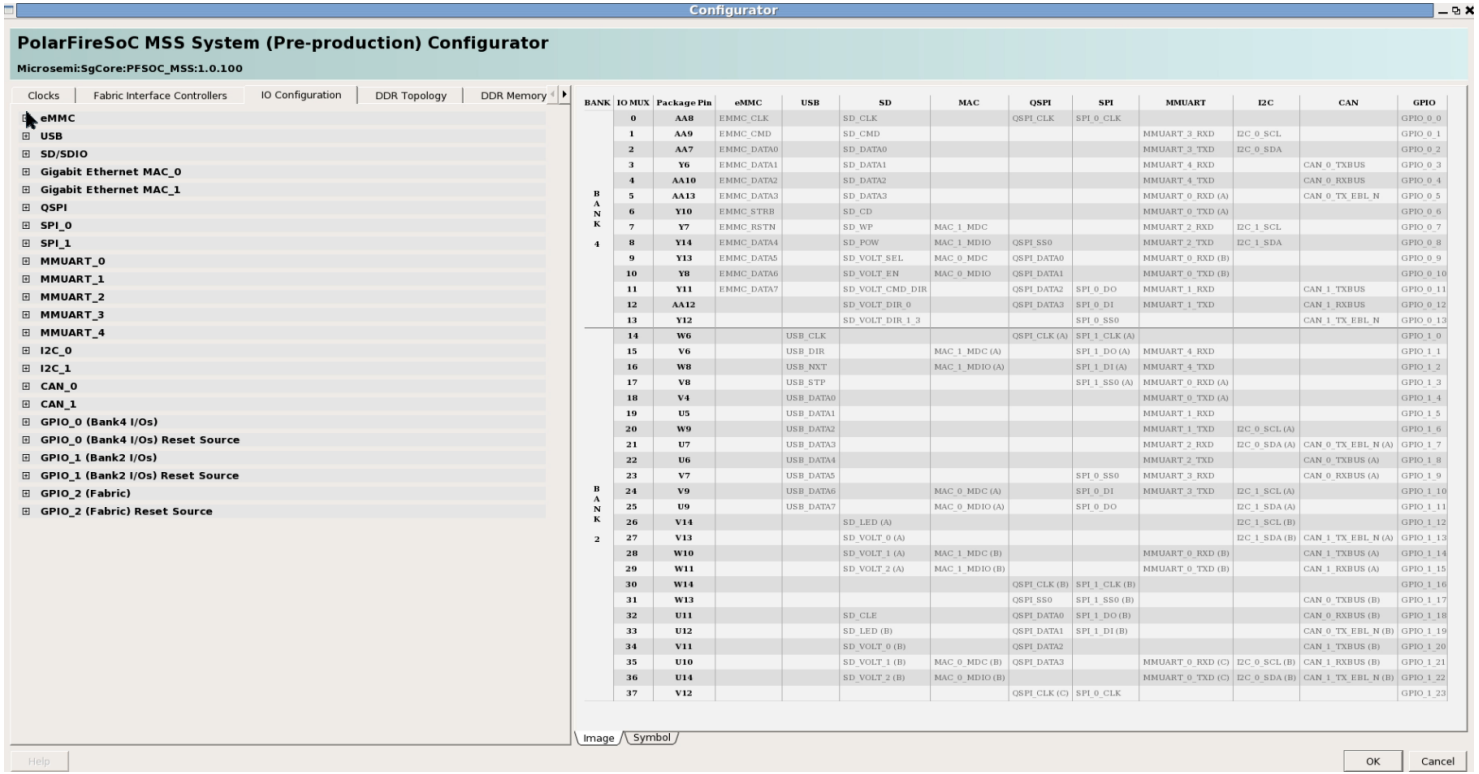
IO Configurations Available:

- eMMC
- USB
- SD/SDIO
- GEM0 / 1
- QSPI
- SPI_0 / 1
- MMUART_0 / 1 / 2 / 3 / 4
- I2C_0 / 1
- CAN_0 / 1
- GPIO_0 / 1 / 2

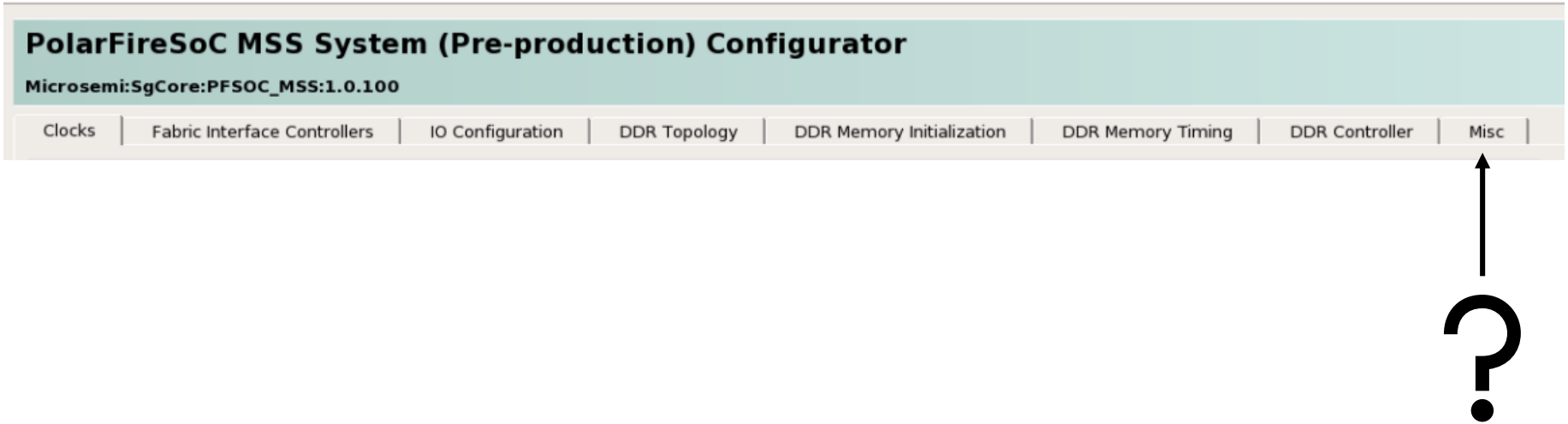


Getting Started with Libero SoC v12.3

The “Image” tab highlights IOs in use and their configurations



Getting Started with Libero SoC v12.3



Getting Started with Libero SoC v12.3

Debug_Trace:

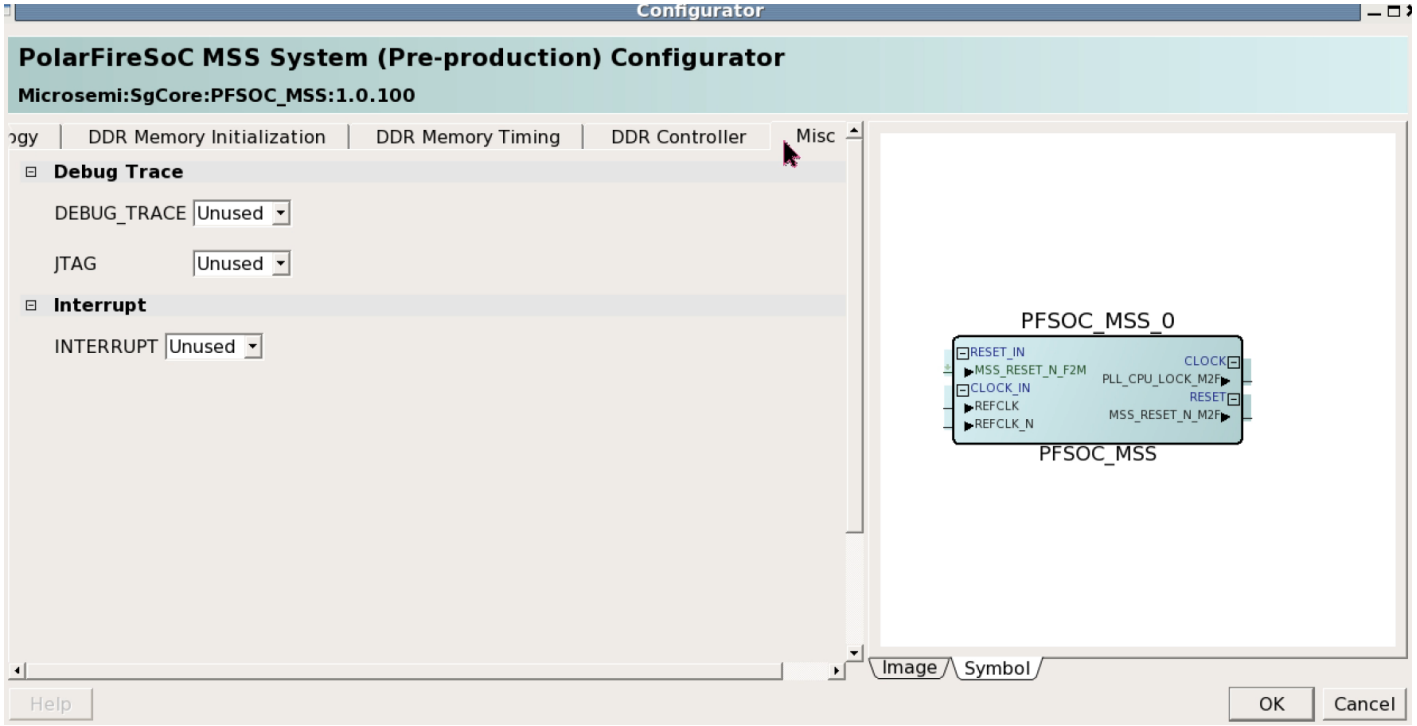
Expose UltraSoC Debug pins to the fabric

JTAG:

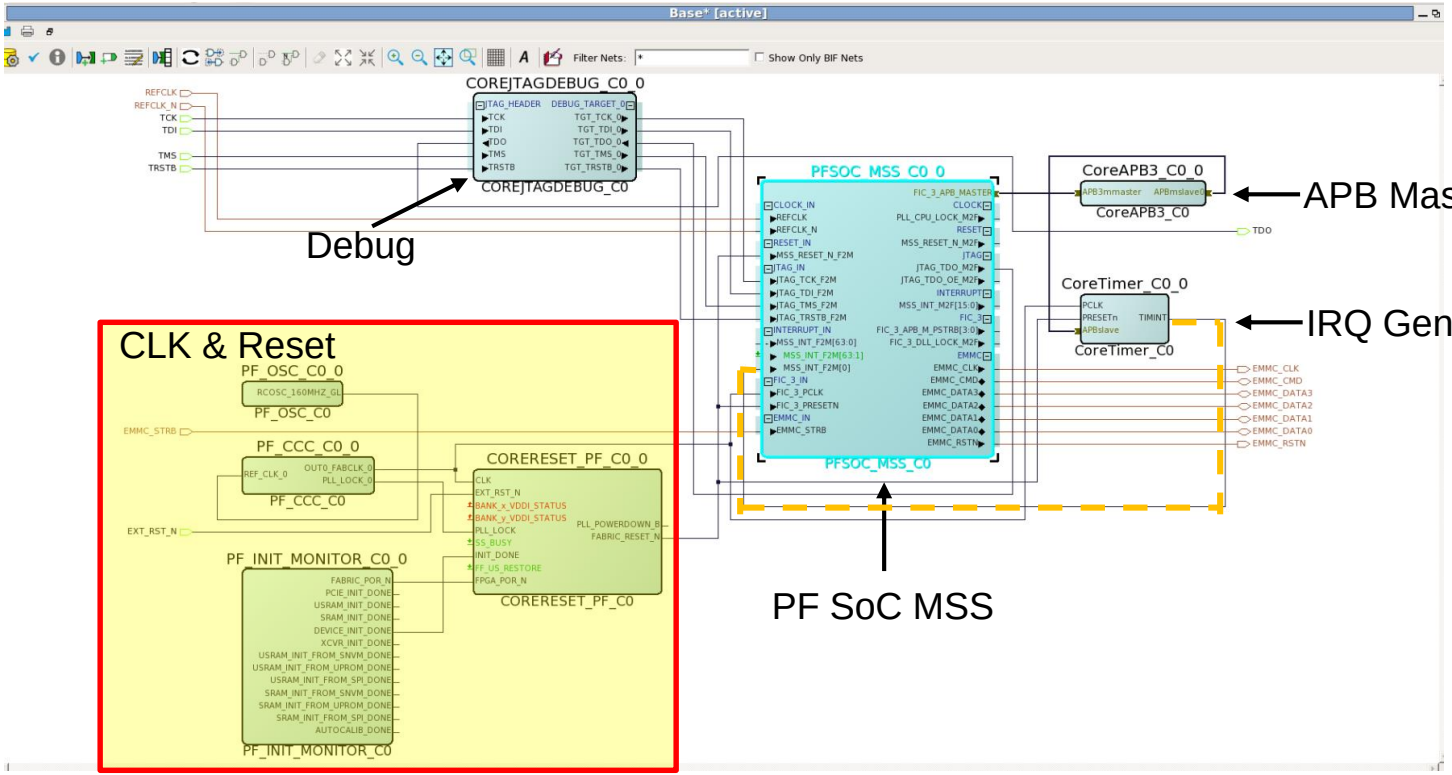
Expose fabric JTAG debug pins

Interrupt:

Expose 64 interrupt pins to the fabric



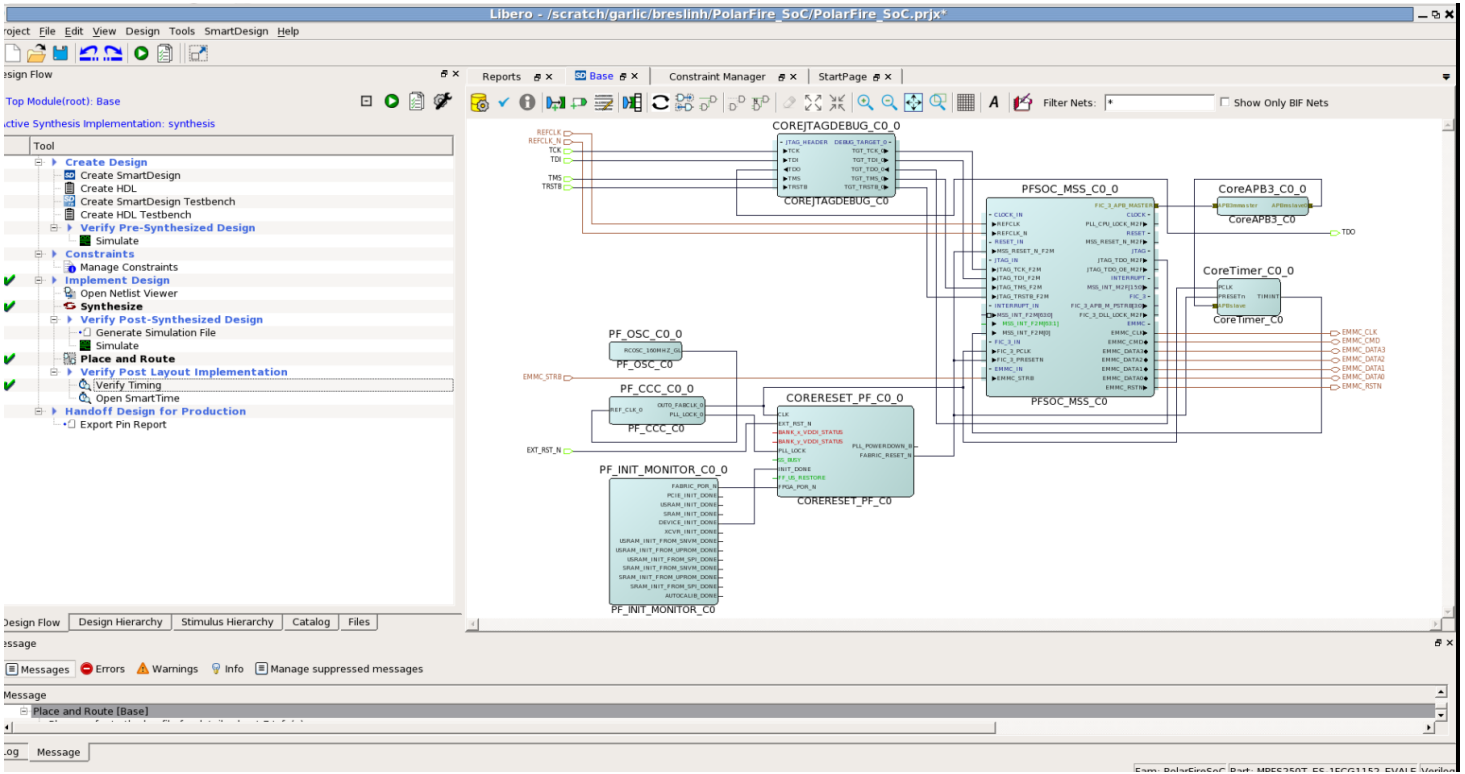
Getting Started with Libero SoC v12.3



Getting Started with Libero SoC v12.3

Currently Available:

- Synthesis
- Place and Route
- Timing Verification

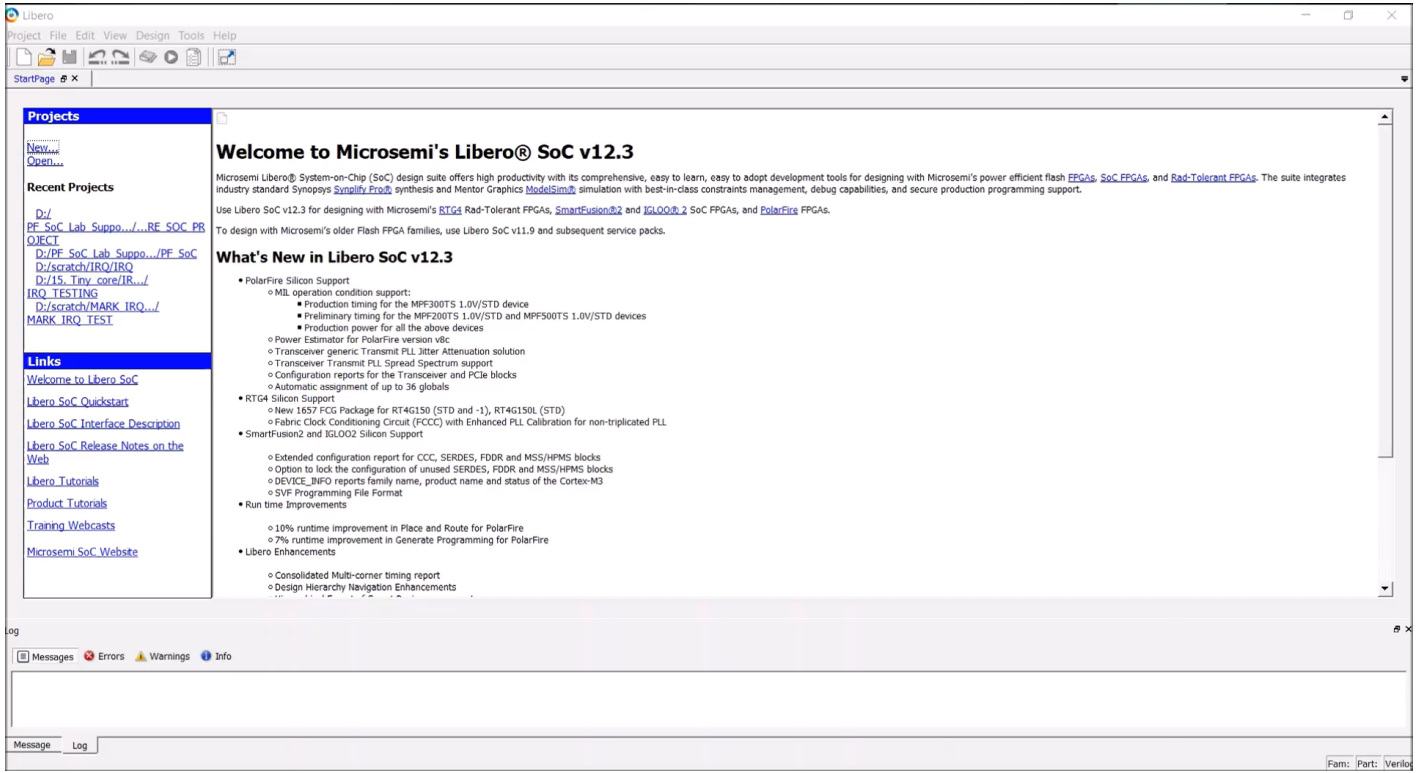


Creating a PolarFire SoC Design in Libero SoC v12.3

Creating a PolarFire SoC Design in Libero SoC v12.3

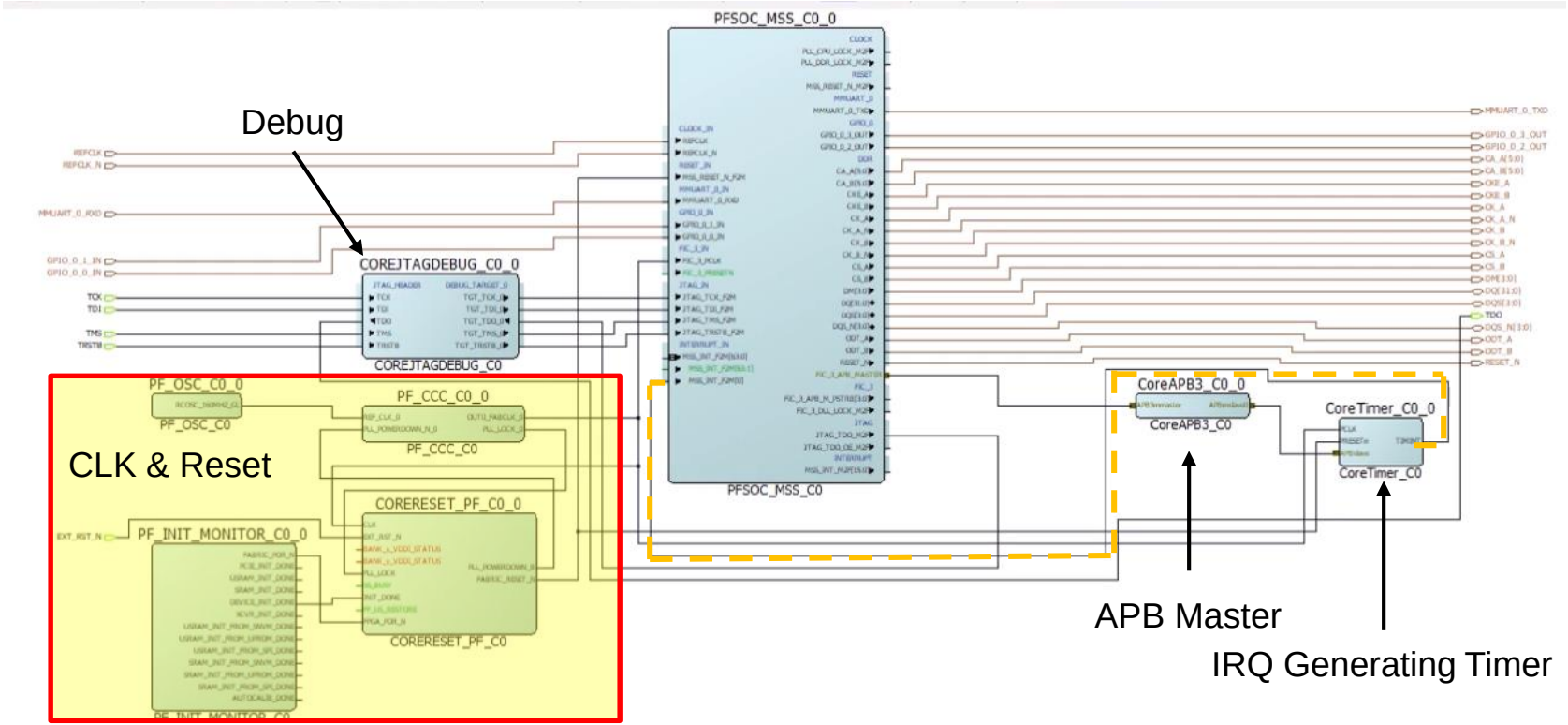
- Create the Project
- Configure the MSS
- Configure Fabric Clock and Reset
- Add Debug
- Add an Interrupt Generating Timer

Creating a PolarFire SoC Design in Libero SoC v12.3



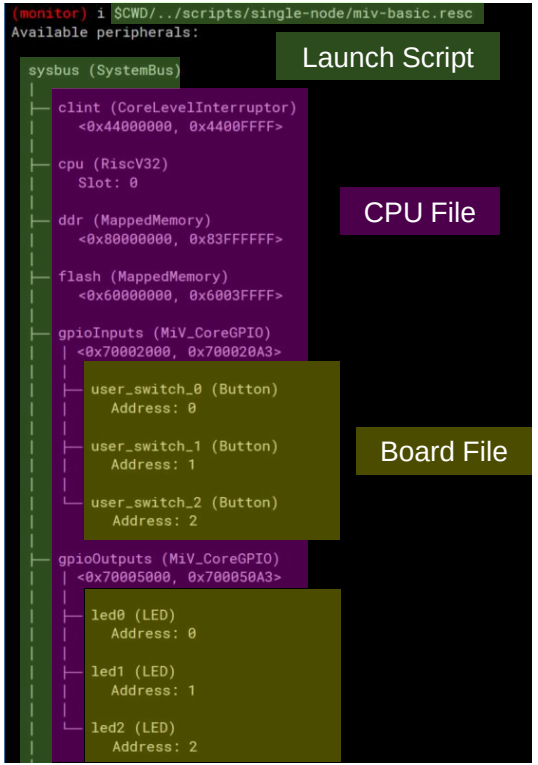
Modifying the Renode Model and MPFS Blinky

Modifying the Renode Model and MPFS Blinky



Modifying the Renode Model and MPFS Blinky

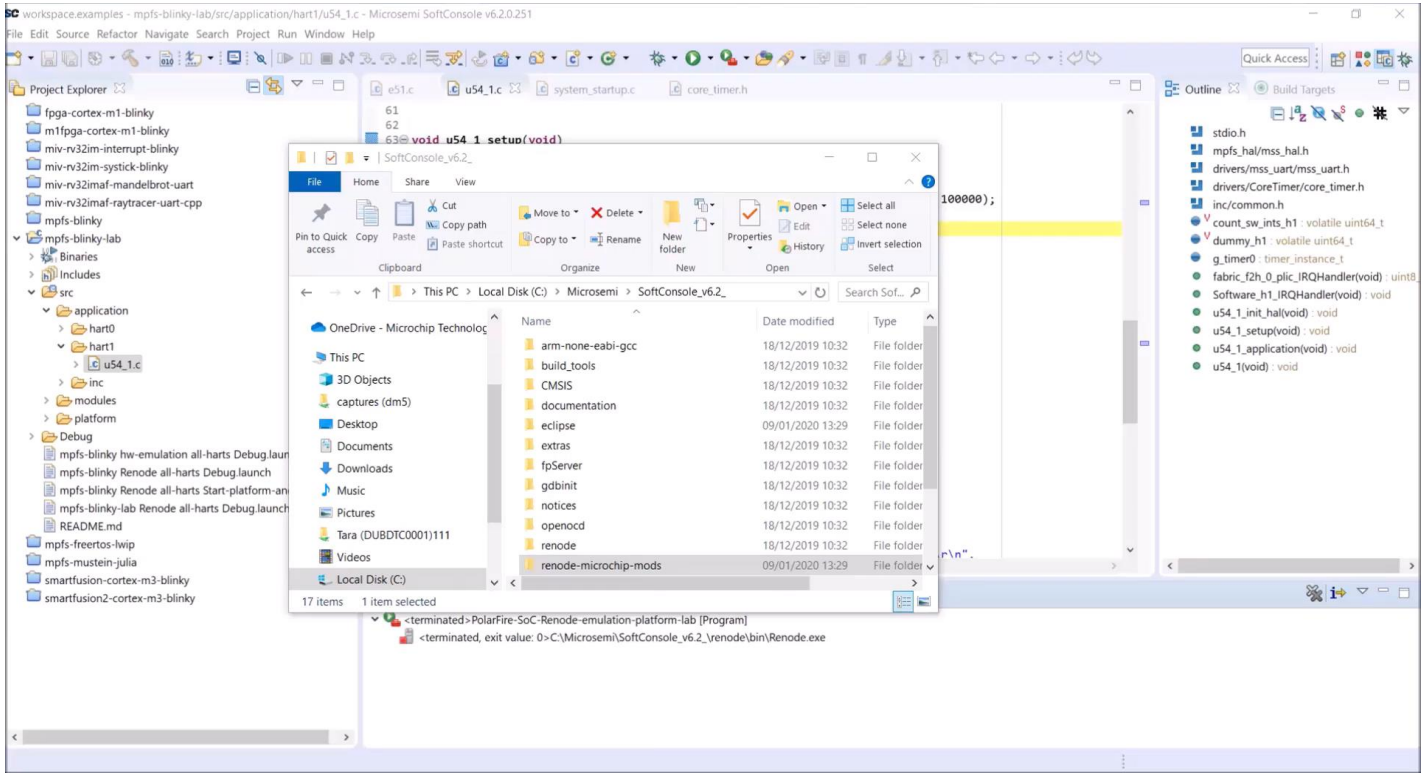
- The timer needs to be added to the CPU file
- It connects to sysbus directly – there is no need for an apb master
- The FIC3 address is 0x40_0000_0000
- The timer interrupt needs to be connected to the fabric interrupts



Modifying the Renode Model and MPFS Blinky

- Drivers for the timer need to be added to the software project
- The timer needs to be configured and started
- The handler for the external interrupt to be used needs to be added to the software

Modifying the Renode Model and MPFS Blinky



Agenda

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- Creating a PolarFire SoC Design in Libero SoC v12.3
- Modifying the Renode Model and MPFS Blinky

Thank You

Any Questions?