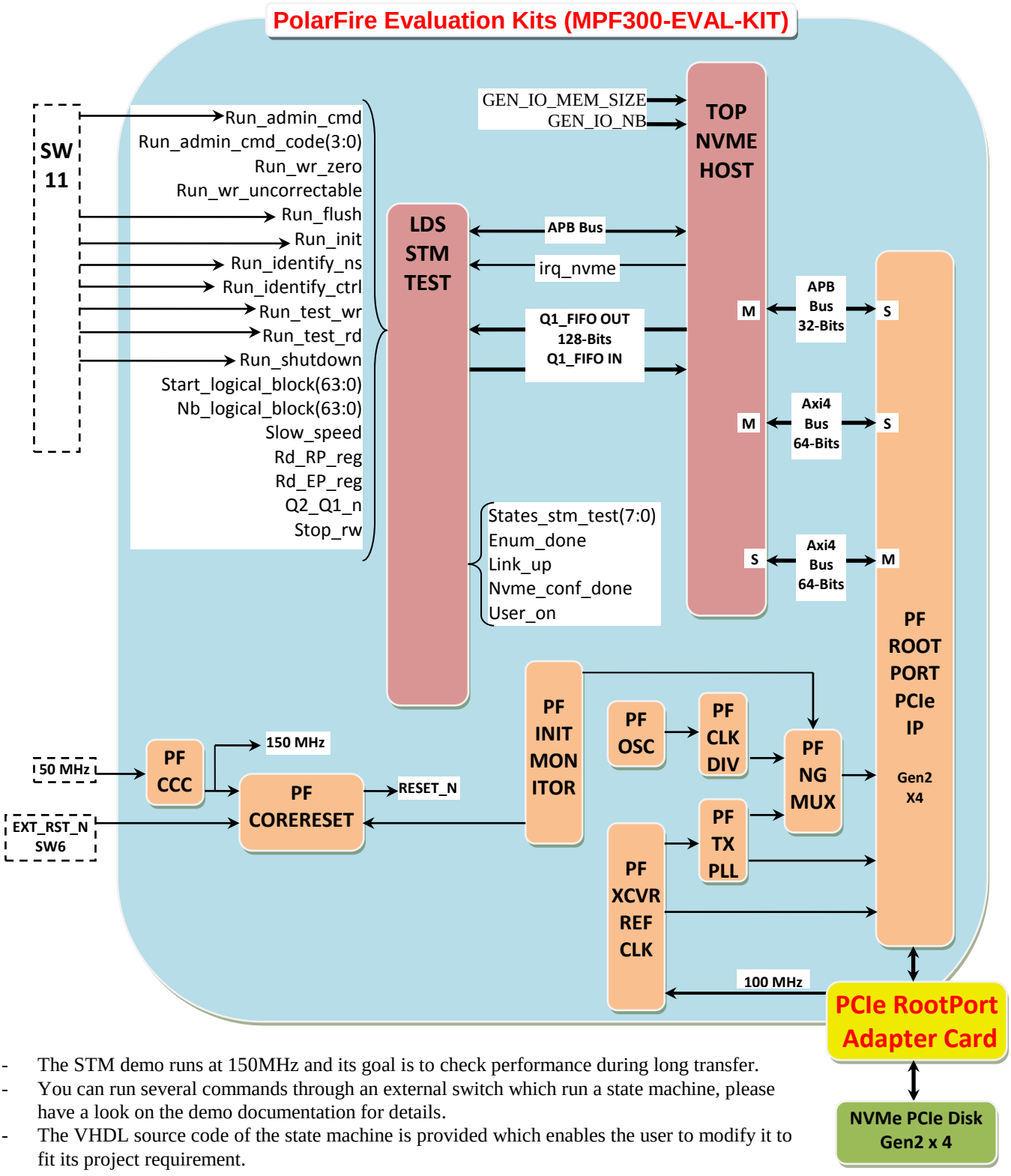
Product Brief
Jun. 19 – Ver. 1.0

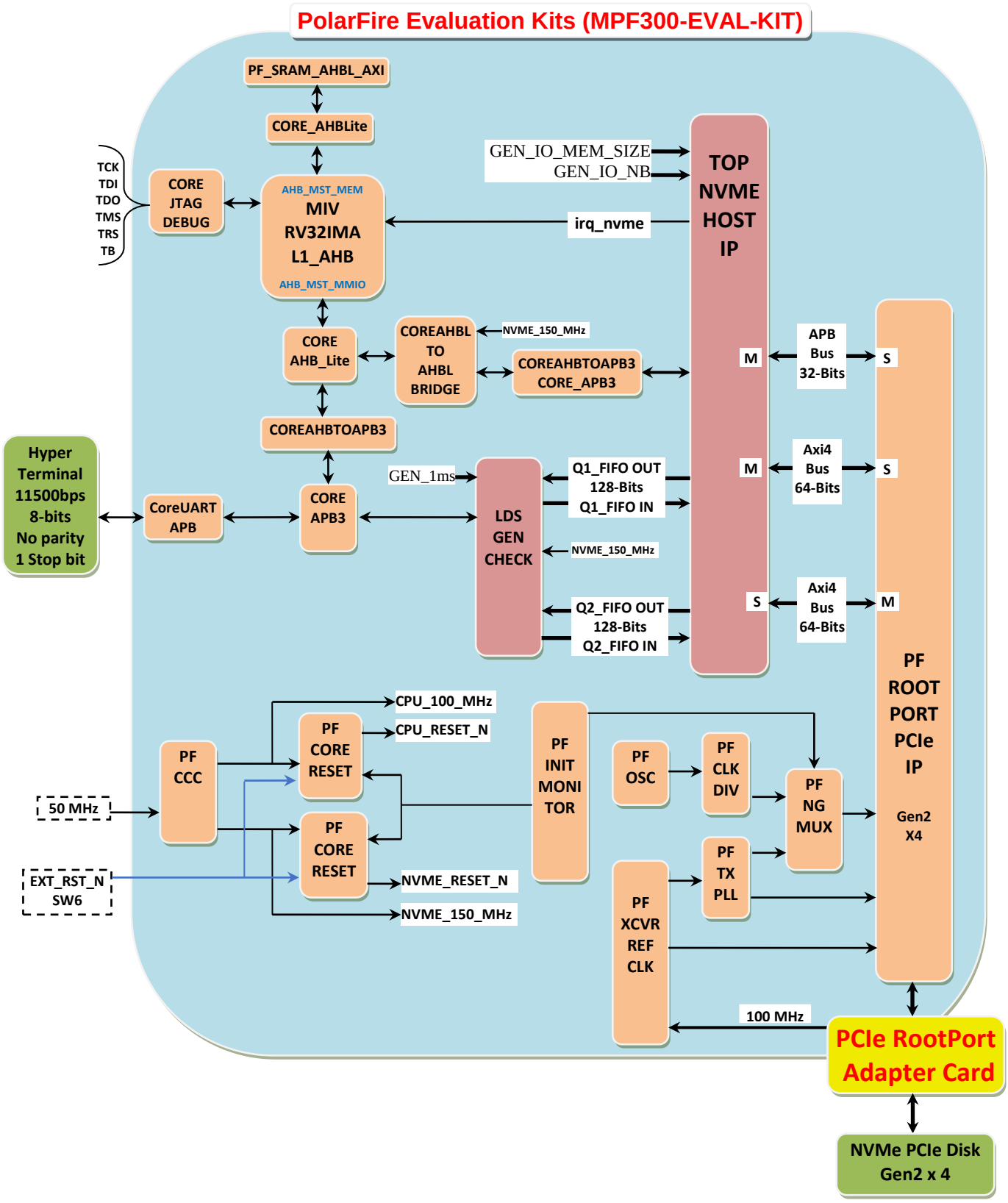
POLARFIRE
NVMe Host Recorder IP

State Machine Demo provided under NDA



- The STM demo runs at 150MHz and its goal is to check performance during long transfer.
- You can run several commands through an external switch which run a state machine, please have a look on the demo documentation for details.
- The VHDL source code of the state machine is provided which enables the user to modify it to fit its project requirement.

CPU Demo provided under NDA



- The RISC-V CPU runs at 100MHz and the NVMe data runs at 150MHz. The goal of the demo is to check performance during long transfer.
- You can run a write and read performance test through a User Interface on the Hyper Terminal, please have a look on the demo documentation for details.
- The C source code is provided which enables the user to modify it to fit its project requirement.

Features

The LDS NVME HOST RECORDER IP has been done for beginners and expert in NVMe to drive NVMe PCIe SSD.

The register file interface simplify the management of the IP for CPU interface or for State Machine interface using APB bus:

- PCIe RP and EP register configuration is done automatically.
- NVMe register configuration is done automatically.
- Able to manage 8 Name Spaces.
- Able to manage until 16 IO Queue to fit specific user requirement.
  - Each IO Queue is independent.
- Able to manage 512Bytes or 4096Bytes sector size.
- Able to run nearly all Admin command in parallel of IO Queue.
- Many IO command already pre-defined to ease use of the IP.
- Configurable IO Queue buffer size to fit user memory requirement in case of small density FPGA: 32KB, 64KB, 128KB or 256KB.
- Able to read all PCIe RP and EP registers.
- Easy connection to embedded Root Port PCIe IP through AXI bus.

When using a PCIe RP IP configured in Gen2 the PCIe frequency is at 125MHz.
When using a PCIe RP IP configured in Gen3 the PCIe frequency is at 250MHz.

The source code format is available for ease of customization. The customization can be done by Logic Design Solutions and **DO254** documentation is available on request.
This IP can be customized according to specific needs (application-specific requirement). Any other pre-designed functions can be integrated into the FPGA. FPGA density and I/O requirements can be defined according to customer specification.

Verification

The LDS NVME HOST RECORDER IP has been validated on the PolarFire Evaluation Kits (MPF300-EVAL_KIT) + MicroChip PCIe Root Adapter Card and several disks. List of disk available on request.

Performance

The demo provided makes a Disk Write and Read performance test on each disk connected.
A counter value is written on the disk and then read back and checked.
The performance depends on disk tested and memory configuration of the IP, especially for read performance.
As an example:

- Clock frequency: 150 MHz
- PCIe Gen2 x 4 HHHL disk
- 100 Giga Byte data transfer
- Sequential Write : 1060 MBytes/s
- Sequential Read : 1055 MBytes/s

Design Package

Device Family	**MICROCHIP PolarFire FPGA** **speed grade : 1**
Package file	**Source code or Source Encrypted.** Data Sheet, IP Interface Description and Constraint File.
Design Tool Used	MICROCHIP LIBERO SoC V12.0.
Support	Support provided by Logic Design Solutions 1 year e-mail and telephone support from Logic Design Solutions included in the IP price. Support does not cover User IP modifications. Maintenance Contract available.

Utilization

IP core only					
IP Configuration	**4LUT**	**USRAM 1K**	**FF**	**LSRAM 18K**	**Logic Element**
1 Queue – 32KBytes Buffer	12000	317	7550	20	12500
1 Queue – 64KBytes Buffer	12500	317	8020	33	13000
1 Queue – 128KBytes Buffer	13900	317	9400	71	14370
1 Queue – 256KBytes Buffer	16220	317	11700	135	16750
2 Queues – 32KBytes Buffer	15274	367	9900	33	15960
2 Queues – 64KBytes Buffer	16140	367	10840	59	16820
2 Queues – 128KBytes Buffer	19070	367	13600	135	19752
2 Queues – 256KBytes Buffer	23630	367	18220	263	24361

Until 16 Queues available.

Ordering Information

To purchase or make further inquiries about this, or any other Logic Design Solutions products and services, contact Logic Design Solutions in France.
Logic Design Solutions also offers IP integration and design services on FPGA.
Logic Design Solutions IPs are purchased under a License Agreement, copies of which are available on request.
Logic Design Solutions reserves the right to make changes to these specifications at any time, without notice.

Available Support Products

Support products available from Logic Design Solutions.

Related Information

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