PD69104B1

Datasheet

4-Port PoE Manager

September 2019

Microsemi

a Microchip company

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Revision 3.0 was published in September 2019. The following is a summary of the changes in revision 3.0 of this document.

- Document is revised to reflect only the PD69104B1. Consult Microchip for PD69104B1F documentation.
- Changed package marking of figure PD69104B1 Pin Configuration and Pinout (see page 21).
- Features section was updated. For more information, see Product Overview (see page 3) section.
- UART Communication Functional Description (see page 12) section was updated.
- Ordering Information (see page 36) section was updated.

1.2 Revision 2.0

Revision 2.0 was published in March 2018. The following is a summary of the changes in revision 2.0 of this document.

- The ordering information table was updated. For more information about the ordering information, see Ordering Information (see page 36).
- Mode of operation was modified. for more information, see Mode of Operation (see page 8).
- LED information in 4 pair pin modes were updated. For more information, see Table 4 (see page 15) .

1.3 Revision 1.5

Revision 1.5 was published in November 2015. The following is a summary of the changes in revision 1.5 of this document.

- The 4 pair mode pin was updated. For more information, see Table 4 (see page 15).
- The serial EEPROM load mechanism section was updated. For more information, see Serial EEPROM Load Mechanism (see page 30).

1.4 Revision 1.4

Revision 1.4 was published in July 2015. In revision 1.4 of this document, the typical application section was updated. For more information, see Typical Application (see page 4).

1.5 Revision 1.3

Revision 1.3 was published in November 2013. The following is a summary of changes in revision 1.3 of this document.

- The current set signal was updated. For more information, see Table 4 (see page 15).
- The LED description in 4 pair mode information was updated. For more information, see Table 4 (see page 15).

1.6 Revision 1.2

Revision 1.2 was published in June 2013. In revision 1.2 of this document, general updates were added.

1.7 Revision 1.1

Revision 1.1 was published in March 2013. In revision 1.1 of this document, full-temperature range P/N information was added.

1.8 Revision 1.0

Revision 1.0 was published in December 2012. It was the first publication of this document.

2 Product Overview

Microsemi's PD69104B1 Power over Ethernet (PoE) Manager enables network devices to share power and data over a single cable. PD69104B1 PoE-Manager chip is employed by both Ethernet switches and midspans. The device integrates power, analog circuitry, and state-of-the-art control logic into a single 48-pin plastic quad flat no-leads (QFN) package.

PD69104B1 device is a four-port, mixed-signal, high-voltage PoE Manager. PD69104B1 supports the following modes of operation.

- MSCC extended auto mode—A stand-alone mode in which the PD69104B1 detects IEEE 802.3AF-2003 compliant powered devices (PDs) and IEEE 802.3AT-2009 high-power devices, ensuring safe power feeding and disconnection of ports based on a power management algorithm while employing a minimum of external components.
- Semi auto mode—Allows the host to control which devices are powered and which are not, as well as communicate with PD69104B1 and configuring it.

PD69104B1 executes all real time functions as specified in IEEE 802.3AF-2003 (AF) and IEEE 802.3AT high power (AT) standards. This includes load detection, AF and AT classifications. In addition, the PD69104B1 device features Multiple Classification Attempts (MCA) port status monitoring.

PD69104B1 supports detection of legacy/pre-standard PD devices. It also provides PD real-time protection through the following mechanisms: overload, under-load, over-voltage, over-temperature, and short-circuit. PD69104B1 supports supply voltages between 44 V and 57 V, with no need for additional power supply sources, and has built-in thermal protection.

PD69104B1 is a low-power device that uses internal MOSFETs and external 0.36 Ω sense resistors.

PD69104B1 is available in a 48 lead, 8 mm × 8 mm QFN package.

2.1 Features

- Supports IEEE 802.3AF and IEEE 802.3AT, including two-event classifications
- MSCC extended auto and semi auto
- Supports pre-standard PD detection
- Supports Cisco device detection
- Single DC voltage input (44 V to 57 V)
- Wide temperature range: –10 °C to 85 °C
- Low-power dissipation (0.36 Ω sense resistor)
- Drives independent 4/2-pairs power port
- Supports Extended PoE Protocol and Register Map
- Includes two selectable communication modes (I^2C and UART). Consult your Microsemi representative before beginning a design based on UART.
- Includes reset command pin integrated with an RPD/MRPD mechanism
- Continuously monitoring port and system data
- Parameter setting using input pins
- Parameters setting from external serial EEPROM device
- Built-in dynamic power management and emergency power management mechanisms with 3 x power supply power-good pins
- Power soft start mechanism
- On-chip thermal protection

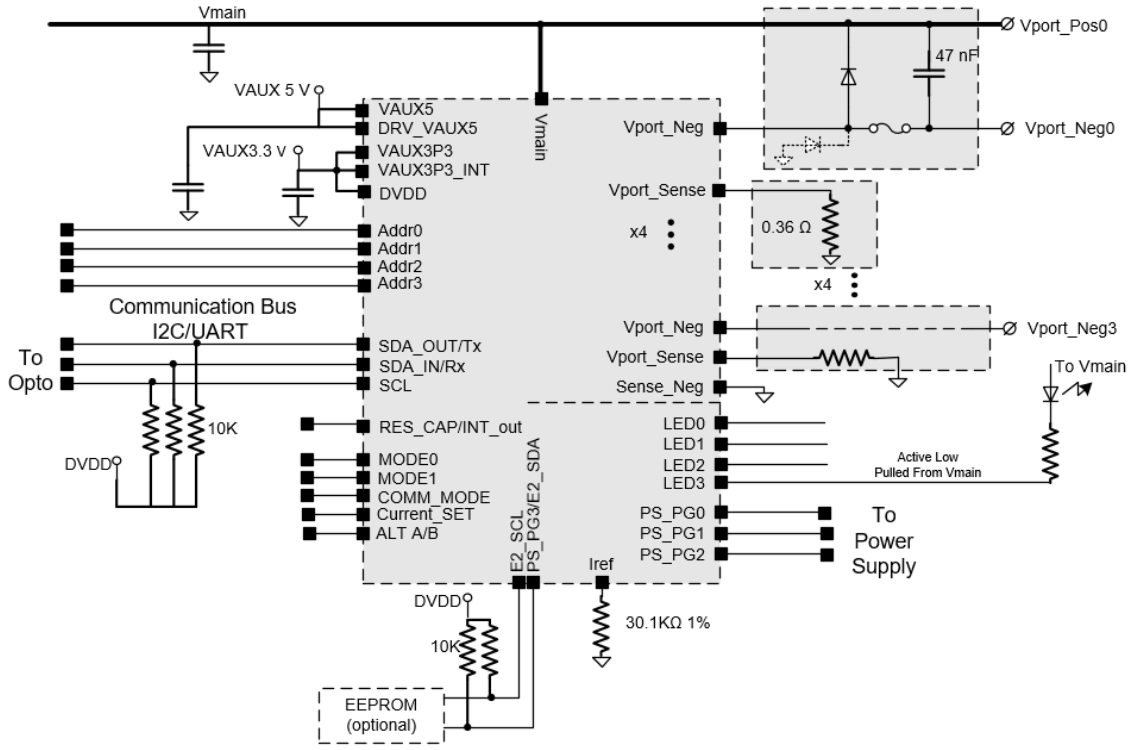
- On-chip continual thermal monitoring
- Voltage/current and temperature monitoring/protection
- Built-in 3.3 V and 5 V regulators
- Internal power on reset
- MSL 3
- RoHS compliant

2.2 Typical Application

The following figure shows a typical application with a simple plug and play PoE solution for a single Ethernet port, switch, or hub.

Plug the positive (POS) and negative (NEG) signals into the RJ45 switch jack.

Figure 1 • Typical Application



Note: Fuses per port are not required for use in circuits with total power level of up to 3 kW, as the PD69104B1 designed to fulfill limited power source (LPS) requirements per the latest editions of IEC60950-1 and EN60950-1.

For more information on detailed schematics of application and layout recommendations, contact your local Microsemi account representative.

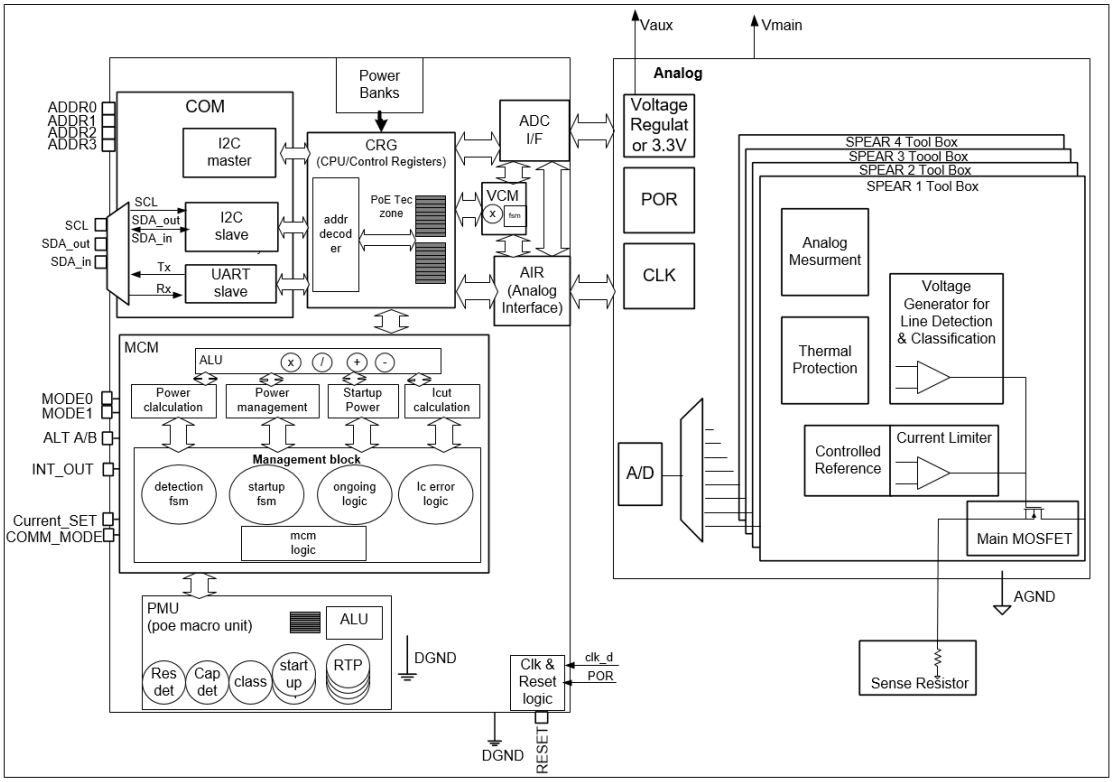
3 Functional Descriptions

The following sections describe the functions of the PD69104B1 device.

3.1 Internal Block Diagram

The following illustration shows the internal block diagram for the PD69104B1 device.

Figure 2 • Internal Block Diagram



3.2 Logic Main Control Module

The logic main control block includes the digital timing mechanisms and the state machines, synchronizing and activating the following PoE functions.

- Real-time protection (RTP)
- Start-up macro (DVDT)
- Load-signature detection (RES DET)
- Classification macro (CLASS)
- Voltage and current monitoring registers (VMC)
- ADC interfacing
- Direct digital signals with analog block

3.3 Line Detection Generator

Upon request from the main control module, the line detection generator creates four different voltage levels. Thus, it ensures robust AF/AT line detection functionality.

3.4 Classification Generator

Upon request from the main control module, the state machine applies regulated class event and mark event voltages to the ports, as required by the IEEE standard.

3.5 Current Limiter

This circuit continuously monitors the current of the powered ports and limits it to a specific value, according to predefined limits set using the Current_Set pin. In case the current exceeds this specific level, the system starts measuring the elapsed time. If this period is longer than the preset threshold, the port is disconnected.

3.6 Main MOSFET

Main power switching FET is used for controlling the PoE current that streams into the load.

3.7 IC and Port Parameters Monitoring

A 10-bit analog-to-digital converter is used for converting analog signals into digital registers.

- IC main voltage monitoring—The chip main voltage is sampled every 1 mS. Each measurement is an average of four consecutive ADC measurements and stored in the relevant register. The main voltage measurement resolution is 5.835 mV/count ±5 %.
- IC thermal monitoring—The PD69104B1 contains a thermal sensor that is sampled to register every 1 mS so the PD69104B1 die temperature can be monitored at all time.
- Port current/voltage monitoring—After the ports start to deliver the power the current/voltage is sampled every 1 mS on each port. Each measurement is an average of four consecutive ADC measurements and stored in the relevant register. Current measurement resolution is 122.07 µA/count ±5% and voltage measurement resolution is 5.835 mV/count ±5 % (see the PD69104B1 User Guide register map document for more details).

3.8 Power-on Reset (PoR)

This element monitors the internal 3.3 V_{DC} levels. If this voltage drops below specific thresholds, a reset signal is generated and the PD69104B1 is reset.

3.9 Voltage Regulator

The voltage regulator generates 3.3 V_{DC} and 5 V_{DC} for the internal circuitry. These voltages are derived from the V_{main} supply.

3.10 Clock (CLK)

This is an internal 8 MHz CLK oscillator.

3.11 I²C Address Selection

The following table lists the I²C address selection for the PD69104B1 device.

Table 1 • I2C Address Selection

CONST Bits	ADDR3 Slave 1 Bit	ADDR2 Slave 0 Bit	ADDR1 ID1 Bit	ADDR0 ID0 Bit	I²C/UART Address
0 1 0	0	0	0	0	0100000b
0 1 0	0	0	0	1	0100001b
0 1 0	0	0	1	0	0100010b
0 1 0	0	0	1	1	0100011b
0 1 0	0	1	0	0	0100100b
0 1 0	0	1	0	1	0100101b
0 1 0	0	1	1	0	0100110b
0 1 0	0	1	1	1	0100111b
0 1 0	1	0	0	0	0101000b
0 1 0	1	0	0	1	0101001b
0 1 0	1	0	1	0	0101010b
0 1 0	1	0	1	1	0101011b
0 1 0	1	1	0	0	0101100b
0 1 0	1	1	0	1	0101101b
0 1 0	1	1	1	0	0101110b
0 1 0	1	1	1	1	0101111b

Address 0000000b is the global address in extended mode operation I²C (MODE<1:0>='00').

Address 0110000b is the global address in semi-auto mode operations (MODE<1:0>='01' or '11').

All the slaves respond to the global address.

Avoid global read transactions.

Address 0001100b is used for extended PoE address (alert response address) in semi-auto mode operations.

When reading from this alert response address, only slaves that assert the Int_out pin will send bytes that consist of their own addresses.

3.12 Mode of Operation

The following table lists the modes of operation for the PD69104B1 device.

Table 2 • Mode of Operation

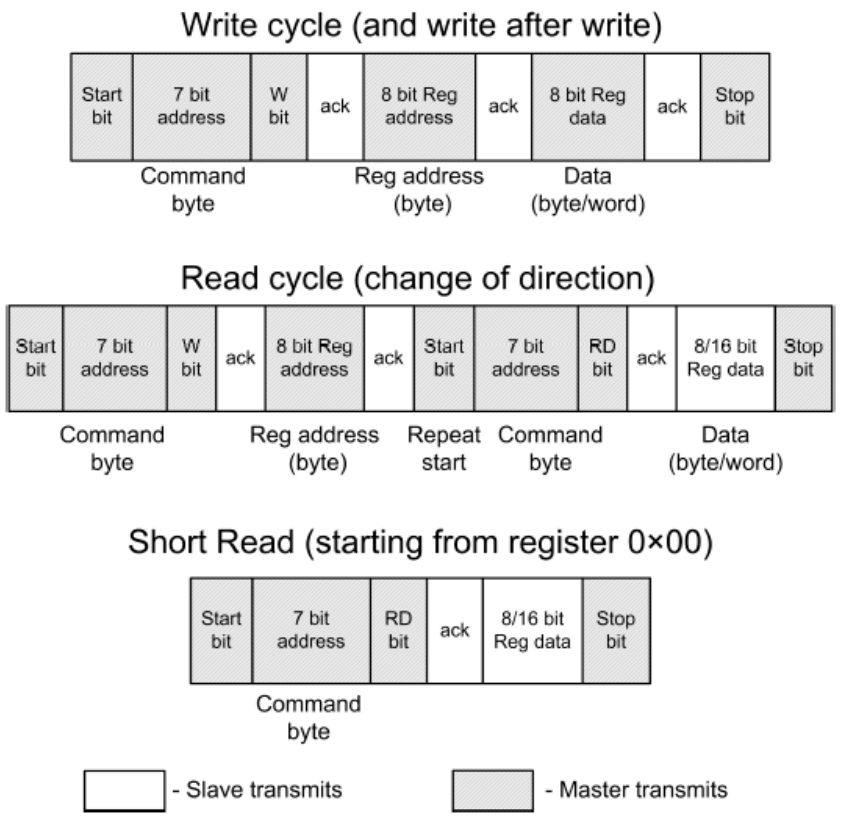
Mode 1	Mode 0	Mode	Comm to the IC	Functionality
0	0	MSCC extended auto mode	I²C or UART (see COMM_MODE pin)	Fully autonomous operation without a need for Host Controller (MCU). This mode supports extended registers map. Default operation—with no interrupt function (interrupt can be enabled by communication command).
0	1	Semi-auto mode	I²C or UART (see COMM_MODE pin)	Host should manage the ports.

Note: Consult Microchip before beginning a design based on UART.

3.13 I²C Communication Functional Description

The following figure shows the I²C communication format of the data write/read access for the PD69104B1 device.

Figure 3 • Packet Structure



3.13.1 Address Phase

This phase is common to both read and write accesses.

- Both accesses (read and write) begin with a START indication.
- The address of the slave is following the START indication. In case of a miss match, the slave ignores the rest of the access and waits for the 'STOP' indication to close the current access. However, in case the slave address matches, the next bit indicates the type of the access (read or write).
- The matched slave acknowledges the first byte.
- The following byte is the internal register address. The slave should acknowledge the byte.

3.13.2 Data Phase

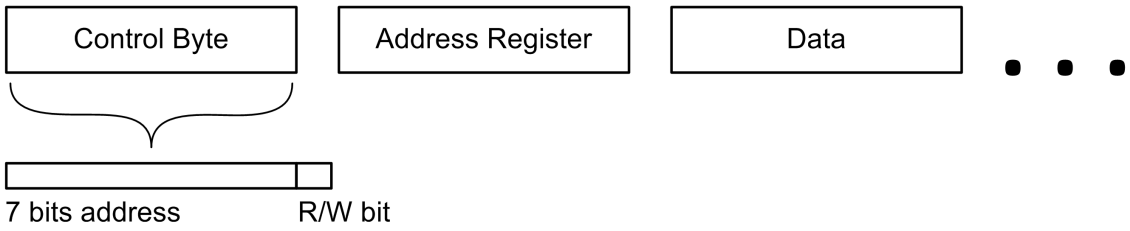
In this phase, the read and write accesses behave differently.

- Write access
  - Byte of write data is transmitted to the slave; the slave acknowledges it.
  - A stop indication from the master closes the current access.
- Read access
  - Another command byte is received, comprised of the slave address and the real command type (in this case, read). The slave acknowledges the byte.
  - At this stage, the master is ready to continue the communication and to sample the read data; hence, the read data must be ready on the next rise of the clock pulse.
  - A byte of data is transmitted to the master; the master acknowledges it.

3.14 I²C High-Level Layer

The following figure shows the supported I²C high-level packet structure.

Figure 4 • High-Level Packet Structure



3.14.1 Byte/Word Read/Write Transaction

- The first byte is the control byte that consists of the chip address and a read/write operation indication.
- The second byte is the internal chip's address register.
- The following bytes/words are data bytes. For a read operation, they are read from the slave, and for a a write operation, they are written to the slave.

3.14.2 Successive Read/Write Transaction

- The master can continue sending bytes that the slaves write, or continue receiving data from a slave during the address phase.
- The slave will continue to send/receive data bytes from/to the master until a 'stop bit' is asserted by the master.

- Each byte received by the slave (or each byte to be read from the registers) is received from the next register address (each byte address is increased by 1).

3.14.3 Read Byte Transaction

The slave supports a 'send byte' transaction.

1. The master begins with a start bit. The following byte consists of the chip address and a read bit.
2. If the chip address is correct, the slave acknowledges the byte and immediately (at the next sck phase) sends a data byte from a constant address (addr 7'h00).
3. A send byte transaction continues with successive read transactions (address 1, address 2, and so on) until the master asserts a stop bit.

3.14.4 Broadcast Support

All slaves answer a general address sent by the master. For semi-auto modes, the general address is 7'h30, and for of MSCC Extended Auto mode, the general address is 7'h0.

The broadcast is for master writing only; read access is ignored in a broadcast transaction.

3.14.5 Timeout Mechanism

The I²C has an internal counter of 14 ms. The counter resets each time the SCL rises or falls. If the SCL is “stuck” for 14 ms, the I²C returns to IDLE state and transaction is ignored (the timeout mechanism is active between the start bit and the stop bit).

3.14.6 I²C Timing Constraints

The following table lists the characteristics of the SDA and SCL bus lines for F/A-mode I²C-bus.

Table 3 • Characteristics of the SDA and SCL Bus Lines for F/A-Mode I2C-Bus

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	4.0		0.6		µs
LOW period of the SCL clock	t_{LOW}	4.7		1.3		µs
HIGH period of the SCL clock	t_{HIGH}	4.0		0.6		µs
Set-up time for a repeated START condition	$t_{SU;STA}$	4.7		0.6		µs
Data hold time: for CBUS compatible masters for I²C-bus devices	$t_{HD;DAT}$	5.0 0[1]	3.45[2]	0[1]	0.9[2]	µs
Data set-up time	$t_{SU;STA}$	250		100[3]		ns
Rise time of both SDA and SCL signals	t_r		1000	20 + 0.1C_b[4]	300	ns
Fall time of both SDA and SCL signals	t_f		300	20 + 0.1C_b[4]	300	ns
Set-up time for STOP condition	$t_{SU;STO}$	4.0		0.6		µs
Bus free time between a STOP and START condition	t_{BUF}	4.7		1.3		µs
Capacitive load for each bus line	C_b		400		400	pF

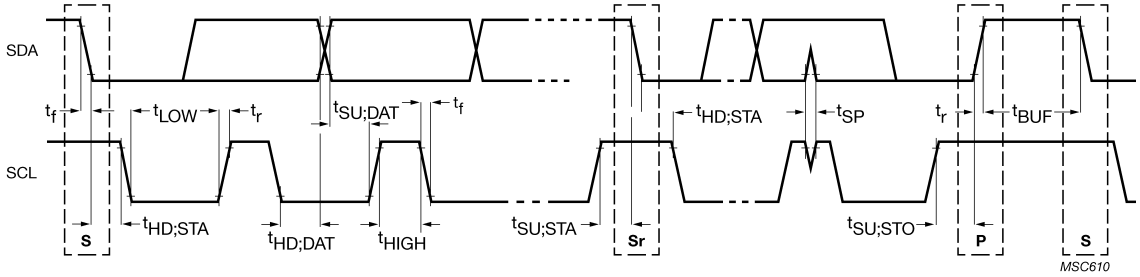
Parameter	Symbol	Standard Mode	Fast Mode	Unit
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nL}	0.1 V_{DD}	0.1 V_{DD}	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nH}	0.2 V_{DD}	0.2 V_{DD}	V

1. A device must internally provide a hold time of at least 300 ns for the SDA signal (refers to the VIHmin of the SCL signal) to bridge the undefined region of the falling edge of the SCL.
2. The maximum tHD;DAT has to be met only if the device does not stretch the LOW period (tLOW) of the SCL signal.
3. A fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement tSU; DAT ³ 250 ns must then be met. This is in case the device does not stretch the LOW period of the SCL signal.
4. If the device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line tr max + tSU;DAT = 1000 ns + 250 ns = 1250 ns (according to the Standard-mode I²C-bus specification) before the SCL line can be released.

Note: All values refer to V_{IHmin} and V_{ILmax} levels. For more information, see Electrical Characteristics (see page 15) section.

The following figure shows the definition of timing for F/S-mode devices on the I²C-bus.

Figure 5 • Definition of Timing for F/S-mode Devices on the I2C-bus



3.15 UART Communication Functional Description

The UART is supported by the PD69104B1 platform to allow communication between PD69104B1 IC's and an external host. The PD69104B1 platform supports UART only as a slave. The following is a list of features for the UART communication mode. Consult your Microsemi representative before beginning a design on the UART interface.

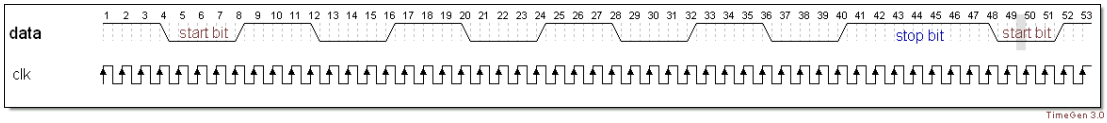
- Slave mode
- Supports 4,800 to 115,200 Baud rate, auto-learning mechanism
- Supports 8-bit address
- Supports 8-bit data access
- Supports general broadcast transmission
- 8N1
  - 8-bits data
  - No parity
  - 1 stop bit
- Frame transaction—header, payload, and suffix
- Timeout mechanism (timeout for frame and per byte)
- No successive read/write—one transaction per register (read/write)
- Half-duplex implementation—Rx starts after Tx ends
- A filter for glitches cancelling on the RX pin

3.15.1 The Physical Layer

The UART protocol has two data lines; the Rx, from where PD69104B1 receives its data, and the Tx, where data is transmitted. UART is a byte protocol in which every byte starts with a start bit and ends with a stop bit.

The following figure shows the UART read/write frame.

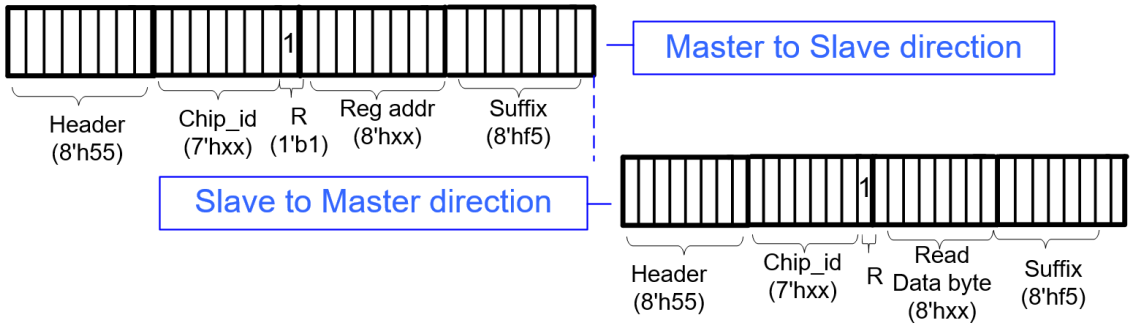
Figure 6 • UART Read/Write Frame



The data is sent in a constant frame in order to be synchronized.

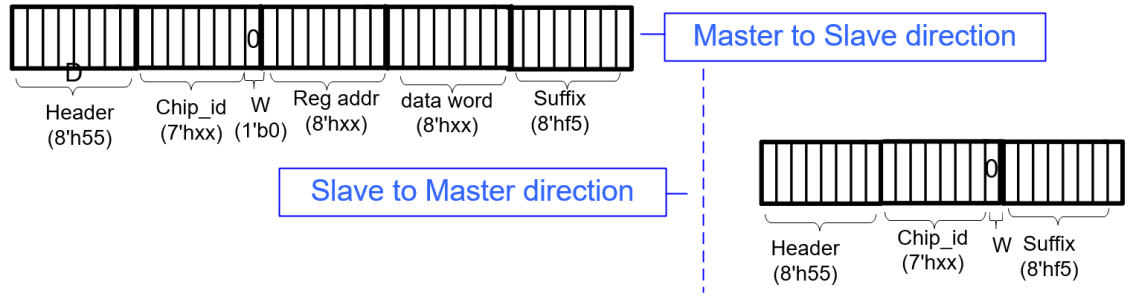
The following figure shows the master's read packet structure.

Figure 7 • Master's Read Packet Structure



The following figure shows the master's write packet structure.

Figure 8 • Master's Write Packet Structure



3.15.2 Broadcast Support

All slaves answer a general address sent by the master. The general address is 7'h0.

Broadcast is for master writing only—read accesses are ignored in a broadcast transaction.

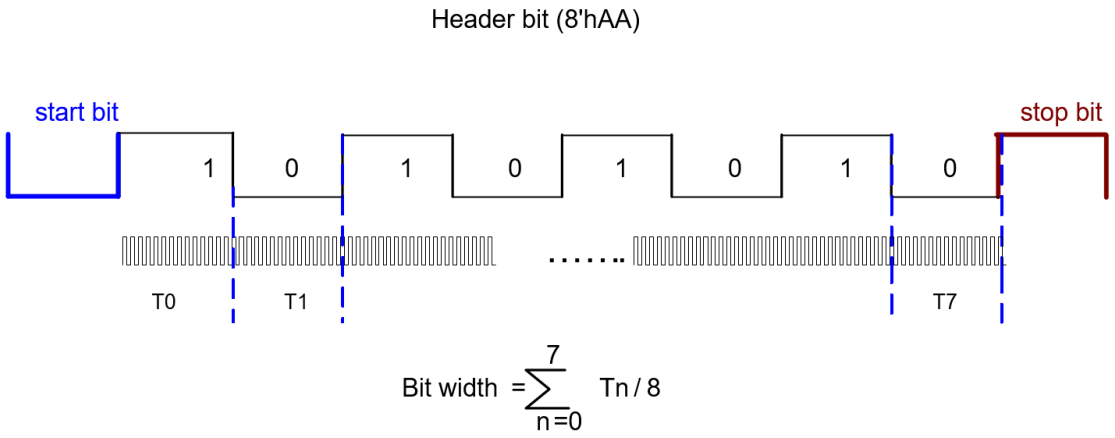
3.15.3 Auto Baud Rate Learning

PD69104B1 has a self-learning baud rate mechanism that allows synchronizing all PD69104B1 slaves to the master's "real" baud rate and thus working with a higher baud rate.

The first byte received by the slave is 8'hAA. At the rising or falling edge of each bit, an 8 MHz counter starts counting the bit width (in a 125 ns resolution). The average width of the 8 header bits is the actual bits rate. By using this mechanism, PD69104B1 slaves can be synchronized with the master and set back data at that rate. The header is a preamble bit that facilitates synchronization.

The following figure shows the header bit width.

Figure 9 • Header Bit Width



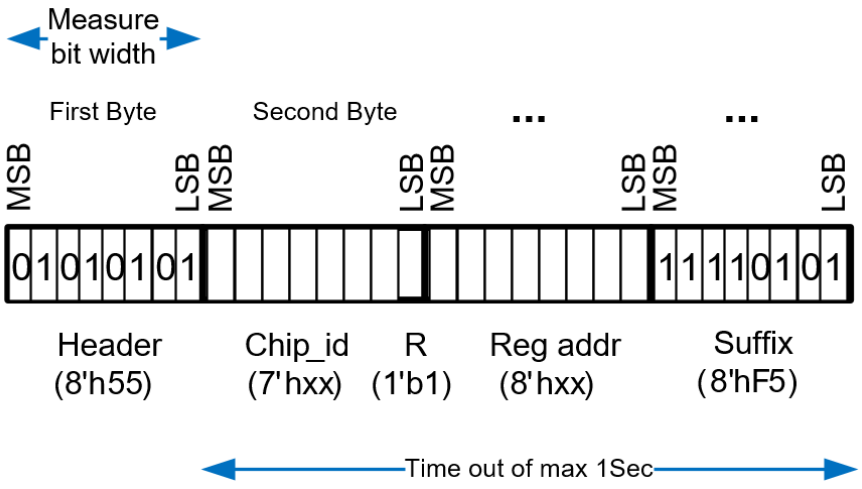
3.15.4 Timeout Mechanisms

The UART protocol has a frame timeout mechanism. This mechanism has the following two purposes.

- Distinguishing between the frame's suffix of 8'f5 and a payload byte with the same value. The mechanism identifies a frame suffix only when it arrives as 2 bytes in a read access or as 4-bytes in a write access; otherwise it is treated as a data byte.
- Preventing UART communication from getting stuck. A 1-second timeout counter is activated beginning with a start frame (the end of header byte) till a suffix arrival. If a suffix byte does not arrive within that time the transaction is ignored and the slave moves into an IDLE state.

The following figure shows the timeout mechanism.

Figure 10 • Timeout Mechanism



4 Electrical Specifications

The following sections describe the electrical specifications of the PD69104B1 device.

4.1 Electrical Characteristics

The following minimum and maximum ratings apply over the entire specified operating ratings of the device, unless otherwise specified under conditions.

The following table lists the power supply for the PD69104B1 device.

Table 4 • Power Supply

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
V_{MAIN}	Input voltage	Supports full IEEE 802.3 functionality	44	55	57	V_{DC}
I_{MAIN}	Power supply current at operating mode	V_{MAIN}= 55 V		10		mA
V_{AUX5}	5 V output voltage		4.5	5	5.5	V_{DC}
V_{AUX3P3}	3.3 V output voltage		2.97	3.3	3.63	V_{DC}
	3.3 V output current	Without external NPN			5	mA
		With external NPN transistor on V_{AUX5}			30	mA
	3.3 V input voltage	REG_EN_N pin= 3.3 V (internal reg. is disabled) V_{AUX3P3_INT} pin=5 V	3	3.3	3.6	V_{DC}

The following table lists the PoR for the PD69104B1 device.

Table 5 • PoR

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
	Threshold		2.575	2.775	2.975	V_{DC}
	Hysteresis		0.2	0.25	0.3	V_{DC}
	Delay		10	50	100	µS

The following table lists the digital I/O for the PD69104B1 device.

Table 6 • Digital I/O

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
V_{IH}	Input logic high threshold		2			V_{DC}
V_{IL}	Input logic low threshold				0.8	V_{DC}
	Input hysteresis voltage		0.4	0.6	0.8	V_{DC}
I_{IH}	Input high current		–10		10	µA
I_{IL}	Input low current		–10		10	µA

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
V_{OH}	Output high voltage	For I_{OH} = –1 mA	2.4			V_{DC}
V_{OL}	Output low voltage	I_{OH} = 1 mA			0.4	V_{DC}

The following table lists the PoE load currents for the PD69104B1 device.

Table 7 • PoE Load Currents

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
AT_LIM_LOW	AT limit mode	Tested with sense resistance= 0.366 Ω (R_{sense} + traces= 0.36 Ω + 6 mΩ= 0.366 Ω) connected at port_sense pin	706	722	767	mA
			847	874	919	mA
			537		1200	mA
AT_LIM_HIGH	AF limit mode		410	425	448	mA
AT configurable	PoE tech high-power port		808	850	892	mA

The following table lists the main power switching FET for the PD69104B1 device.

Table 8 • Main Power Switching FET

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
R_{dson}	On resistance			0.3		Ω
	Internal thermal protection threshold			200		°C

The following table lists the line detection for the PD69104B1 device.

Table 9 • Line Detection

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
	Range	According to IEEE 802.3 standard	19		26.5	KΩ

The following table lists the classification for the PD69104B1 device.

Table 10 • Classification

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
	Class event output voltage	Measured between V_{MAIN} and V_{PORT_NEG} pins	16.5	18	19.5	V_{DC}
	Mark event output voltage	Measured between V_{MAIN} and V_{PORT_NEG} pins	7.5	8.5	9.5	V_{DC}

The following table lists the LED 0 to 3, MAX_LED drivers for the PD69104B1 device.

Table 11 • LED 0 to 3, MAX_LED Drivers

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
I_{sink} (from V_{MAIN} to AGND)	Current sink	Measured between V_{MAIN} and V_{PORT_NEG} pins		3	5	mA

The following table lists the three states analog input pins (current set, comm_mode) for the PD69104B1 device.

Table 12 • Three States Analog Input Pins (Current Set, Comm_Mode)

Symbol	Parameter	Test Conditions/Comment	Min	Typ	Max	Units
	High-level input voltage		80% V_{AUX3P3}			V_{DC}
	Open	Not connected	40% V_{AUX3P3}		60% V_{AUX3P3}	V_{DC}
	Low-level input voltage				20% V_{AUX3P3}	V_{DC}

4.1.1 Typical Power Dissipation Information

The following table lists the typical power dissipation information for the PD69104B1 device.

Table 13 • Typical Power Dissipation Information

Typical Power Dissipation Information
R_{sense} Power Dissipation: 0.36 Ω × I_{port}^2
R_{ds_ON} Power Dissipation: 0.3 Ω × I_{port}^2
P_{port_AF} = 15.4 W ==> Port Power Dissipation at R_{sense}= 37 mW (320 mA)
Port Power Dissipation at R_{ds_ON} = 31 mW (320 mA)
P_{port_AT} = 30 W ==> Port Power Dissipation at R_{sense}= 130 mW (600 mA)
Port Power Dissipation at R_{ds_ON} = 108 mW (600 mA)
Using Internal 3.3 V regulator
Typical PD69104B1 self power dissipation (including internal regulations) = 0.5 W (50 V)
Typical PD69104B1 at 4 × Port AF application power dissipation = 0.5 W + 4 x 31 mW + 4 × 37 mW = 0.77 W
Typical PD69104B1 at 4 × Port AT application power dissipation = 0.5 W + 4 x 108 mW + 4 × 130 mW = 1.45 W
Using External 3.3 V regulator
Typical PD69104B1 self power dissipation (external 3.3 V source) = 0.25 W (50 V)
Typical PD69104B1 at 4 × Port AF application power dissipation = 0.25 W + 4 x 31 mW + 4 × 37 mW = 0.52 W
Typical PD69104B1 at 4 × Port AT application power dissipation = 0.25 W + 4 x 108 mW + 4 × 130 mW = 1.2 W

4.2 Dynamic Characteristics

PD69104B1 utilizes three current level thresholds (I_{min}, I_{cut}, I_{lim}) and three timers (T_{min}, T_{cut}, T_{lim}).

- Loads that consume I_{lim} current for more than T_{lim} are labeled as 'short circuit state' and are shutdown.
- Loads that dissipate more than I_{cut} for longer than T_{cut} are labeled as ‘overloads’ and are shutdown.
- If output power is below I_{min} for more than T_{min}, the PD is labeled as ‘no-load’ and is shutdown.

Automatic recovery from overload and no-load conditions is attempted every T_{OVLREC} period (typically 1 second). Output power is limited to I_{lim}, which is the maximum peak current allowed at the port.

The following table lists the operational mode parameters.

Table 14 • Operational Mode Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{UDLREC}	Automatic recovery from no-load shutdown	Measured from port shutdown point (can be modified through control port)		1		s
	Cutoff timers accuracy	Typical accuracy of T_{cut}		2		ms
I_{Inrsh}	Inrush current	For t= 50 ms, C_{load}= 180 µF max.	400		450	mA
I_{port}	Output current operating range	Continuous operation after startup period	10		725	mA
P_{port}	Output power available, operating range	Continuous operation after startup period at port output	0.57		36	W
I_{min1}	Off-mode current	Must disconnect where T is greater than T_{UVL}	0		5	mA
		May or may not disconnect where T is greater than T_{UVL}	5	7.5	10	mA
I_{min2}	PD power maintenance request drop-out time limit	Buffer period to handle transitions	300		400	ms
T_{PMDO}	Overload time limit		50		75	ms
T_{OVL}	Turn-on rise time	From 10% to 90% of V_{port} (specified for PD load consisting of 100 µF capacitor parallel to 200 Ω resistor)	15			µs
T_{rise}	Turn-off time	From V_{port} to 2.8 V_{DC}			500	ms
T_{off}	Time maintain power signature	DC modulation time for DC disconnect		49		ms

The following table lists the IEEE 802.3AT mode parameters.

Table 15 • IEEE 802.3AT Mode Parameters

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{UDLREC}	Automatic recovery from no-load shutdown	Measured from port shutdown point (can be modified through control port)		1		s
	Cutoff timers accuracy	Typical accuracy of T_{cut}		2		ms
I_{Inrsh}	Inrush current	For t= 50ms, C_{load}= 180µF max.	400		450	mA
I_{port}	Output current operating range	Continuous operation after startup period	10		725	mA
P_{port}	Output power available, operating range	Continuous operation after startup period at port output	0.57		36	W
I_{min1}	Off-mode current	Must disconnect where T is greater than T_{UVL}	0		5	mA
		May or may not disconnect where T is greater than T_{UVL}	5	7.5	10	mA
I_{min2}	PD power maintenance request drop-out time limit	Buffer period to handle transitions	300		400	ms
T_{PMDO}	Overload time limit		50		75	ms
T_{OVL}	Turn-on rise time	From 10% to 90% of V_{port} (Specified for PD load consisting of 100µF capacitor parallel to 200 W resistor)	15			µs
T_{rise}	Turn-off time	From V_{port} to 2.8 V_{DC}			500	ms
T_{off}	Time maintain power signature	DC modulation time for DC disconnect		49		ms

4.3 Absolute Maximum Ratings

The following table lists the absolute maximum ratings for the PD69104B1 device.

Table 16 • Absolute Maximum Ratings

Parameter	
Supply input voltage (V_{MAIN})	–0.3 V_{DC} to 74 V_{DC}
Port_Neg [0..7] pins	–0.3 V_{DC} to 74 V_{DC}
LED pins	–0.3 V_{DC} to 74 V_{DC}
Port_Sense[0..7] pins	–0.3 V_{DC} to 3.6 V_{DC}
QGND, GND pins	–0.3 V_{DC} to 0.3 V_{DC}
V_{AUX5}, DRV_VAUX5	–0.3 V_{DC} to 5.5 V_{DC}
All other pins	–0.3 V_{DC} to 3.6 V_{DC}
PD69104B1 operating ambient temperature range	–10 °C to 85 °C
Maximum operating junction temperature	160 °C
ESD protection at all I/O pins	JESD22 Class 1C HBM (±2 KV)
Storage temperature range	–65 °C to 150 °C

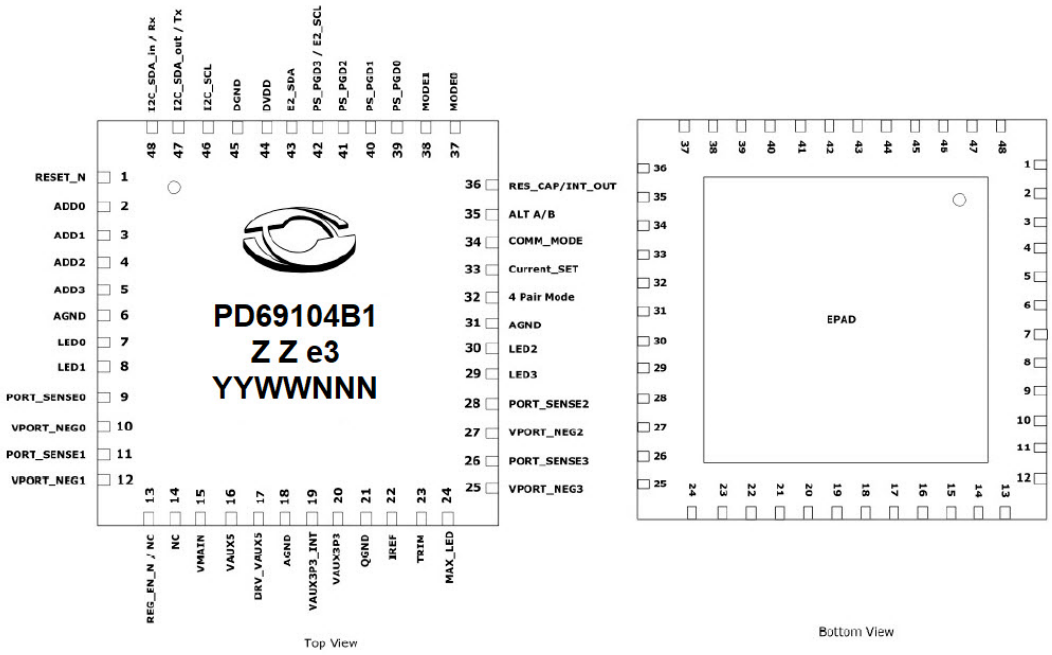
Note: Exceeding these ratings can cause damage to the device. All voltages are with respect to ground. Currents are marked positive when flowing into specified terminals and marked negative when flowing out of specified terminals.

5 Pin Descriptions

The PD69104B1 device has 48-pins, which are described in this section.

The following figure shows the top view of the PD69104B1 pin configuration and pinout.

Figure 11 • PD69104B1 Pin Configuration and Pinout



Note: RoHS/Pb-free 100 % matte tin finish. PD69104B1 for –10 °C to 85 °C operating ambient temperature range.

The following table lists the functional pin descriptions for the PD69104B1 device.

Table 17 • Pin Descriptions

Pin	Pin Name	Pin Type	Description
0	PAD	Analog GND	Exposed PAD: connect to analog ground (AGND). A decent ground plane should be deployed around this pin whenever possible (see PD69104B1 Layout Design Guidelines).
1	RESET_N[1]	Digital input	Reset input – active low ('0'= reset) This pin is also used for RPD/MRPD function.
2	ADDR0	Digital input	Address bus for setting the address of the chip. See Table 1 (see page 7) .
3	ADDR1	Digital input	Address bus for setting the address of the chip. See Table 1 (see page 7) .
4	ADDR2	Digital input	Address bus for setting the address of the chip. See Table 1 (see page 7) .
5	ADDR3	Digital input	Address bus for setting the address of the chip. See Table 1 (see page 7) .
6	AGND	Power	Analog ground

Pin	Pin Name	Pin Type	Description
7	LED 0	Open drain output	Port 0 LED indication–active low ('0' = LED on). See Table 22 (see page 32).
8	LED 1	Open drain output	Port 1 LED indication–active low ('0' = LED on). See Table 22 (see page 32).
9	PORT_SENSE0	Analog input	Sense resistor port input (connected to 0.36 Ω, 1% resistor to QGND with ~6 mΩ trace for measurements accuracy).
10	VPORT_NEG0	Analog I/O	Negative port output
11	PORT_SENSE1	Analog input	Sense resistor port input (connected to 0.36 Ω, 1% resistor to QGND with ~6 mΩ trace for measurements accuracy).
12	VPORT_NEG1	Analog I/O	Negative port output
13	REG_EN_N/NC	Analog I/O	An input pin that enables control of the 3.3 V_{DC} internal regulator. Disables internal 3.3 V_{DC} regulator in case external 3.3 V_{DC} is used to supply the chip. If connected to GND or unconnected, internal regulator is enabled. If connected to 3.3 V_{DC}, internal regulator is disabled.
14	NC	Analog I/O	A test pin used only during production. Keep unconnected.
15	VMAIN	Power	Supplies voltage for the internal analog circuitry. A 1 µF (or higher) low ESR bypass capacitor, connected to AGND, should be placed as close as possible to this pin through low resistance traces.
16	VAUX5	Power	Regulated 5 V_{DC} output voltage source, needs to be connected to a filtering capacitor of 4.7 µF or higher. If an external NPN is used to regulate the voltage, connect this pin to the emitter (the collector should be connected to V_{MAIN}).
17	DRV_VAUX5	Power	Driven outputs for 5 V_{DC} external regulations. In case internal regulation is used, connect to pin 16. In case an external NPN is used to regulate the voltage, connect this pin to the Base.
18	AGND	Power	Analog ground
19	VAUX3P3_INT	Power	In case internal 3.3 V_{DC} regulator is used, connected to V_{AUX3P3} (pin 20). In case external 3.3 V_{DC} regulator is used, connect to VAUX5 (pin 16).
20	VAUX3P3	Power	Regulated 3.3 V_{DC} output voltage source. A 4.7 µF or higher filtering capacitor should be connected between this pin and AGND. When an external 3.3 V_{DC} regulator is used, connect it to this pin to supply the chip.
21	QGND	Power	Quiet analog ground
22	IREF	Analog input	A reference resistor pin. A 30.1 kΩ, 1% resistor should be connected between this pin and QGND.
23	TRIM	Test input	Trimming input for IC production. Should be connected to V_{AUX3P3}.
24	MAX_LED	Open drain output	MAX LED analog output. Indicates the device has exceeded maximum power budget. See Table 22 (see page 32).
25	VPORT_NEG3	Analog I/O	Negative port output
26	PORT_SENSE3	Analog input	Sense resistor port input (connected to 0.36 Ω, 1% resistor to QGND with ~6 mΩ trace for measurements accuracy).
27	VPORT_NEG2	Analog I/O	Negative port output

Pin	Pin Name	Pin Type	Description
28	PORT_SENSE2	Analog input	Sense resistor port input (connected to 0.36 Ω, 1% resistor to QGND with ~6 mΩ trace for measurements accuracy).
29	LED 3	Open drain output	Port 3 LED indication–active low ('0' = LED on). See Table 22 (see page 32).
30	LED 2	Open drain output	Port 2 LED indication–active low ('0' = LED on). See Table 22 (see page 32).
31	AGND	Power	Analog ground
32	4 pairs mode	Analog input	2 state input pin. Select 4 pairs mode: • "0" (GND) - 4 ports of 2 pairs. • "1" (VCC) - 2 ports of 4 pair.
33	Current_SET	Analog input	3 state input pin, used for selecting output current and AF/AT mode: • "0" (AGND) – AF mode • "open" (N.C) – Low AT mode 600mA • "1" (V_{DD}) – High AT mode 720mA
34	COMM_MODE	Analog input	3 state input pin communication. Following options are available: • "0" (AGND) – UART active • "open" (N.C) – E2PROM connected and I^2C active if connected.In this case within 2PROM Register 0x7E (SYS_CFG) bit 5 (i2c_en) should be set to "1". • "1" (V_{DD}) – I2C active
35	ALT A/B	Digital input	User input pin, used for setting the chip working mode: • GND – ALT B mode = Midspan mode (midsp [1:4] bits ="1") • DVDD – ALT A mode = Endspan mode (midsp [1:4] bits ="0")
36	INT_OUT	Digital I/O (open drain)	In MSCC Extended Auto mode: User input pin. Used for setting the chip legacy detection mode: • "1" (V_{DD}) – IEEE802.3af compliant resistor detection only • "0" (GND) – IEEE802.3 AF/AT Detection and Legacy (non-standard) line detection In semi-auto mode: Interrupt out pin. Indicates an interruption event has occurred. An external 10K pull-up resistor should be connected between this pin and DVDD.
37	Mode0	Digital input	Used for IC operational mode selection. See Table 2 (see page 8).
38	Mode1	Digital input	Used for IC operational mode selection. See Table 2 (see page 8) .
39	PS_PGD0	Digital input	Power supply power good 0; power budget set pin – for fast power control. See Table 23 (see page 34).
40	PS_PGD1	Digital input	Power supply power good 1; power budget set pin – for fast power control. See Table 23 (see page 34).
41	PS_PGD2	Digital input	Power supply power good 2; power budget set pin – for fast power control. See Table 23 (see page 34).

Pin	Pin Name	Pin Type	Description
42	PS_PGD3 / E2_SCL	Digital I/O (open drain)	Power supply power good 3; Power budget set pin—for initial configuration (See Table 7) Or (refer to COMM MODE PIN) E2_SCL: I²C Clock Out to EEPROM When working with EPROM—an external 10K pull-up resistor should be connected between this pin and DVDD.
43	E2_SDA	Digital I/O (open drain)	EEPROM I²C data I/O pin. Used for power-up configuration in stand alone systems. An external 10K pull-up resistor should be connected between this pin and DVDD.
44	DVDD	Power	Digital 3.3 V_{DC} power input
45	DGND	Power	Digital GND
46	I2C_SCL	Digital input	I²C bus, serial clock input. An external 10K pull-up resistor should be connected between this pin and DVDD.
47	I2C_SDA_out	Digital I/O (open drain)	I²C bus, data output/UART Tx output An external 10K pull-up resistor should be connected between this pin and DVDD.
48	I2C_SDA_in	Digital I/O (open drain)	I²C bus, data input/UART Rx input An external 10K pull-up resistor should be connected between this pin and DVDD.

1. This pin should be free of large capacitance in order to prevent RPD and MRPD pulses distortion (See the MSCC PD69104B Application Note).

Note: “0”= connect to DGND and “1”= connect to DVDD.

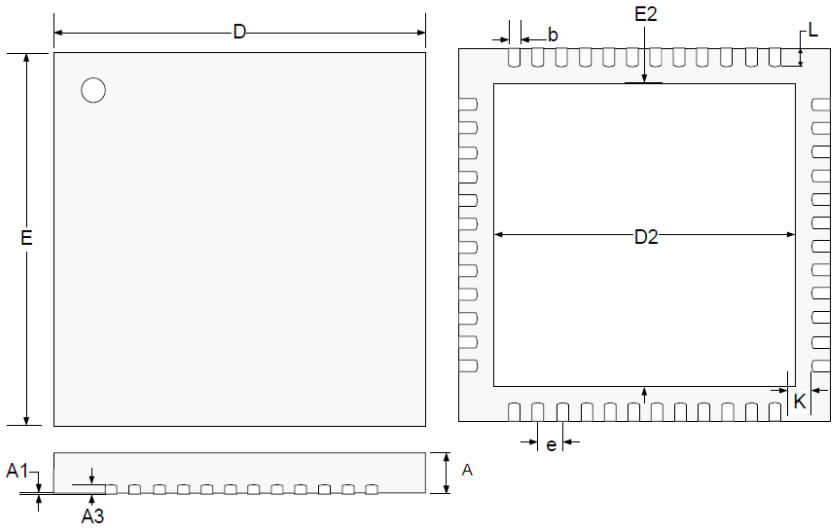
6 Package Information

The following sections describe the package information for the PD69104B1 device.

6.1 Package Outline Drawing

The following illustration shows the package outline drawing for the PD69104B1 device.

Figure 12 • Package Outline Drawing



The following table lists the dimensions and measurements of the PD69104B1 device.

Table 18 • Dimensions and Measurements

Dim	Millimeters		Inches	
	Min	Max	Min	Max
A	0.80	1.00	0.031	0.039
A1	0.00	0.05	0	0.002
A3	0.20 ref		0.008 ref	
K	0.20 min		0.008 min	
e	0.50 BSC		0.02 BSC	
L	0.30	0.50	0.012	0.02
b	0.18	0.30	0.007	0.012
D2	6.35	6.60	0.250	0.260
E2	6.35	6.60	0.250	0.260
D	8.00 BSC		0.315 BSC	
E	8.00 BSC		0.315 BSC	

Note: Dimensions do not include protrusions; these should not exceed 0.155 mm (0.006") on any side. The lead dimension shall not include solder coverage.

6.2 Thermal Specifications

Thermal resistance-junction to ambient is 25 °C/W.

Thermal resistance-junction to case is 4 °C/W.

Note: All of the above assume no ambient airflow. Junction temperature calculation: $T_J = T_A + (P_D \times \theta_{JA})$. The θ_{JA} numbers are guidelines for the thermal performance of the device/PC-board system.

6.3 RoHS and Solder Reflow Information

The following lists the recommended RoHS and solder reflow information for the PD69104B1 device.

- RoHS 6/6
- Pb-free 100 % matte tin finish
- Package peak temperature for solder reflow (40 seconds maximum exposure)—260 °C (0 ° C, –5 °C)

Note: Exceeding these ratings can cause damage to the device.

The following table lists the reflow profiles.

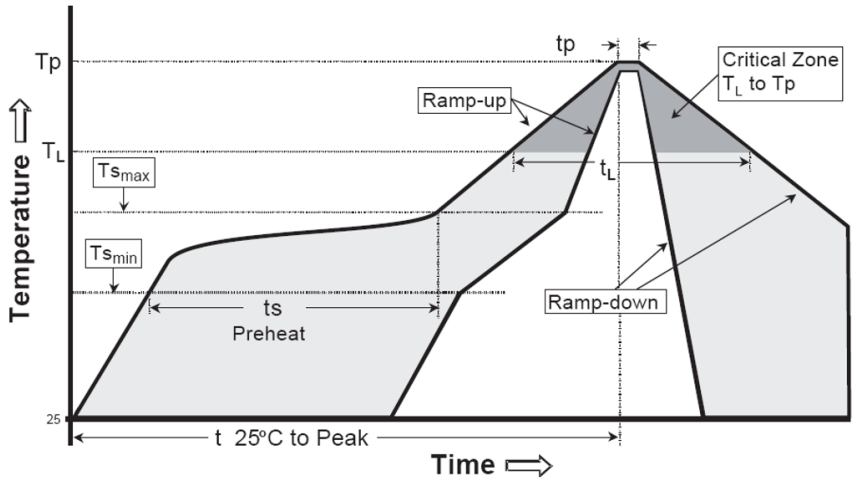
Table 19 • Classification Reflow Profiles

Profile Feature	Pb-Free Assembly
Average ramp-up rate (TS_{max} to Tp)	3 °C/second max
Preheat	150 °C
Temperature min (TS_{min})	200 °C
Temperature max (TS_{max})	60 seconds–180 seconds
Time (ts_{min} to ts_{max})	
Time maintained	217 °C
Temperature (T_L)	60 seconds–150 seconds
Time (t_L)	
Peak classification temperature (T_P)	240 °C–255 °C
Time within 5 °C of actual peak temperature (tp)	20 seconds–40 seconds
Ramp-down rate	6 °C/second max
Time 25 °C to peak temperature	8 minutes max

Note: All temperatures refer to topside of the package, measured on the package body surface.

The following figure shows the classification reflow profiles.

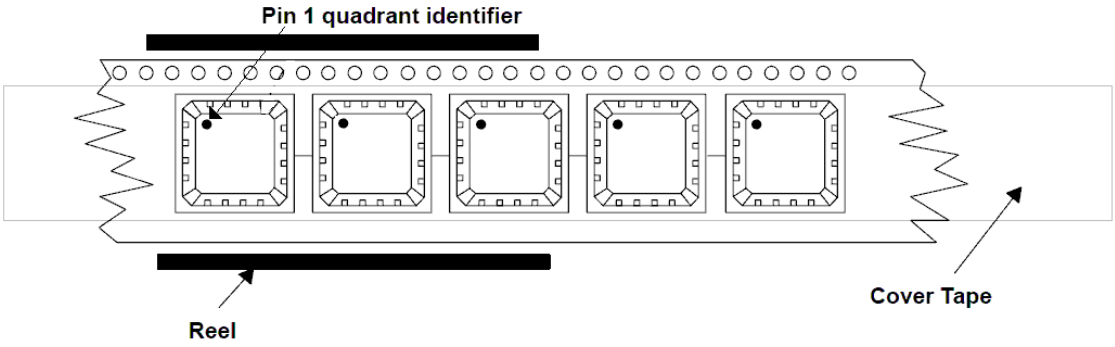
Figure 13 • Classification Reflow Profiles



6.4 Tape and Reel Packaging Information

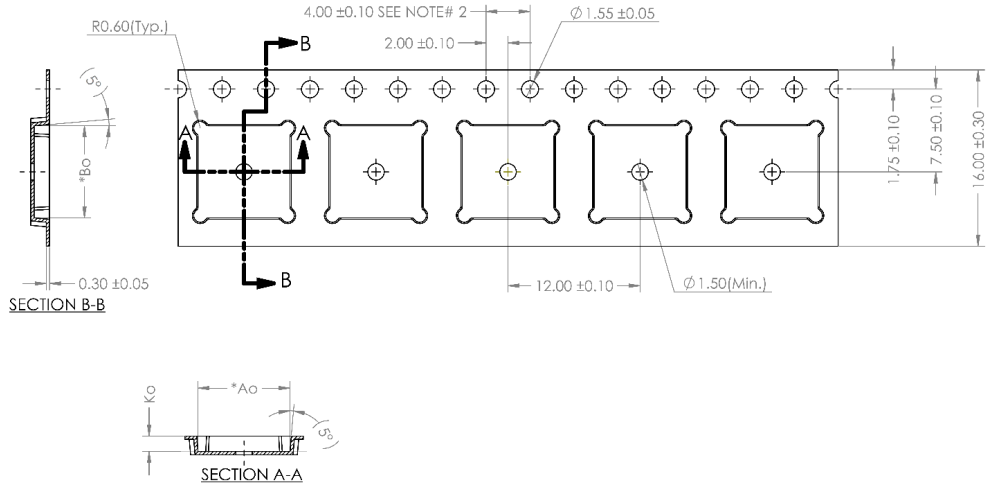
The following figure shows the Pin 1 orientation.

Figure 14 • Pin-1 Orientation



The following figure shows the tape and reel shipment specifications.

Figure 15 • Tape Shipment Specifications



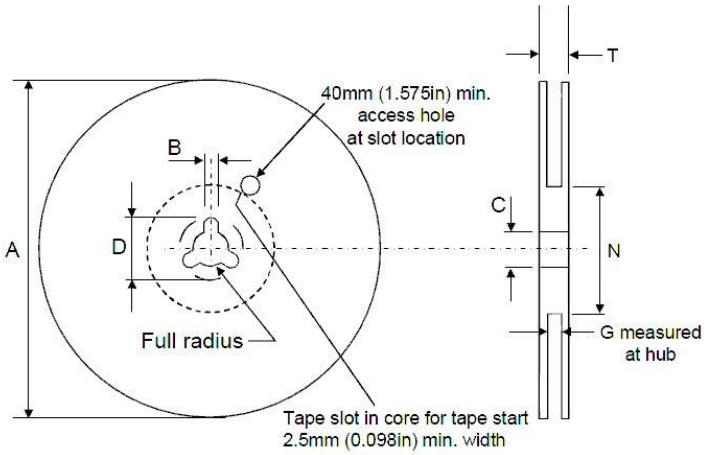
The following table lists the tape mechanical data.

Table 20 • Tape Mechanical Data

Dimensions	(mm)
Ao	8.35 ±0.10
Bo	8.35 ±0.10
Ko	1.40 ±0.10
K1	N/A
Pitch	12.00 ±0.10
Width	16.00 ±0.30

The following figure shows the reel specifications.

Figure 16 • Reel Specifications



The following table lists the reel mechanical data. The base quantity are 2000 pcs.

Table 21 • Reel Mechanical Data

Dimension	mm	Inch
Tape size	16.00 ±0.3	0.630 ±0.012
A max	330	13
B max	1.5	0.059
C	13.0 ±0.20	0.512 ±0.008
D min	20.2	0.795
N min	50	1.968
G	16.4 + 2.0/–0.0	0.645 + 0.079/–0.0
T max	29	1.142

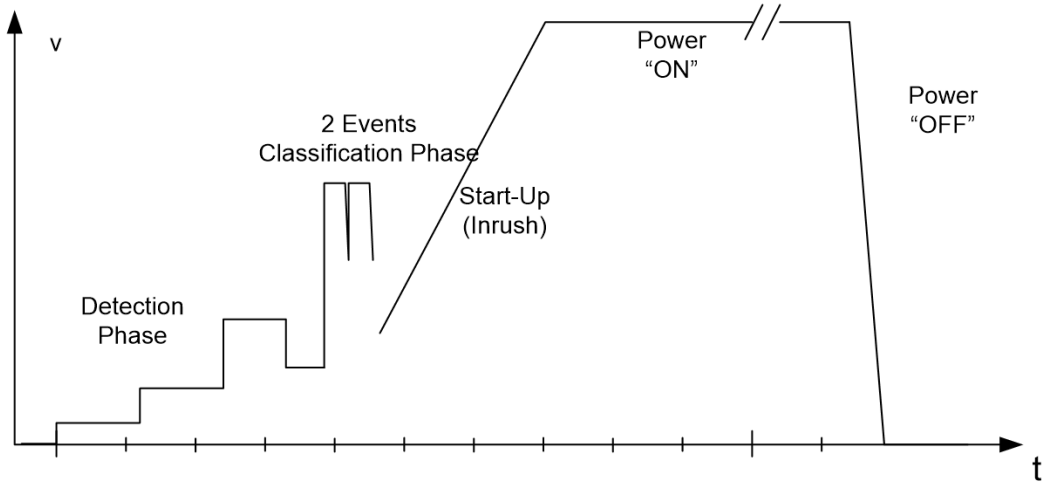
7 Application Information

PD69104B1 meets IEEE 802.3af and IEEE 802.3at functionality standards, as well as legacy (capacitor) and Cisco's PDs detection standards. Moreover, it supports additional protections such as short circuit, and dV/dT protection upon port startup.

7.1 Line Detection

The line detection feature detects a valid AF or AT load, as specified in the IEEE 802.3 standard. The resistance value should range from 19 kΩ to 26.5 kΩ. Line detection is based on four different voltage levels generated over the PD (the load), as shown in the following figure.

Figure 17 • Typical PoE Voltage vs. Time Diagram



The first two levels (low voltage level < 3 V) are for detecting if load up to 200 KΩ is connected to the PSE; preventing from applying high voltages on the PSE when there is no-load, and eliminating potential risk to the DTE. If the first detection passes, next two levels of resistor detection are applied. If the POE detects a valid resistor signature value, the detection is passed. Otherwise, the detection fails and moves to IDLE.

7.2 Legacy (Cap) Detection

If pin 36 (RES_CAP / INT_OUT) is set to "0", the detection mechanism of PD69104B1 is configured to detect and power LEGACY PDs, as well as AF/AT compliant PDs.
This mechanism also detects and powers CISCO Legacy PDs.

7.3 Classification

The classification process takes place immediately after the resistor detection is successfully completed. The main goal of the classification process is to detect the PD class, as specified in the IEEE 802.3AF and AT standards. The process is done by applying a voltage to the PD nodes and measuring the port current.
In the AF mode, the classification mechanism is based on a single-voltage level step (single finger).
In the AT mode, the classification mechanism is based on two-voltage level steps (dual finger), as defined in the IEEE 802.3at standard.

7.4 Port Startup

Upon a successful detection and classification process, power is applied to the load via a controlled startup mechanism.

During this period current is limited to 425 mA for a typical duration of 65 ms. This enables the PD load to charge and to enter a steady state power condition.

7.5 Over-Load Detection and Port Shut Down

After power up, PD69104B1 automatically initializes its internal protection mechanisms. These mechanisms are utilized to monitor and disconnect the power from the load in case of an extreme conditions scenario. For example, scenarios such as over-current or short ports terminals, as specified in the IEEE 802.3AF/AT standard.

7.6 Disconnect Detection

PD69104B1 supports the DC Disconnect function as per the IEEE 802.3AF/AT standard.
This mechanism continuously monitors the load current and disconnects the power in case it drops below 7.5 mA (typical) for more than 322 ms.

7.7 Over-temperature Protection

PD69104B1 has internal temperature sensors that continuously monitor the junction temperature and set alarm bit when it exceeds 120 °C, or disconnect load power when it exceeds 200 °C. This mechanism protects the device from extreme events, such as high ambient temperature or other thermo-mechanical failures that may damage the PD69104B1 device.
The Alarm threshold can be set by register.

7.8 V MAIN Out of Range Protection

The PD69104B1 automatically disconnects the ports power when V_{main} exceeds 58.5 V threshold (with 180 mV hysteresis) or drops below 40 V threshold (with 180 mV hysteresis). This extremely valuable feature protects the load in case the main power source is faulty or damaged.

7.9 Serial EEPROM Load Mechanism

The PD69104B1 is capable of loading its registers values from an external serial EEPROM during a boot slot time.
To utilize the EEPROM boot, the COMM_MODE pin must be set to E2PROM_MODE (not connected).

The following is a list of features for the PD69104B1 device.

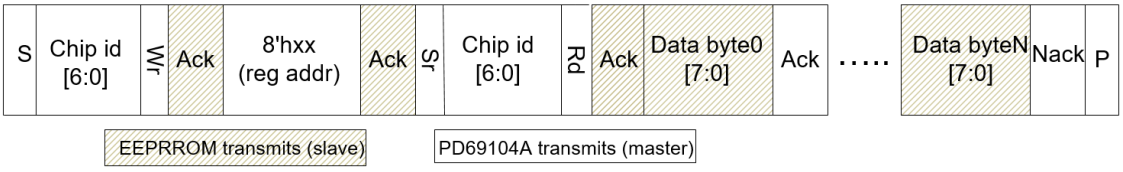
- MASTER I^2C communication.
- 7-bit addressing
- 250 KHz frequency
- EEPROM constant address: 7'hA0
- EEPROM must support read byte and read after read
- Two repeated transactions in case the EEPROM does not acknowledge the transaction
- A FIR filter for glitches cancelling

There are five consecutive read transaction (master transactions) made by the PD69104B1 for reading data from the EEPROM and uploading it to the PD69104B1 registers.

- The first transaction reads all registers from address 8'h70 to address 8'h9F.
- The second transaction reads registers HPEN and HPMD1 (from addresses 8'h44 and 8'h46).
- The third transaction reads register HPMD2 (from address 8'h4b).
- The fourth transaction reads register HPMD3 (from address 8'h50).
- The fifth transaction reads register `mp_hpmd4 (from address 8'h55).

The following figure shows the read transaction format.

Figure 18 • I2C EEPROM High-Level Packet Structure



For more information on the I²C timing constraint, see the Characteristics of the SDA and SCL Bus Lines for F/A-Mode I2C-Bus (see page 10) table.

The EEPROM registers mapping should be identical to the PD69104B1 registers mapping.

Note: In EEPROM mode, only I²C (not UART) is used by PD69104B1 for communication with the host (after finishing the configuration upload from EEPROM).

The following table lists the LED indications.

Table 22 • LED Indications

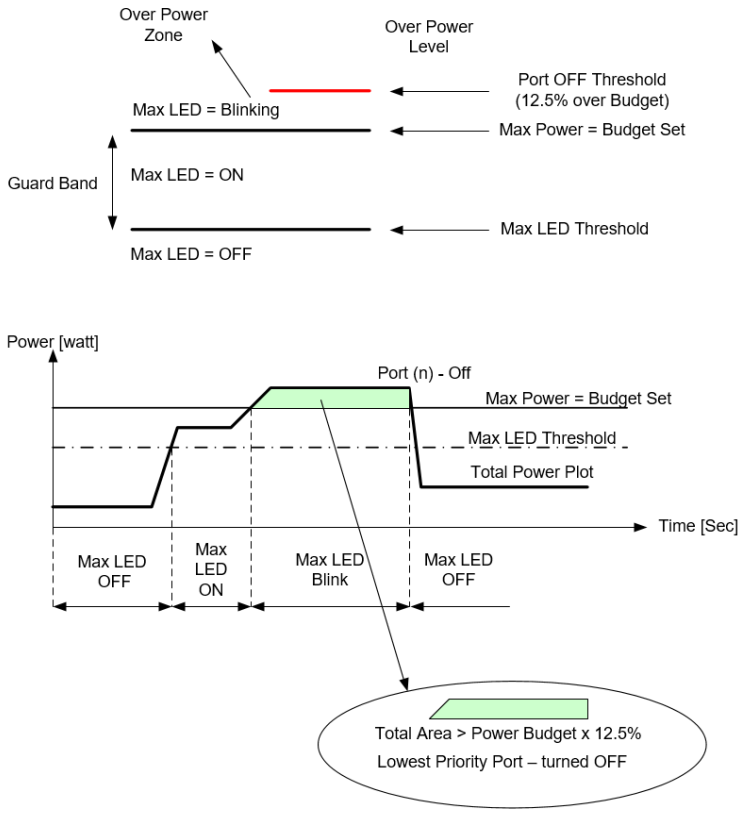
Pin	Status	LED
LED<3:0>	Port power on	On
	Power management event	0.4 Hz blink
	Port over load Port short circuit Port failed at startup	0.8 Hz blink
	Vmain_Out of range or over temp	All LEDs :3.3 Hz blink
	Port pff	Off
MAX_LED	Total power consumption is below power guard band determined by the user	Off
	Total power consumption is above power guard band but below total budget.	On
	Total power consumption is above total budget, or Power Integral is still positive	Blink

MAX_LED:

- Max power budget and max LED guard band (GB) can be configured through the following internal registers.
  - Max power budget registers: PWR_BNK0 to PWR_BNK7 (address 0x89 to 0x90)
  - Max LED guard band register: PoE_MAX_LED_GB (address 0x9F)
- PoE_MAX_LED_GB Register LSB = 1 W
- Max LED reflects total power for all 4 ports
- When total power consumption < (Max Power—Guard Band) > Max LED is OFF (below the bottom line)
- When total power consumption > (Max Power—Guard Band) > Max LED is ON (between the lines)
- When total power consumption > (Max Power) > LED is BLINKING (above top line)
- When total power > budget (above top line):
  - An internal digital power integration calculation machine starts integrating power
  - When this Integrated total power is larger than Budget + 12.5 % (RED LINE) > lowest priority port is turned OFF
  - This specific port LED is OFF
  - Max LED will reflect the NEW Total Power status
  - If ports turn off due to PM, their per port LEDs will blink (in PM frequency) and MAX_LED will turn off
  - Timing to shut down this port is proportional to the over power (above budget) but limited to a maximum of two seconds.
- In 4 pairs mode, use the master LED per port only (LED 1 and LED 3 are masters in 4 pairs mode, LED 0 and 2 should not be used).
- In 4 pairs mode, the port's LED blinks when the ports enter UDL condition, unlike the 2 pairs condition.

The following figure shows the MAX_LED behavior description.

Figure 19 • MAX_LED Behavior Description



For example:

- Budget = 100 W, GB = 20 W
- When total power = 70 W – MAX LED is OFF
- When total power = 85 W – MAX LED is ON (power Integrator is not activated)
- When total power = 110 W – MAX LED BLINKS (power Integrator is activated)—Port at lowest priority is shut off
- Timing to shut off is based on : delta(P) x T_{off} = Power Budget × 1.125
- In this example, 10 W x T_{off} = 100 W × 0.125 T_{off} = 1.25 seconds
- If total power = 105 W delta (P) = 5, then T_{off} = 2 seconds (the max timer)

The following table lists the power budget for the PD69104B1 device.

Table 23 • Power Budget

PS_PG3/ Bank Range Select	PS_PG2	PS_PG1	PS_PG0	Total Power Budget [W]	Remarks
0	0	0	0	144 (default value in AT low mode) 176 (default value in AT high mode)	Register PWR_BNK0
0	0	0	1	140 (default value)	Register PWR_BNK1
0	0	1	0	136 (default value)	Register PWR_BNK2
0	0	1	1	132 (default value)	Register PWR_BNK3

PS_PG3/ Bank Range Select	PS_PG2	PS_PG1	PS_PG0	Total Power Budget [W]	Remarks
0	1	0	0	128 (default value)	Register PWR_BNK4
0	1	0	1	124 (default value)	Register PWR_BNK5
0	1	1	0	120 (default value)	Register PWR_BNK6
0	1	1	1	116 (default value)	Register PWR_BNK7
1	0	0	0	112	Constant
1	0	0	1	108	Constant
1	0	1	0	104	Constant
1	0	1	1	100	Constant
1	1	0	0	96	Constant
1	1	0	1	92	Constant
1	1	1	0	88	Constant
1	1	1	1	84	Constant

Note: There are 16 power levels, whereas the first eight levels are registers that can be configured by users. During operation, a change in one of the PG pins changes PD69104B1's total power budget and may result in turning off ports. The power level can be set either by PS_PG0 to PS_PG3 pins or by the host through communication.

7.10 Reset Mechanism

To reset PD69104B1, the RESET line should be pulled low for more than 16 µs.

8 Ordering Information

The following table lists the ordering information for the PD69104B1 device. Both parts have plastic 48-pin QFN 8 mm × 8 mm and RoHS compliant/Pb-free, MSL3 package.

Table 24 • Ordering Information

Part Number	Package	Packaging Type	Temperature TA (°C)	Part Marking
PD69104B1ILQ	QFN 8 mm × 8 mm, 0.5 mm pitch 48 pins	Tray	–10 °C to 85 °C	Microsemi Logo PD69104B1 Z Z e3 YYWWNNN

Notes:

1. Available in tape and reel. Append the letters “TR” to the part number (for example, PD69104B1ILQ-TR).
2. ZZ e3: ZZ = Random character with no meaning and e3 = 2nd level interconnect.
3. YY = Year, WW = Week, NNN = Trace Code

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