Packaging FAQs

June 2011

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I. Physical Dimensions

1. What is a package footprint?

A package footprint is the actual layout used to attach a package to a printed circuit board (PCB). See an example of a package footprint at www.actel.com/documents/RecPCBdesign.pdf.

2. What is the flatness limit for all BGA packaged ICs?

Flatness refers to the amount of allowable package bend of the plane of the solder balls and bend of the plane of the package surface bearing the solder balls (Figure 1). Microsemi SoC Products Group packages satisfy the JEDEC standards for flatness on all BGA, FBGA, and CS packages. Refer to *Package Mechanical Drawings* at www.actel.com/documents/PckgMechDrwngs.pdf.

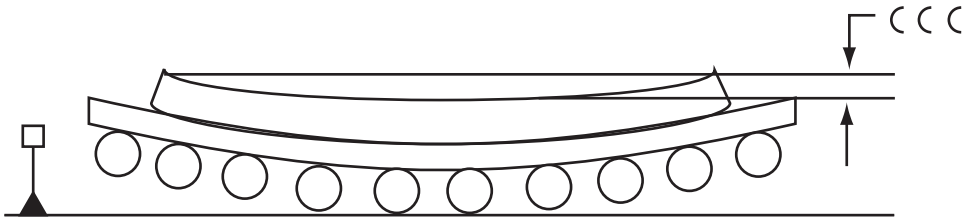

Figure 1: **Diagram of Flatness Measurement (from JEDEC Standard 95, page 4.17-17/A)**

3. Can Microsemi's packages be purchased in die form? If so, what are the die sizes for Microsemi's FPGAs?

Contact your local sales representative for bare die purchase information. The die size is proprietary information and is not made available publicly. Contact Technical Support at (800) 262-1060 or email soc_tech@microsemi.com for further information.

4. What is basic spacing between centers (BSC)?

To specify package mechanical dimensions, we frequently use the term BSC, which means basic spacing between centers. This is a theoretical true position dimension and has no tolerance (Figure 2).

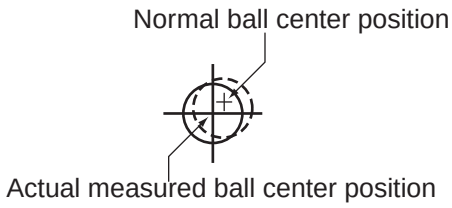

Figure 2: **Diagram of BSC Measurement (from JEDEC Standard 95, page 4.17-11/A)**

5. What is the land size for the Microsemi BGA package?

The land size of Microsemi's BG313, BG272, and BG329 is 0.75 ± 0.03 mm in diameter with solder mask defined open at 0.63 ± 0.03 mm, which is about 25 mils.

6. Where can I get information about total weights for Microsemi devices in various packages?

The latest package weight information is available in the *Package Thermal Characteristics and Weights* document: www.actel.com/documents/Package_Charact_Weights.pdf. Weights are approximate values. For greater accuracy, we recommend weighing the parts yourself. There may be slight variations from lot to lot.

7. Where can I get hermetic package mechanical configuration information (cavity, weight, lid size, and heat sink size)?

Refer to *Hermetic Package Mechanical Configuration* at: www.actel.com/documents/HermeticPckg.pdf.

8. What packaging considerations must be taken into account when changing a design from A54SX08-VQ100 to A54SX08A?

In order to transition from A54SX08-VQ100 to A54SX08A, you must make a package switch from the VQ100 to the TQ100.

These two packages have an identical footprint, but the package height is different:

SX – VQ100 package height = 1.2 mm

SX-A – TQ100 package height = 1.6 mm

The pinouts are basically the same, except that the VCCR pins on the SX device will be "no connects" on the SX-A device. The VCCR reference voltage was eliminated on the SX-A devices to enable a hot- swappable feature.

II. Materials

9. What materials are used in Microsemi's Plastic Leaded packages?

Table 1 lists the materials that are used in Microsemi's Plastic Leaded packages.

Table 1: **Standard Plastic Leaded Package**

Materials	Package Type				
	PLCC	**PQFP**	**TQFP**	**VQFP**	**RQFP**
Lead Frame					
Material	Cu 151	Cu 7025 or Cu 194	Cu 64T or Cu 194	Cu 64T or Cu 194	Cu 64T or Cu 194
Composition	99.9% Cu and 0.1% Zn	96.2% Cu, 3.0% Ni, 0.65% Si, and 0.15% Mg or 97.5% Cu, 2.35% Fe, 0.12% Zn and 0.03% P	96.17% Cu, 0.30% Cr, 0.27% Sn, and 0.26% Zn or 97.5% Cu, 2.35% Fe, 0.12% Zn and 0.03% P	96.17% Cu, 0.30% Cr, 0.27% Sn, and 0.26% Zn or 97.5% Cu, 2.35% Fe, 0.12% Zn and 0.03% P	96.17% Cu, 0.30% Cr, 0.27% Sn, and 0.26% Zn or 97.5% Cu, 2.35% Fe, 0.12% Zn and 0.03% P
Die Attach Material					
Type	Conductive				
Filler	Silver				
Wire					
Wire Size	1.0 or 1.2 mil				
Composition	99.99% Au				
Heat Sink					
Type	—	Anodized Aluminum	—	—	Copper Alloy
Mold Compound					
Resin	OCN (Ortho-creasol novolac)	OCN (Ortho-creasol novolac)	Bi-phenyl	Bi-phenyl	OCN (Ortho-creasol novolac)
Lead Finish					
Plating	Solder Plate				
Composition	85% Sn / 15% Pb				

10. What materials are used in Microsemi's Plastic Array packages?

Table 2 lists the materials that are used in Microsemi's Plastic Array packages.

Table 2: **Standard Plastic Ball Grid Array Package**

Materials	Package Type		
	PBGA	FBGA	CS
Substrate			
Material	BT (Bismaleimide Triazine) Resin		
Die Attach Material			
Type	Conductive		
Filler	Silver		
Wire			
Wire Size	1.0 mil		
Composition	99.99% Au		
Solder Ball			
Composition	62% Sn / 36% Pb / 2% Ag or 63% Sn/37% Pb	63% Sn / 37% Pb	62% Sn / 36% Pb / 2% Ag

11. What materials are used in Microsemi's Hermetic packages?

Table 3 lists the materials that are used in Microsemi's Hermetic packages.

Table 3: **Hermetic Package**

Materials	Package Type	
	CQFP	CPGA
Lead Frame		
Raw Material	Kovar	
Composition	53% Fe / 29% Ni / 17% Co / 1% others	
Finish	Gold over Nickel	
Subatrate		
Material	Alumina	
Composition	98%Al 202	
Bond Finger		
Bare Material	Tungsten	
Finish	Gold over Nickel	
Die Attach Material		
Type	Cynate Esther Paste	
Wire		
Wire Size	1.25 Mil or 1.0 Mil	
Composition	Al = 99% Al / 1% Si, Au = 99.99%	
Lid		
Raw Material	Kovar	
Composition	53% Fe / 29% Ni / 17% Co / 1% others	
Finish	Gold over Nickel	
Preform Composition	80% Au / 20% Sn	
Lead		
Finish	Gold or Solder Dip (63&Sn / 37% Pb)	

12. Which Microsemi packages are hermetically sealed?

The Ceramic Quad Flat package (CQFP), CCGA (Ceramic Column Grid Array), and CPGA (Ceramic Pin Grid Array) packages are hermetically sealed.

13. When using BGA, FBGA, and CS packages, what PCB material is recommended for use?

The PCB material can be FR-4 (Military-type GF) or FR-5 (Military-type GH).

14. For CQFP packages, there is a small metal lid on the base of the package. Is the die attached to this? Is it a heat sink for the die?

The die is not attached to this lid, and it is not a heat sink. There is an air cavity between the die and the lid. It is metal, so it does conduct some heat away from the package, but the die is not directly connected to it as in the RQ packages.

15. Do the PQFP packages have a heat sink? If so, what material is used?

Some of the PQFP packages have either an embedded (drop-in) heat spreader or an exposed heat spreader as described in *Plastic Packages Containing a Heat Spreader* at www.actel.com/documents/Heat_Spreader.pdf.

16. Which Microsemi packages have an internal cavity?

The CQFP, CPGA, and CCGA packages have an internal cavity. Some of the plastic packages have a heat spreader, as mentioned in *Plastic Packages Containing a Heat Spreader* at www.actel.com/documents/Heat_Spreader.pdf.

17. What is meant by 100% Matte Tin? Which lead termination does the A3PN030-ZQNG48I device have? Is the tin whisker test applicable for it?

100% Matte Tin means 100% tin and A3PN030-ZQNG48I external lead finish is 100% tin. The tin whisker test applies to 100% Sn matte plating only.

18. Do Hermetic devices ship with 100% Matte Tin leads?

No. Refer to the notification on use of pure tin at www.actel.com/documents/TinComponentsLtr.pdf.

19. Is there any Boron content in the FBGA package material or silicon (for Fusion and ProASIC®3 devices)?

No. There is no boron content in either the package material or silicon.

20. What is the lead-free package?

Japan now requires all semiconductors manufactured in their country to have lead-free packaging. Most Japan-based companies are insisting that all of their vendors comply with the regulations. Europe has moved in the same direction with its Restriction of Hazardous Substances (RoHS) directive, which required the replacement of lead in electrical and electronic equipment by January 1, 2007. One of the critical requirements is that lead-free packages should pass 260°C maximum surface mount temperature. Maximum operating temperature and other package characteristics will not change. The surface mount reflow temperature depends on package thickness and volume. Refer to the *Solder Reflow Profile for Standard and Lead-Free Packages* document: www.actel.com/documents/Solder_Reflow_LeadFree.pdf.

III. Moisture/Soldering

21. What is the specification for the various moisture sensitivity levels?

The specification is defined in the JEDEC standard J-STD-020C Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface-Mount Devices. Download the standard from the JEDEC website: www.jedec.org/download/search/.

22. What are the moisture sensitivity levels of Microsemi devices?

All Microsemi plastic packages have a moisture sensitivity rating of level 3, except for RQFP and QN packages, which have level 4 and 2, respectively. The BGA package is also a level 3 device. Hermetic packages are not moisture sensitive, so there is no moisture sensitivity level for ceramic packages such as CQFP, CPGA, and CCGA.

Refer to *Moisture Sensitivity* at www.actel.com/documents/Moisture_Sensitivity.pdf for more information.

23. What are the storage conditions for moisture sensitivity levels 3 and 4?

Storage condition for moisture sensitivity level 3:

- Floor Life: The allowable time period after removal from a moisture barrier bag and before the solder reflow processes for a moisture-sensitive device to be exposed to a factory ambient not exceeding 30°C, 60% RH, and168 hours.
- Safe Storage: Dry SMD packages held in a controlled humidity condition so that the Floor Life clock remains at zero. Acceptable safe storage conditions for SMD packages classified as level 3 are listed below:
  - Dry Pack: Dry packed SMD in an intact moisture barrier bag will have a calculated shelf life of at least 12 months from the bag seal date shown on the caution or bar code level.
  - Dry Atmosphere Cabinet: Storage cabinet that maintains low humidity by purging with dry air or nitrogen at 25 ± 5°C. The cabinet must be capable of recovering to the stated humidity rating within one hour from routine excursions such as door opening/closing.
  - Dry Cabinet at 5% RH: SMD packages not sealed in moisture barrier bags may be placed in a dry atmosphere cabinet, maintained at not greater than 5% RH.

Storage condition for moisture sensitivity level 4:

- Floor Life: The allowable time period after removal from a moisture barrier bag and before the solder reflow processes for a moisture-sensitive device to be exposed to a factory ambient not exceeding 30°C, 60% RH, and 72 hours.
- Safe Storage: Same as above.

24. Why does Microsemi recommend that some devices should be baked?

Certain device packages are sensitive to moisture. The recommended bake times will dry out any moisture that the plastic package has absorbed while sitting in the open. We base our bake times on moisture deabsorption data from our assembly plants.

25. Is there any reason not to bake the devices for 24 hours? If so, is the limitation due to lead oxidation causing poor solderability or is there another reason?

There is no problem associated with 24 hour dry bake; we prefer a shorter time to avoid any soldering problems.

26. Is there a recommended maximum number of bake cycles?

There is no recommended maximum limit for bake cycles.

27. What is the recommend baking process?

All of Microsemi's plastic packages have a moisture sensitivity rating of level 3, except for RQFP and QN packages, which have level 4 and 2, respectively. Microsemi recommends baking the parts at 125°C. The following table lists the bake times.

Bake Time for Package Types	Maximum Exposure Time to Ambient Condition Prior to Surface Mount	Bake Time at 125°C	Moisture Level
BG272, BG328, BG456, BG729	168 hours	8 hours	Level 3
FG144, FG256, FG324, FG484, FG676, FG896, FG1152	168 hours	8 hours	Level 3
VF49, VF128, VF180, VF289	168 hours	8 hours	Level 3
CS81, CS196, CS201, CS281	168 hours	8 hours	Level 3
UC81	168 hours	8 hours	Level 3
QN108, QN132, QN180	1 year	8 hours	Level 2
QN68	168 hours	8 hours	Level 3
RQ208, RQ240	72 hours	8 hours	Level 4
PQ100, PQ144, PQ160, PQ208, PQ240	168 hours	8 hours	Level 3
TQ64, TQ100, TQ144, TQ176	168 hours	5 hours	Level 3
VQ80, VQ100	168 hours	5 hours	Level 3
PL44, PL68, PL84	168 hours	8 hours	Level 3

28. Does Microsemi dry pack all their devices?

All packages are dry-packed except for CQFP and CPGA packages.

29. Where can I find the temperature profile for reflow soldering?

For more information, refer to *Standard Reflow Profile for Standard and Lead-Free Packages* at www.actel.com/documents/Solder_Reflow_LeadFree.pdf.

30. What is the maximum number of reflow cycles allowed for Microsemi FPGA packages?

The recommended maximum number of reflows is three.

31. Are the CQFP packages moisture sensitive?

CQFP packages are hermetically sealed and thus are not moisture sensitive.

32. How and where can the moisture sensitivity level be found on the Microsemi packaging?

The moisture sensitivity label is on the packing bag (Figure 3 on page 11 and Figure 4 on page 12).

Moisture Sensitive Warning Label

STANDARD PACKAGE

CAUTION! THIS BAG CONTAINS MOSITURE SENSITIVE
DEVICES WHICH HAVE BEEN SEALED UNDER
CONTROLLED CONDITIONS

1. After this bag is opened, devices that will be subjected to reflow or equivalent processing (peak package body temp. 200°) must be:
   PLCC, TQFP, VQFP, PQFP, BGA, CS and QFN packages:
   a) Mounted within 168 hours (level 3) at factory conditions of ≤ 30°C/60% RH, or
   b) Stored at ≤ 20% RH.
   RQ Packages (with heat sink)
   c) Mounted within 72 hours (level 4) at factory conditions of ≤ 30°C/60% RH, or
   d) Stored at ≤ 20% RH.

2. Devices for all packages require baking before mounting, if
   a) Humidity card is > 20% when read at 23°C ± 5°C or
   b) 1a or 1b (for PLCC, PQFP, TQFP, VQFP, BGA, and QFN), 1c or 1d (for RQ) are not met.

3. If baking is required, devices may be baked for:
   a) 192 hours at 40°C +5°C/–0°C and <5% RH for low temperature device containers, or
   b) 24 hours at 125°C ± 5°C for high temperature device containers.

Original Bag Seal Date:

Note: Body temperature defined by IPC/JEDEC J-STD-020

Figure 3: **Moisture Sensitive Warning Label – Leaded Lead-free Package**

LEADED LEAD-FREE PACKAGE
CAUTION! THIS BAG CONTAINS MOSITURE SENSITIVE
DEVICES WHICH HAVE BEEN SEALED UNDER
CONTROLLED CONDITIONS

1. After this bag is opened, devices that will be subjected to reflow or equivalent processing (peak package body temp. 245°C, 250°C or 260°C, depending on pkg. thickness & volume) must be: PLCC, TQFP, VQFP, PQFP and QFN packages:
   a) Mounted within 168 hours (level 3) at factory conditions of ≤30°C/60% RH, or
   b) Stored at < 10% RH.

2. Devices for all packages require baking before mounting, if
   a) Humidity card is > 20% when read at 23°C ± 5°C or
   b) 1a or 1b (for PLCC, TQFP, VQFP, PQFP and QFN)

3. If baking is required, devices may be baked for:
   a) 192 hours at 40°C + 5°C/–0°C and < 5% RH for low temperature device containers, or
   b) 24 hours at 125°C ±5°C for high temperature device containers.

Original Bag Seal Date: _____

Note: Body temperature defined by IPC/JEDEC J-STD-020

Figure 4: **Moisture Sensitive Warning Label – Array Lead-free Package**

IV. Miscellaneous

33. What is JEDEC?

The JEDEC Solid State Technology Association, once known as the Joint Electron Device Engineering Council, is the semiconductor engineering standardization body of the Electronic Industries Alliance (EIA), a trade association that represents all areas of the electronics industry. Many of today's packaging standards are defined by JEDEC specification, and these specifications will be referenced from time to time. More information is available at www.jedec.org/.

34. What are the recommended sockets for Microsemi FPGAs?

The recommended sockets for Microsemi FPGAs can be found at the following web page: www.actel.com/products/solutions/package/docs.aspx#prototyping.

35. What are the die bond pin assignments for PGA and BGA packages?

Contact Technical Support at (800) 262-1060 or email soc_tech@microsemi.com to obtain the wire bond diagrams for the device you are using. The linked files below are cross-reference charts that list the die pad number and the pin to which it corresponds on all BGA and PGA packages.

Note that VSS and VKS = GND, all VPP and VSV = VCC.

1010PG84	1020PG84	1225PG84
1240PG132	1280PG176	14100BG313
14100PG257	1415PG100	1425PG133
1440PG175	1460BG225	1460PG207

36. Do you have any information on forming and trimming the leads for CQFP packages?

CQFP packages are an industry standard for applications operating in extreme conditions and high reliability expectations. Designers for Military applications routinely choose CQFPs due to their high reliability characteristics. These characteristics include package reliability at high temperatures and resistance to moisture due to being hermetically sealed. Microsemi provides a range of CQFP packages for all Microsemi devices. For more information on the specific devices, refer to www.actel.com.

The document at www.actel.com/docs/sockets/sy-cq196.pdf shows a drawing of a CQFP package. The bottom of the first page shows a CQFP package in its frame, also referred to as a Ceramic Tie Bar, and the package leads are attached to the frame. CQFP packages are shipped from Microsemi with these frames attached. CQFP devices are programmed by inserting the package into a CQFP programming adapter on an Microsemi Activator. The next step is to trim and form the leads (Gullwing shape) to surface mount the device onto the circuit board. Microsemi recommends that this procedure is handled by vendors who specialize in trimming and forming leads. One such vendor is Fancort Industries, Inc. For more information regarding trimming and forming leads for CQFP packages, contact Fancort Industries at:

Fancort Industries, Inc.

31 Fairfield

West Caldwell, NJ 07006

Phone (201) 575-0610

Fax (201) 575-9234

The 84-pin CQFP package is shipped and handled differently than the other CQFP packages. For the 84-pin CQFP package, each device and its frame are placed inside a chip carrier and then shipped.
The 84-pin CQFP device is programmed by inserting the package with chip carrier into a CQFP programming adapter on an Microsemi Activator. Once the device is programmed and ready to be surface mounted onto the circuit board, the carrier must be removed. The CQFP package is unloaded from the carrier using a carrier extraction tool. One such carrier extraction tool is manufactured by Wells, who also manufactures the chip carriers. The part number for the carrier extraction tool is T-0315-9. The next step is to trim and form the leads (Gullwing shape) to surface mount the device onto the circuit board as with the other CQFP packages.

37. Are lids on Microsemi's ceramic packages grounded?

Yes, lids on all Microsemi ceramic packages, including Ceramic Pin Grid Array (CPGA) and Ceramic Quad Flat Pack (CQFP), are grounded.

38. Are there any recommendations for connecting the heat sink to the board GND?

The heat sink is connected to an internal package GND panel so it is not necessary to connect the heat sink to the board GND.

39. Are there any recommendations for the epoxy used on a PCB for system and package vibration tests?

No, we do not provide a recommendation. The tester should follow the standard testing method, and the epoxy material depends on the test condition.

40. Does Microsemi perform the Particle Impact Noise Detection (PIND) test on any devices?

We do PIND for RH and RT devices.

41. What is the difference between RQFP and PQFP packages?

RQFP has an exposed heat slug, and PQFP does not.

42. Why do I see notches on the leads of CQFP package?

The notches are placed on the package pins during rework to attain compliance with the package lead specifications. The form factor of this rework is clearly defined on MIL-STD-1835B, Notice 2, detail G on page 136 (see sketch) and note 11 on page 141. See the detailed explanation in the *Lead Frame Rework* on Microsemi CQFP Packages located at www.actel.com/documents/LeadRework.pdf.

43. What type of ink is used to mark Microsemi devices and where can I find the details regarding the change from Ink to Laser marking methodology for Microsemi devices?

For Plastic packages: Markem 4481, 4488 white or equivalent for heat cure.

For Ceramic packages: Markem 4405, 4408R, 4488 black or equivalent for heat cure.

Markem 4481, 4488 white or equivalent for backside mark.

Most units are now lasered marked. Package markings could have both ink and laser markings.

Details regarding the change from ink to Laser marking can be found on the website:
www.actel.com/documents/PCN0612_LaserMarking.pdf.

44. What are the "lot number" and "date code" and where can they be found on a Microsemi FPGA? what do the different markings on packages mean?

To trace a device's lot history from qualification test records, Microsemi must have the lot number of the device under investigation. The lot number allows Microsemi to identify the silicon ingot and wafer from which the device was fabricated.

For most Microsemi FPGAs, the lot code and date code are now printed on top of the package. In either case, the lot number is easy to identify, given the following example:

Lot Number: 2ACT312381

Date Code: 9919

These values indicate that the device was fabricated the 19th week, 1999, and the wafer is from the lot number #2ACT312381.

Figure 5 and Figure 6 on page 16 show the top and bottom side marking of different packages. Markings vary slightly from package to package. Figure 5 shows the markings used in all packages with special markings used in specific packages.

Front View Description

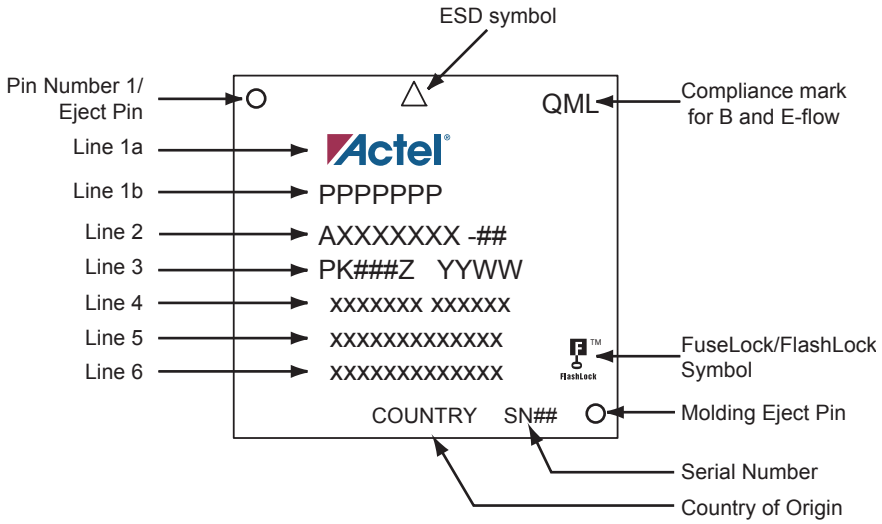

Figure 5: **Front View Description**

Line 1 can be Line 1a or Line1a plus Line 1b.

Line 1a: "Actel Logo"

a. Actel Logo applies to all Actel products except radiation hardened (RH) products.

b. Actel Logo continues to apply to RH product including CQ84 and CQ172 packages.

c. CS49 package uses text "ACTEL" instead of Actel Logo.

Line 1b: Logo of ProASIC, ProASIC$^{PLUS®}$, ProASIC3, ProASIC3E, or Axcelerator®
(this is referred to as PPPPPPP in Figure 5).

Line 2: AXXXXXXX - ##

AXXXXXXX: Actel Device type; examples A1010A, A1020A, etc.

–##: Speed Grade. Available Speed Grades are: F, Standard (Blank), 1, 2, 3.

Line 3: PK###Z YYWW

PK: Package code:

- BG: BGA
- PQ: PQFP
- CS: Chip Scale Package
- RQ: EDQUAD TQ: Thin QFP
- VQ: Very Thin QFP
- PL: PLCC
- FG: Fine Pitch BGA

###: Number of leads: 68, 84, 176, 208, etc.

Z: Temperature Grade:

- B: MIL-883 Class B
- I: Industrial
- C: Commercial
- M: Military
- E: MIL-883 Extended Flow
- PP: Pre Production
- ES: Engineering Samples
- A: Automotive

Note: For MX, SX, ProASIC, eX, SX-A, ProASIC^{PLUS}, Axcelerator, ProASIC3, and ProASIC3E, the "C" for commercial temperature is not marked unless otherwise specified.

The I, A, and M designators may also be marked in the upper right hand corner of the package.

YYWW: Assembly Date Code

YY: Last two digits for seal year

WW: Work week the part was sealed

Line 4, 5: Customer Type Number as specified on lot traveler

Line 4: "X79" for Lead (Pb) free packages

Back View Description

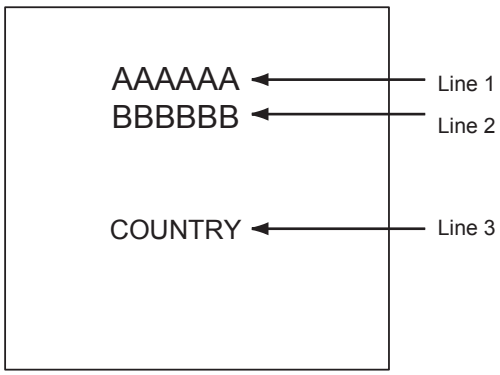

Figure 6: **Back View Description**

Line 1: AAAAAA = Wafer Lot number

Line 2: BBBBBB = Assembly Lot number (optional)

Line 3: Assembly Location: Hong Kong, Philippines, Korea, Taiwan, Singapore, or USA.

Specific Marking Requirement

Plastic Packages

The FuseLock™ or FlashLock® logo (refer to the *Security FAQ* for details) appeared on all plastic packages (including PQ, TQ, VQ, BG, FG, CS, and PL). It was marked on the right bottom corner (above the molding eject pin if there was a molding eject pin on the package at the right bottom corner). Placement of Fuselock and Flashlock logos on devices was discontinued in 2009 (PCN 0915).

For the RQ package with a heat sink on the back of the package (A14100A and A14100B only) and BG packages, only a front marking is present. Lines 1-3 as shown in Figure 5 on page 15 are marked on the front. Line 4 contains the wafer lot number and assembly lot number, also shown in Figure 6 as AAAAAA BBBBBB.

For the RQ package with the heat sink on the front of the package (A32200DX and A32300DX only), wafer lot number and assembly location are marked on the back of the package, as shown in Figure 6. For BG and FG packages, the country of origin is marked on the front at the bottom, as shown in Figure 5 on page 15 as COUNTRY.

For the CS49 package, the country of origin is placed in the same line with the word ACTEL (line 1) and is identified by a three-character symbol – SIN for Singapore.

For CS128 and CS180, the country code is placed in Line 5 and is identified by a three-character symbol – SIN for Singapore. The Actel lot number is marked in Line 4.

There is no backside marking on Chip Scale Packages.

For the PQ160 cavity down package (for example, A32140DX-PQ160 and A32100DX-PQ160 assembled in STATS), a white dot is added to indicate Pin 1 orientation (Figure 5 on page 15).

Ceramic Packages – Top Side Marking

For military identification: the ESD triangle is marked on all military parts, centered above the Actel Logo. QML compliance mark is used ONLY on all Class B and E-flow devices that have an approved SMD. The QML compliance mark is on the top right corner on the same line as the ESD mark.

Table 4: **QML Compliance Mark**

Assembly Flow	Compliance Mark
Commercial	None
Military Temperature	None
Military Class B	QML
Military E-flow	QML

Line 4 is used for the SMD mark: DSCC SMD device lot and applicable lead finish.

For extended flow and 883B flow, which require a serialization mark, the serial mark is located at bottom right corner, shown in Figure 5 on page 15 with the SN##.

Ceramic Packages – Back Marking

An alternative mark format is used for PG100. The wafer lot number in Line 1 and the assembly location in Line 3 of the back marking (Figure 6 on page 16) are marked on the top.

QML Class V devices have only the serial number on the back.

Ceramic Column Grid Array (CG) and Ceramic Carrier (CC)

CG – All marks are on front only. Marking of CG is the same as ceramic packages, except wafer lot and country of origin are added on the front marking.

CC – All marks are on the front only. Marking for CC will follow the sequence listed below.

Line 1: Actel Logo

Line 2: Device name

Line 3: CC###ZSYYWW

Where:

CC: Package code

###: Lead count

Z: Product Grade

S: 1 to 2 blank spaces

YYWW: Assembly Date Code.
YY: Last two digits for seal year.

WW: Work week the part was sealed.

Line 4: Country of Origin

45. Where can I find the new part marking methodology for Microsemi devices?

Refer to the following document: www.actel.com/documents/CN1004_newmarking.pdf.

46. What does the designator “K” stand for?

K stands for the extended temperature selection (– 55°C to 100°C) for Fusion devices.

47. Does Microsemi provide OrCAD symbols for its packages?

We do not have OrCAD schematics of our parts but there is a way to generate them if you have a version of OrCAD.

The EDA tool vendors supply those libraries. OrCAD has a **New Part from Spreadsheet** command in their capture tool that should allow you to automatically generate a symbol from a spreadsheet containing pin number, pin name, pin type, etc. For all Microsemi device families, you can manually enter the pin information into the OrCAD spreadsheet to generate the symbol.
Contact Technical Support at (800) 262-1060 or email soc_tech@microsemi.com for the pin list of various Microsemi device families.

If you can give the CAE the full part number, the CAE can provide you with the pinout spreadsheet for that part. Then you can simply copy and paste this file into your OrCAD file to generate the symbol. Refer to www.ema-eda.com/newsltr/nov05/TECH_Article_FPGAs_11-05.htm.

48. Where can I find the theta ja, jb, and jc values?

Refer to the respective device datasheets for the values of theta ja and jc. For theta jb, contact Technical Support at (800) 262-1060 or email to soc_tech@microsemi.comfor further information.

49. How can I infer from the part number that the component is RoHS compliant or not and what does the suffix “X79” refer to?

Microsemi part numbers with the letter G included after the package designator indicate that the devices are RoHS6 compliant. For example: A40MX04-PLG44.

X79 means lead free. It has the same meaning as the indicator “G” in the package name, which refers to the lead free component.

50. How can I obtain Material Content Declaration information for a particular device and package combination?

Contact Technical Support at (800) 262-1060 or email soc_tech@microsemi.com for information on devices and package combinations.

V. Related Documents

Links to various important Package related documents:

RoHS compliant components

www.actel.com/documents/RoHS_Compliant_Components.pdf

RoHS certificate of Compliance

www.actel.com/documents/RoHS_Certificate.pdf

Standard Reflow Profile for Standard and Lead-Free Packages

www.actel.com/documents/Solder_Reflow_LeadFree.pdf

Package Mechanical Drawings

www.actel.com/documents/PckgMechDrwngs.pdf

Moisture Sensitivity

www.actel.com/documents/Moisture_Sensitivity.pdf

Environmental Packaging FAQ

www.actel.com/documents/Environmental_FAQs.pdf

VI. List of Changes

The following table lists critical changes that were made in each revision of the document.

Revision*	Changes	Page
Revision 3 (June 2011)	Added Question 18 (SAR 30679) and updated the answer for Question 20 (SAR 30679).	8
	For Question 27, naming conventions in the table were changed as per *Package Mechanical Drawings* document (SAR 30679).	10
	Added Question 30, Question 31, and Question 32 (SAR 30679).	10
	Added Figure 3 and Figure 4 (SAR 30679).	11 , 12
	Restructured the answer for Question 41 (SAR 27167).	14
	Updated Question 43 and Question 44 to match current practices (SAR 29632).	14, 15
	Added Question 46, Question 47, Question 48, Question 49, and Question 50 (SAR 30679).	18

*Note: *The revision number is located in the part number after the hyphen. The part number is displayed at the bottom of the last page of the document. The digits following the slash indicate the month and year of publication.*

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