AN4682

PolarFire FPGA Temperature and Voltage Sensor

Introduction

Each PolarFire device is equipped with a Temperature and Voltage Sensor (TVS). TVS reports die temperature and voltage of device supply rails in digital form to the FPGA fabric.

TVS is implemented using a 4-channel ADC, and the channel information is given as follows:

- Channel 0—1V voltage supply
- Channel 1—1.8V voltage supply
- Channel 2—2.5V voltage supply
- Channel 3—Die temperature

The TVS outputs a 16-bit encoded value that represents voltage or temperature and the corresponding channel number. The temperature and voltage information is translated into standard temperature and voltage values. For more information, see PolarFire FPGA and PolarFire SoC FPGA Security User Guide.

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1. PolarFire FPGA Temperature and Voltage Sensor

This demo highlights the TVS feature of the PolarFire using a UART-based application (GUI). The demo design continuously pumps the data from TVS channels to UART, displayed on the GUI. This demo design also shows how to simulate the TVS feature of the PolarFire device.

The demo design can be programmed using one of the following options:

- Using the job file: To program the device using the job file provided along with the design files, see 4. Appendix 1: Programming the Device Using FlashPro Express.
- Using Libero SoC: To program the device using Libero SoC, see 2. Libero Design Flow. Use this option when the demo design is modified.

1.1 Design Requirements

The following table lists the hardware and software requirements for this demo design.

Table 1-1. Design Requirements

Requirement	Version
Operating system	64-bit Windows 7, 8, or 10
Hardware	
PolarFire Evaluation Kit (MPF300-EVAL-KIT)	Rev D or later
Software	
Libero SoC	**Note:** Refer to the `readme.txt` file provided in the design files for the software versions used with this reference design.
ModelSim	
FlashPro Express	

Important: Libero SmartDesign and configuration screen shots shown in this document are for illustration purpose only. Open the Libero design to see the latest updates.

1.2 Prerequisites

Before you begin:

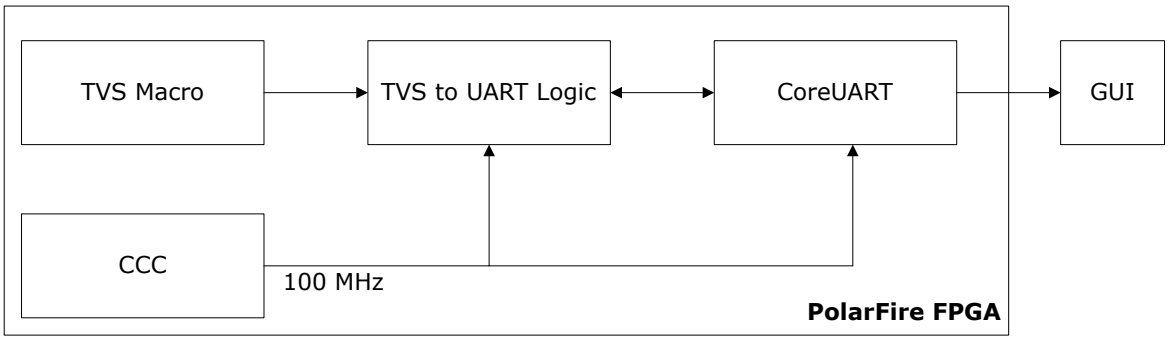
For demo design files download link:
www.microchip.com/en-us/application-notes/AN4682

Download and install Libero SoC (as indicated in the website for this design) on the host PC from the following location:
Libero SoC Installation link
The latest versions of ModelSim, Synplify Pro, and FTDI drivers are included in the Libero SoC installation package.

1.3 Demo Design

The following figure shows the top-level block diagram of the TVS design. All four channels of TVS are enabled in the design to monitor the die temperature and voltage rails. The Fabric logic captures the TVS channels outputs and sends them to UART IF through CoreUART IP.

Figure 1-1. TVS Block Diagram



The GUI receives TVS values per channel and decodes to display them as described:

Die Temperature

The temperature channel's 16-bit output value is represented in Kelvin and can be decoded as listed in the following table. For example, the temperature channel's output value of 0x133B implies 307.56 Kelvin.

Table 1-2. Temperature Channel Value Decoding

Bit Number	Description
15	Reserved
[14:4]	Integer value of temperature
[3:0]	Fractional value of temperature

Voltage

The data present at the VALUE and CHANNEL outputs are valid only when the VALID output is asserted. When a channel is disabled by deasserting the corresponding channel enable input, then the channel data present on the outputs is not valid even if the VALID output is asserted. The voltage channel's 16-bit output value is represented in millivolts (mV) and can be decoded as listed in the following table. For example, the voltage channel's output value of 0x385E implies 1803.75 mV.

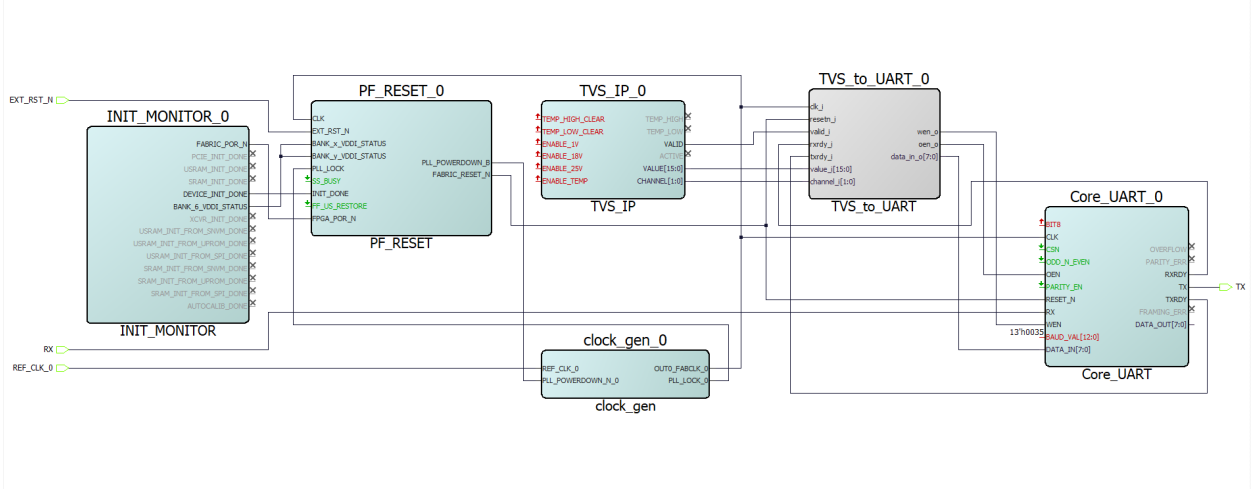
Table 1-3. Voltage Channel Value Decoding

Bit Number	Description
15	Signed bit
[14:3]	Integer value of voltage
[2:0]	Fractional value of voltage

1.3.1 Design Implementation

The following figure shows the Libero SoC software design implementation of the TVS demo design.

Figure 1-2. TVS Demo Design



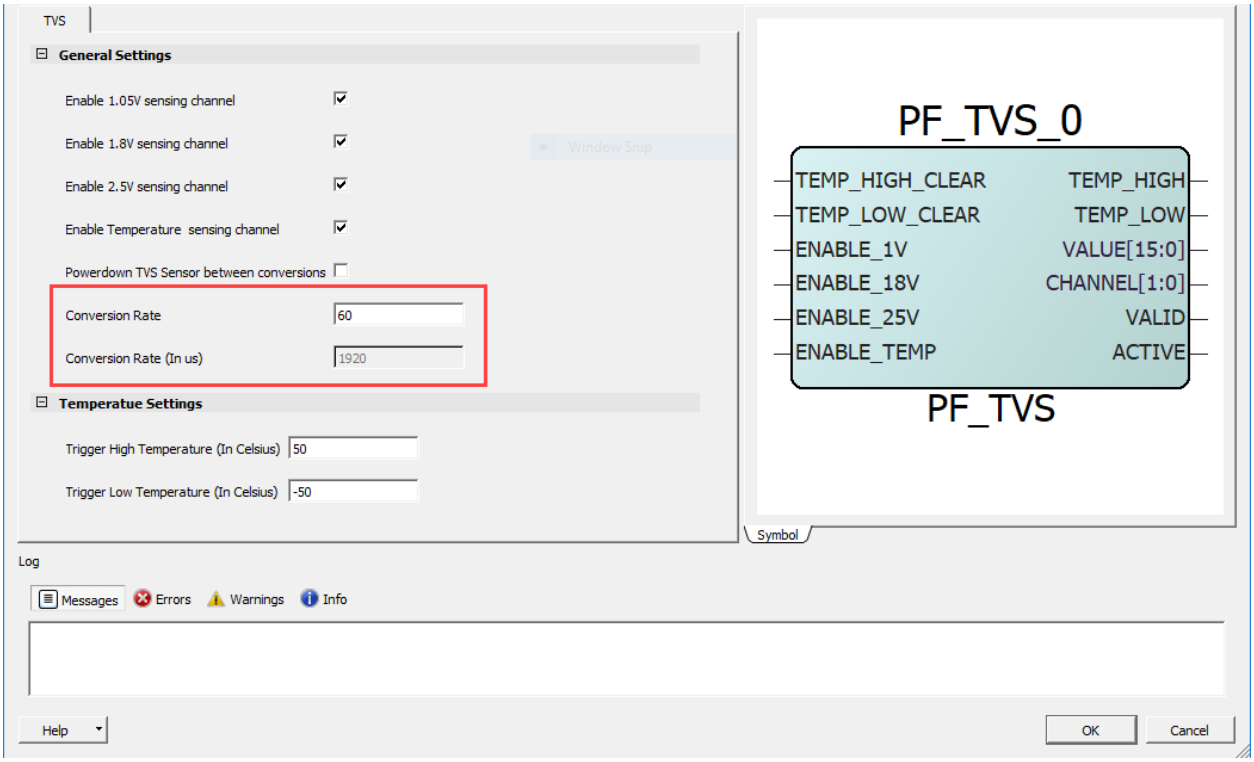
The top-level design includes the following components:

- TVS_IP_0 Macro
- Core_UART_0
- TVS_to_UART_0 logic
- clock_gen_0
- INIT_MONITOR_0 and PF_RESET_0

1.3.1.1 TVS_IP_0 Macro

The following figure shows the TVS interface configurator.

Figure 1-3. TVS Configurator



The GUI displays the die temperature in degree Celsius by converting Kelvin values.

Celsius value = Kelvin value - 273.15

1.3.1.2 TVS_to_UART_0

The TVS to UART logic captures the Temperature and Voltage values from the TVS macro and sends the data to Core_UART_0.

1.3.1.3 clock_gen_0

CCC is configured to generate the 100 MHz clock.

1.4 Simulation Flow

The TVS simulation model updates the TVS macro outputs based on reading instructions given in the `.mem` file or `.txt` file. The file name must be passed to the simulation model for the TVS outputs to toggle. The parameter used to store the `.mem` file name is called “TVS_MEMFILE”. Add the following `vsim` command to pass the file name.

```
-gTVS_MEMFILE="PATH_TO_FILE_RELATIVE_TO_SIMULATION_FOLDER"
```

.MEM File Format

The following format of the file is in hex:

```
<simulation time (τ) in hexadecimal>
```

```
<value of channel 0 at time τ>
```

```
<value of channel 1 at time τ>
```

```
<value of channel 2 at time τ>
```

```
<value of channel 3 at time τ>
```

The `.mem` file contains the simulation time followed by the digital values (16-bit) of the four ADC channels at that time. A value is required for the channel even if it is not used. The value can be 0. The simulation starts with all channel outputs being 0. The pattern can be repeated several times in the .mem file to reflect several values of the channel outputs. The content of the mem file is limited to 256 lines.

1.4.1 Simulating the Design

The Libero project includes a test-bench to simulate the TVS block. The testbench captures all four TVS channel values using CoreUART IP. The digital values for the four channels are passed through the `.mem` file.

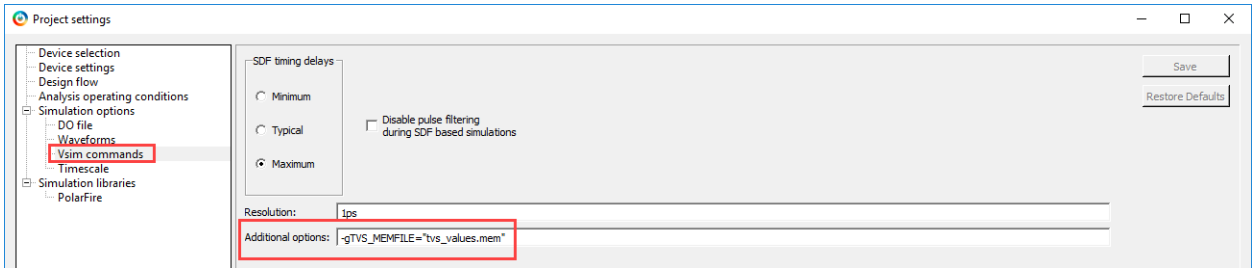
1.4.1.1 Simulation Settings

Perform the following steps to pass the `.mem` file for simulation:

1. Open the Libero SoC project settings (**Project** > **Project Settings**).
2. Select Vsim commands under the **Simulation options**. Enter `-gTVS_MEMFILE="tvs_values.mem"` in the **Additional options** field and then click **Save**.

A sample tvs_values.mem file is provided in the simulation folder. The .mem file must be available in simulation folder of the Libero project. The tvs_values.mem file captures the 16-bit digital output of the TVS block at different time instances.

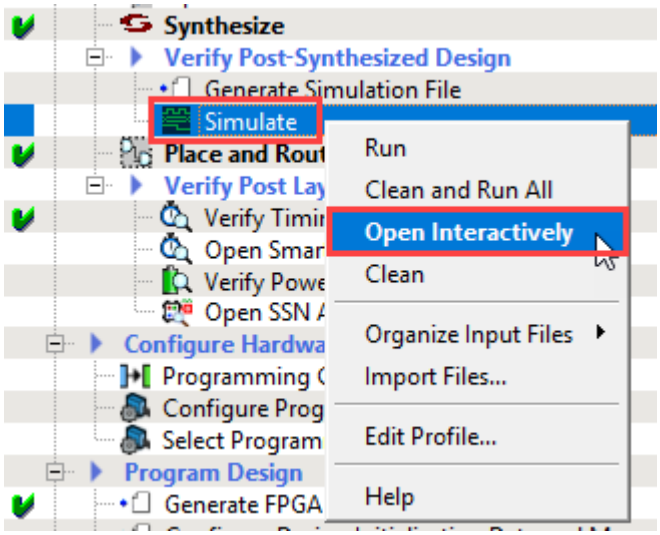
Figure 1-4. Simulation Options-Vsim Command



Perform the following steps to simulate the design:

1. In the **Design Flow** tab, right click **Simulate** under **Verify Pre-Synthesis Design** and then select **Open Interactively**.

   Figure 1-5. Design Flow-Simulate

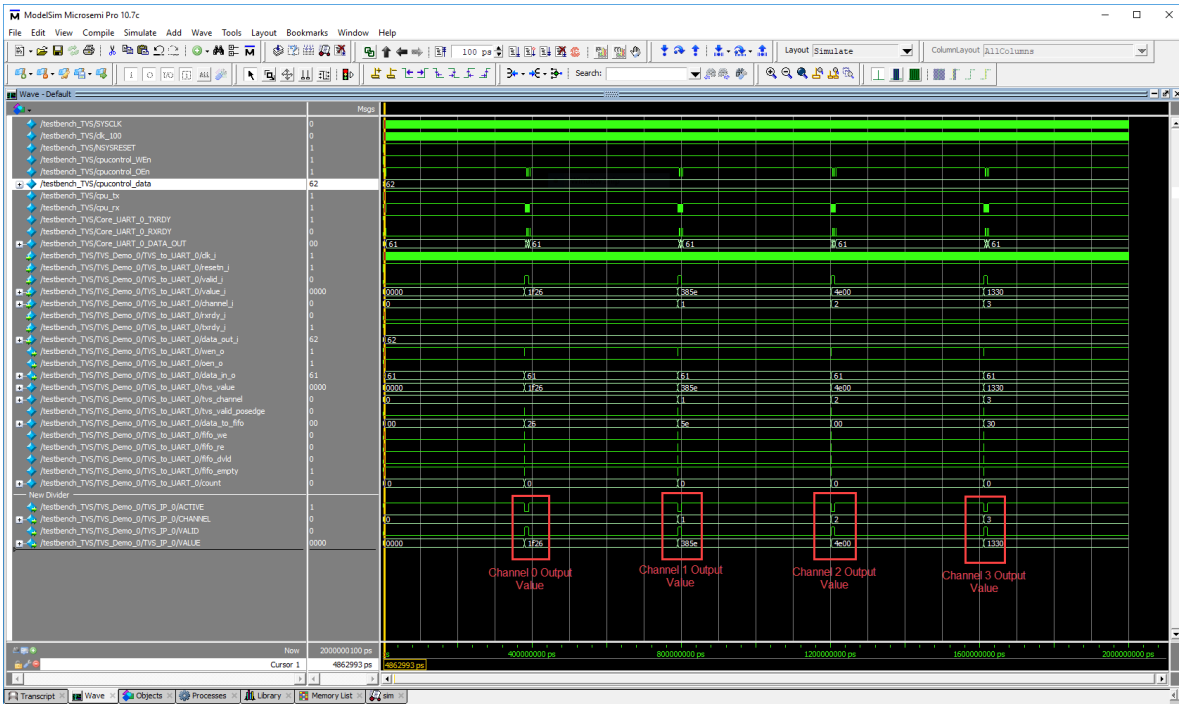


   The Wave window appears when the simulation is completed, as shown in the following figure. Since all the four channels are enabled, the TVS circuit outputs a value of the four channels at a given point in time on the VALUE output along with the channel number on the CHANNEL output. The data present on the VALUE and CHANNEL outputs are valid only when the VALID output is asserted. Observe the following from the simulation results:

   - After the channel is enabled for conversion, the TVS block takes 390 microseconds to complete the conversion.
   - Each channel has a conversion delay of 410 microseconds.
   - The conversion rate is equal to 1920 microseconds, which is same as the conversion rate set in the TVS configurator.
   - TVS block generates the output values based on the values given in the tvs_values.mem file.

2. The following figure shows the UI of ModelSim Pro ME Wave window.

Figure 1-6. ModelSim Pro ME Wave Window



3. Close ModelSim Pro ME and the Libero project.

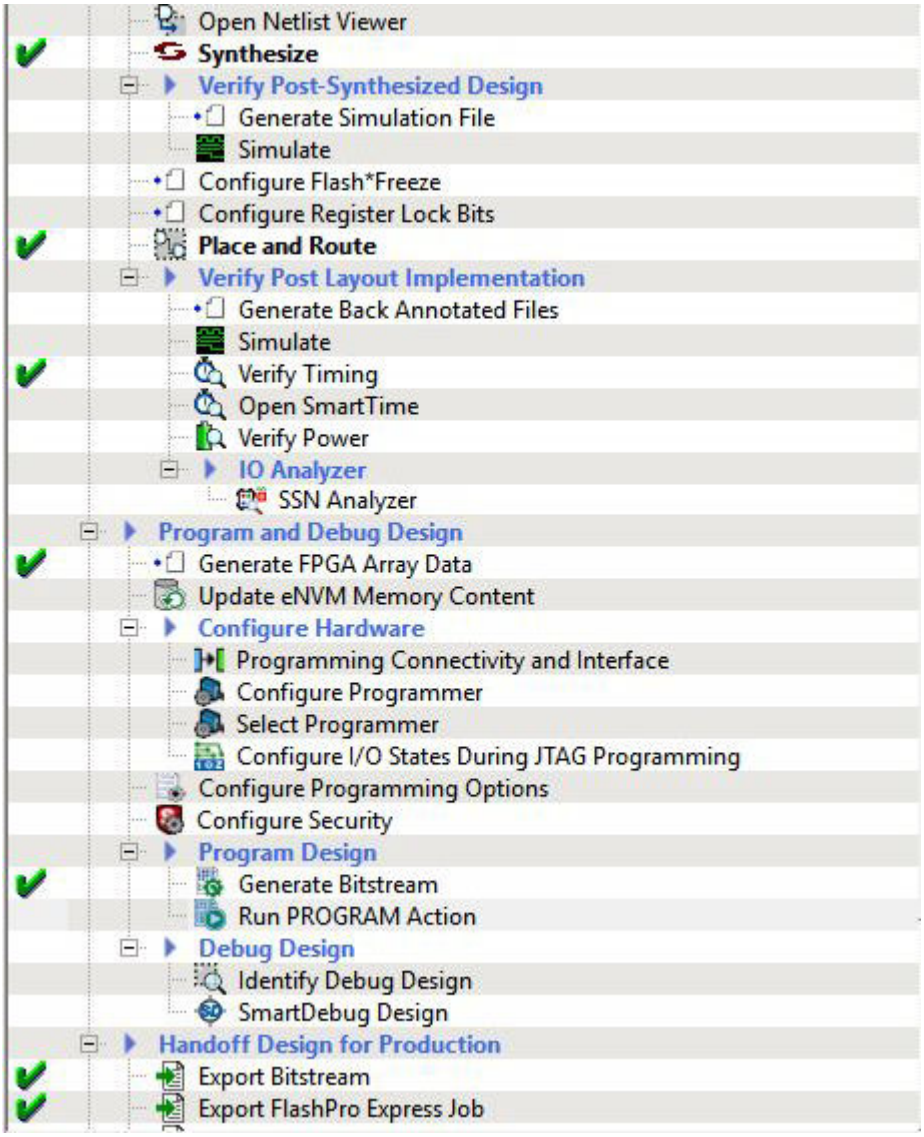
2. Libero Design Flow

This chapter describes the Libero design flow of the demo design. The Libero design flow involves the following steps:

- Synthesize
- Place and route
- Verify Timing
- Generate Bitstream
- Run PROGRAM Action

The following figure shows these options in the Design Flow tab.

Figure 2-1. Libero Design Flow Options



2.1 Synthesize

Perform the following steps to synthesize the design:

1. From the **Design Flow** window, double click **Synthesize**.
   A green tick mark appears when the synthesis is successful, as shown in Figure 2-1.
2. Right click **Synthesize** and select **View Report** to view the synthesis report and log files in the Reports tab.

2.2 Place and Route

1. From the **Design Flow** window, double click **Place and Route**.
   A green tick mark appears when the place and route is successful, as shown in Figure 2-1.
2. Right click **Place and Route** and select **View Report** to view the place and route report and log files in the **Reports** tab.

2.3 Verify Timing

To verify timing, perform the following steps:

1. From the **Design Flow** window, double click **Verify Timing**.
   When the design successfully meets the timing requirements, a green tick mark appears, as shown in Figure 2-1.
2. Right click **Verify Timing** and select **View Report** to view the verify timing report and log files in the **Reports** tab.

2.4 Generate FPGA Array Data

To generate FPGA array data, double click **Generate FPGA Array Data** from the **Design Flow** window.

A green tick mark is displayed after the successful generation of the FPGA array data, as shown in Figure 2-1.

2.5 Generate Bitstream

Perform the following steps to generate the bitstream:

1. Double click **Generate Bitstream** from the **Design Flow** tab.
   When the bitstream is successfully generated, a green tick mark appears, as shown in Figure 2-1.
2. Right click **Generate Bitstream** and select **View Report** to view the corresponding log file in the **Reports** tab.

2.6 Run PROGRAM Action

After generating the bitstream, the PolarFire device must be programmed. Perform the following steps to program the PolarFire device:

1. Ensure that the following Jumper Settings are set on the board.

Table 2-1. Jumper Settings

Jumper	Description	Default
J18, J19, J20, J21, and J22	Short pin 2 and 3 for programming the PolarFire FPGA through FTDI	Closed
J28	Short pin 1 and 2 for programming through the on-board FlashPro5	Open
J26	Short pin 1 and 2 for programming through the FTDI SPI	Closed
J4	Short pin 1 and 2 for manual power switching using SW3	Closed
J12	Short pin 3 and 4 for 2.5 V	Closed

2. Connect the power supply cable to the J9 connector on the board.
3. Connect the USB cable from the Host PC to J5 (FTDI port) on the board.

4. Power the board using the SW3 slide switch.
5. Double click **Run PROGRAM Action** from the **Libero** > **Design Flow tab**.
   A green tick mark appears when the device is programmed successfully, as shown in Figure 2-1.

3. Running the Demo

This chapter describes installing and using the Graphic User Interface (GUI) to run the TVS demo. The PolarFire TVS demo application is a simple GUI that runs on the host PC to communicate with the PolarFire Device.

Perform the following steps to install the GUI:

1. Extract the contents of the `mpf_an4682_v2022p1_eval_df.rar` file. From the `mpf_an4682_v2022p1_eval_df\GUI\TVS_Monitor_GUI_Installer` folder, double click the `setup.exe` file.
2. Follow the instructions displayed on the installation wizard.

After successful installation, TVS_Monitor_GUI appears on the **Start** menu of the host PC desktop.

Perform the following steps to run the TVS demo:

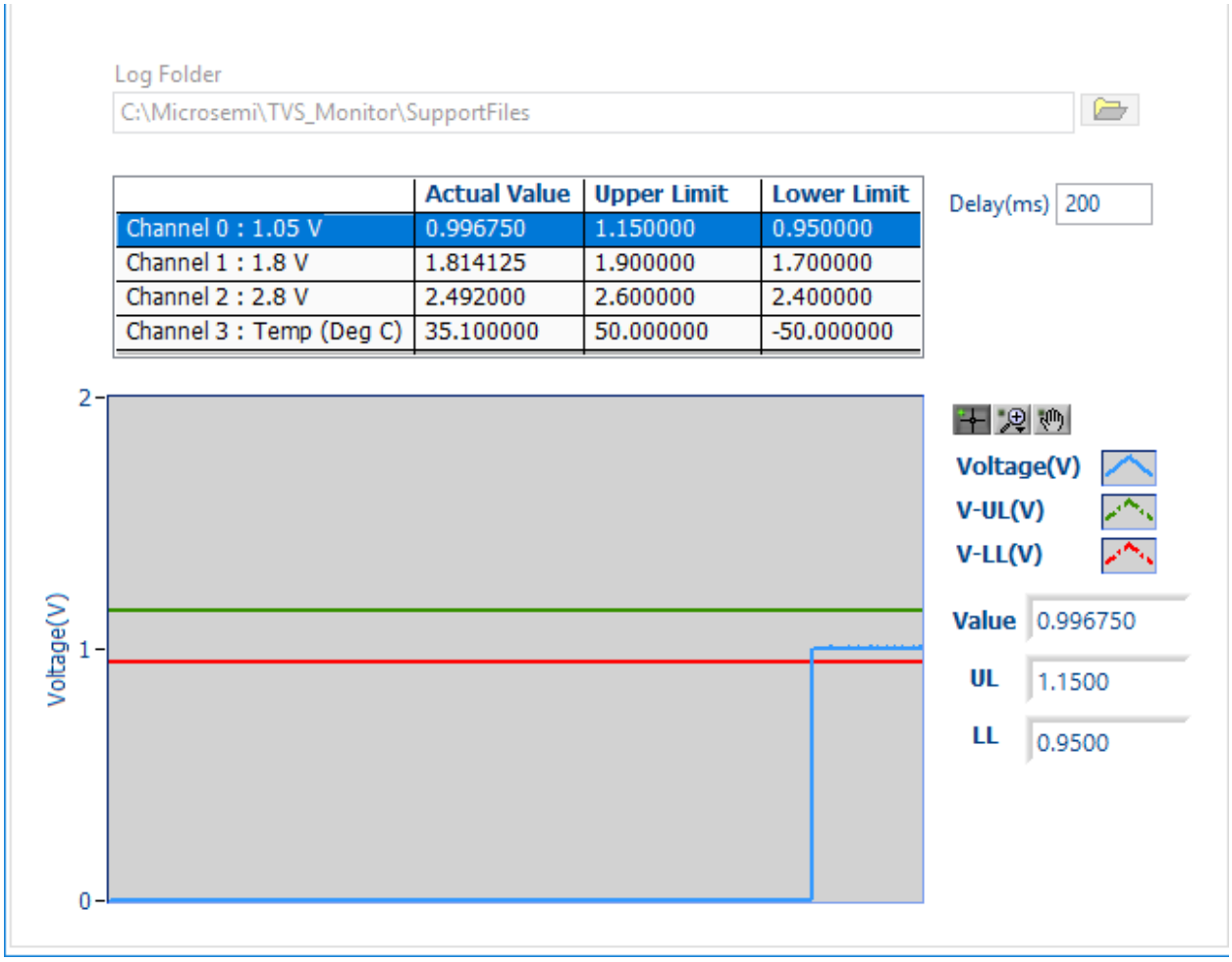
1. From the **Start** menu, click **TVS_Monitor_GUI** to launch the application. Ensure that the board is connected and appropriate Log Folder is selected.
2. Click **Connect**. On a successful connection, the GUI shows the temperature and voltage values. The Log file is created with the time stamp in the file name at the Log Folder location.
   By default, Log Folder points to the 'SupportFiles' folder in the installation directory. Users can modify the Log Folder location before connecting to the board.

Important: Ensure that the Log Folder is not a system-restricted location. In this case, the user must launch the GUI with admin privileges (right click and **run as admin**).

3. Upper Limit, Lower Limit, and the minimum variation in logging for each channel are configurable in the setup.ini file. Channel values are logged in the log file if a variation exceeds the specified 'min var' values in the setup.ini file.

The following figure shows the standard temperature and voltage values of channel 0 (1.05 V). The plot corresponds to the values of Channel 0. Similarly, select the other channels and view their corresponding values and plots.

Figure 3-1. Selecting COM Port and Connecting-Channel 0



Important: The GUI updates the TVS channel values with the delay entered in the Delay (ms) field.

4. Appendix 1: Programming the Device Using FlashPro Express

This chapter describes how to program the PolarFire device with the .job programming file using FlashPro Express. The .job file is available at the following design files folder location:

```
mpf_an4682_v2022p1_eval_df\Programming_Job
```

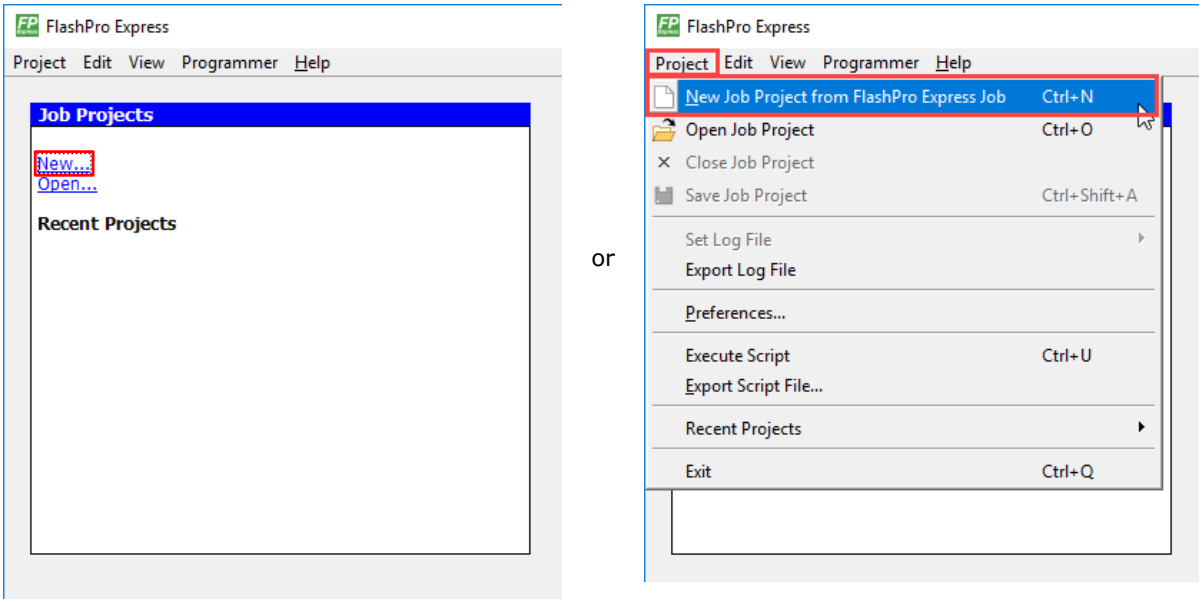
Perform the following steps to program the device:

1. Ensure that the jumper settings on the board are the same as listed in Table 2-1.

> **Important:** The power supply switch must be switched off while making the jumper connections.

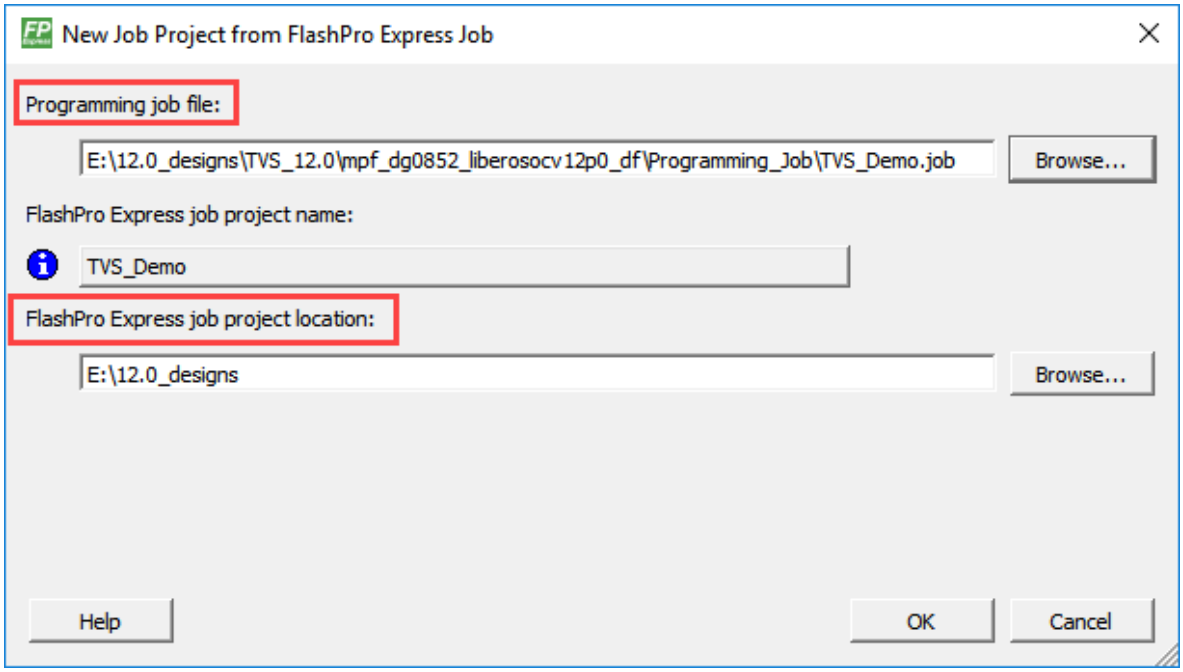
2. Connect the power supply cable to the J9 connector on the board.
3. Connect the USB cable from the Host PC to the J5 (FTDI port) on the board.
4. Power the board using the SW3 slide switch.
5. On the host PC, launch the **FlashPro Express** software.
6. Click **New** or select **New Job Project from FlashPro Express Job** from the **Project** menu to create a new job project, as shown in the following figures.

Figure 4-1. FlashPro Express Job Project



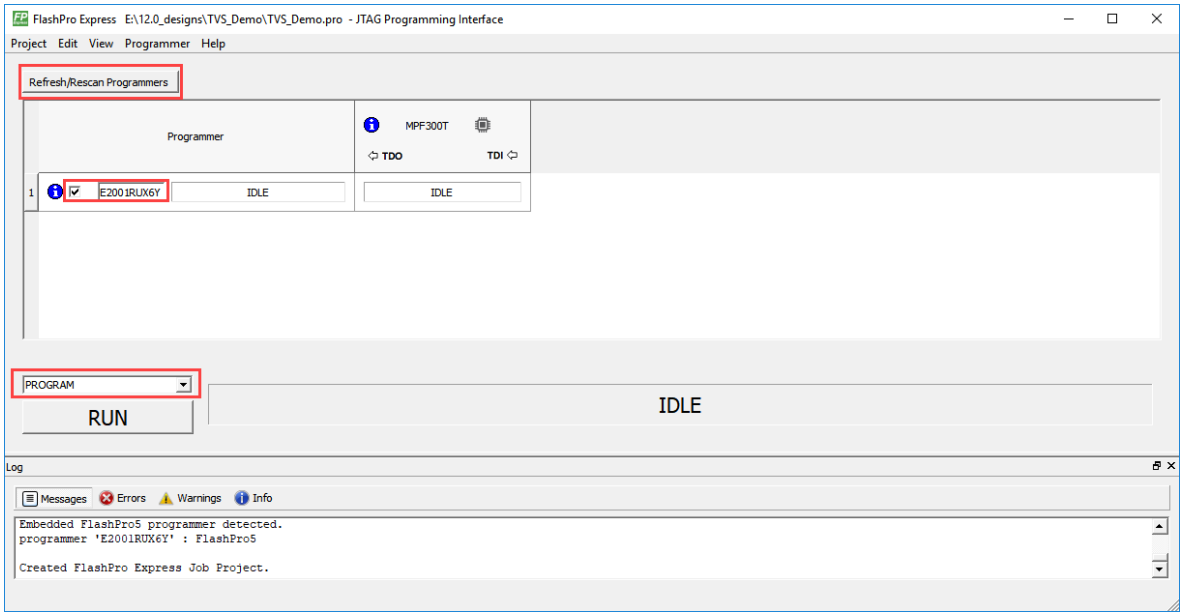
7. Enter the following in the **New Job Project from FlashPro Express Job** dialog box:
   - **Programming job file**: Click **Browse**, navigate to the location where the .job file is located, and select the file. The default location is: `<download_folder>\mpf_an4682_v2022p1_eval_df\Programming_Job`.
   - **FlashPro Express job project location**: Click **Browse** and navigate to the location where you want to save the project.

Figure 4-2. New Job Project from FlashPro Express Job



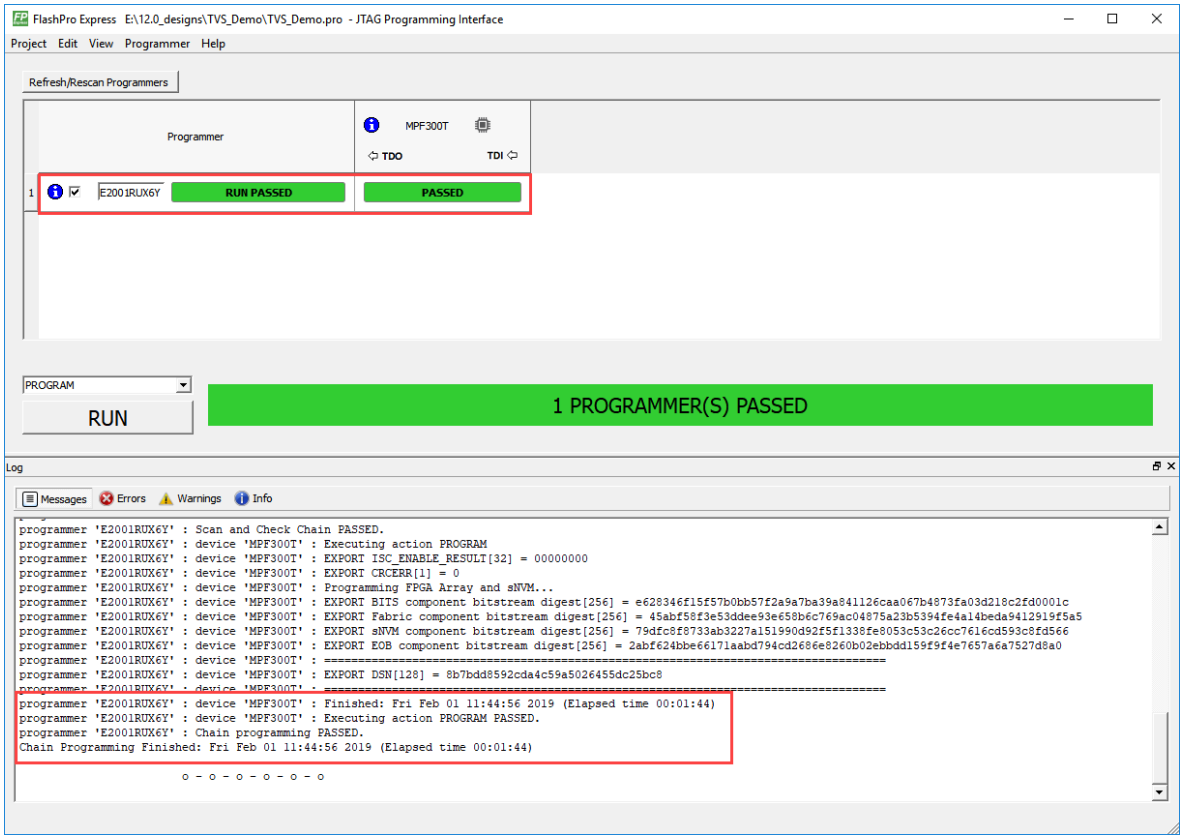
8. Click **OK**. The required programming file is selected and ready to be programmed in the device.
9. The FlashPro Express window appears as shown in the following figure. Make sure that a programmer number appears in the Programmer field. If not, check the board connections and click **Refresh/Rescan Programmers**.

Figure 4-3. Programming the Device



10. Click **RUN** to program the device. When the device is programmed successfully, a **RUN PASSED** status is displayed, as shown in the following figure. See 3. Running the Demo to run the TVS demo.

Figure 4-4. FlashPro Express-RUN PASSED



11. Close **FlashPro Express** or in the **Project** tab, click **Exit** in the **Project** tab.

5. Appendix 2: Running the TCL Script

TCL scripts are provided in the design files folder under the directory TCL_Scripts. If required, the design flow can be reproduced from Design Implementation to the job file generation.

Perform the following steps to run the TCL:

1. Launch the Libero software
2. Select **Project > Execute Script....**
3. Click **Browse** and select `script.tcl` from the downloaded TCL_Scripts directory.
4. Click **Run**.

After successful execution of TCL script, the Libero project is created within TCL_Scripts directory.

For more information about TCL scripts, refer to **mpf_an4682_v2022p1_eval_df/TCL_Scripts/readme.txt**.

Refer to Tcl Commands Reference Guide for more details on TCL commands. Contact Technical Support for queries encountered when running the TCL script.

6. Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Table 6-1. Revision History

Revision	Date	Description
A	07/2022	The following is the list of changes in revision A of the document: • The document was migrated to the Microchip template. • The document number was updated to DS00004682A from 50200852. • The document ID was updated to AN4682 from DG0852. • Updated the Figure 1-2. • Removed Resource Utilization section.
3.0	_	The following is a summary of the changes made in this revision. Added 5. Appendix 2: Running the TCL Script. Updated Figure 2, page 4. Updated Figure 1-3.
2.0	_	The following is a summary of the changes made in this revision. Updated the document for Libero SoC v12.2. Removed the references to Libero version numbers.
1.0	_	The first publication of this document.

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