MMA041AA Datasheet

DC–26 GHz GaAs MMIC Distributed Low-Noise Amplifier

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0

Revision 2.0 is the second publication of this document.

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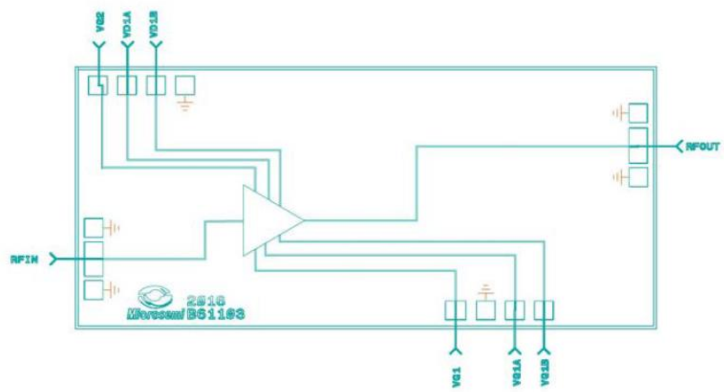
2 Product Overview

MMA041AA is a gallium arsenide (GaAs) monolithic microwave integrated circuit (MMIC) pseudomorphic high-electron mobility transistor (pHEMT) distributed amplifier die that operates between DC and 26 GHz. It is ideal for test instrumentation and communications infrastructure applications. The amplifier provides a flat gain of 18 dB, 3.2 dB noise figure, and 22 dBm of output power at 1 dBm gain compression. Output IP3 is typically 36 dBm. The MMA041AA amplifier features RF I/Os that are internally matched to 50 Ω, which allows for easy integration into multi-chip modules (MCMs). It is also available in packaged form as the MMA041PP5.

The following image shows the primary functional blocks of the MMA041AA device.

Figure 1 Functional Block Diagram



2.1 Applications

The MMA041AA device is designed for the following applications:

- Test and measurement instrumentation
- Electronic warfare (EW), electronic countermeasures (ECM), and electronic counter-countermeasures (ECCM)
- Military and space
- Telecom infrastructure
- Wideband microwave radios
- Microwave and millimeter-wave communication systems

2.2 Key Features

The following are key features of the MMA041AA device:

- Frequency range: DC to 26 GHz
- High gain: 18 dB
- High output IP3: 36 dBm
- Low noise figure: 3.2dB
- Supply voltage: 7 V at 150 mA
- 50 Ω matched I/O
- Compact die size: 3 mm × 1.30 mm × 0.1 mm

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings at 25 °C unless otherwise specified.

Table 1 Absolute Maximum Ratings

Parameter	Rating
Storage temperature	–65 to 150 °C
Operating temperature	–55 to 85 °C
Drain bias voltage, (V_D)	8 V
First gate bias voltage, (V_{G1})	–2 to 0.5 V
Second gate bias voltage, (V_{G2})	V_D +/- 20%
V_D current (I_{DD})	300 mA
RF input power	19 dBm
DC power dissipation (T = 85 °C)	2.4 W
Channel temperature	150 °C
Thermal impedance	18 °C/W

3.2 Typical Electrical Performance

The following table lists the specified electrical performance of the MMA041AA device at 25 °C, where VDD is 7 V, IDD is 150 mA, and VGG is –0.4 V.

Table 2 Specified Electrical Performance

Parameter	Frequency Range	Min	Typ	Max	Units
Operational frequency range		DC		26	GHz
Gain	DC-6 GHz	18	20		dB
	6 GHz-12 GHz	18	18.5		dB
	12 GHz-20 GHz	17	18		dB
Gain flatness	4 GHz-12 GHz		± 0.5		dB
	12 GHz-20 GHz		± 0.25		dB
Noise figure	DC-6 GHz		2.7		dB
	6 GHz-12 GHz		2		dB
	12 GHz-20 GHz		2.5		dB
Input return loss	DC-6 GHz		17		dB
	6 GHz-12 GHz		20		dB
	12 GHz-20 GHz		20		dB
Output return loss	DC-6 GHz		12		dB
	6 GHz-12 GHz		16		dB
	12 GHz-20 GHz		16		dB
P1dB	DC-6 GHz	22	22.5		dBm
	6 GHz-12 GHz	21	22		dBm
	12 GHz-20 GHz	18	20		dBm
Psat	DC-6 GHz		24		dBm
	6 GHz-12 GHz		24		dBm
	12 GHz-20 GHz		22		dBm
OIP3	DC-6 GHz		35		dBm
	6 GHz-12 GHz		34		dBm
	12 GHz-20 GHz		36		dBm
V_{DD} (drain voltage supply)			7		V
I_{DD} (drain current)			150		mA
V_{GG} (gate voltage supply)		-1.0	-0.4	0	V

3.3 Typical Performance Curves

The following graphs show the typical performance curves of the MMA041AA device at 25 °C, unless otherwise indicated.

Figure 2 Gain vs. Temperature (V_{DD} = 7v, I_{DD} = 150mA)

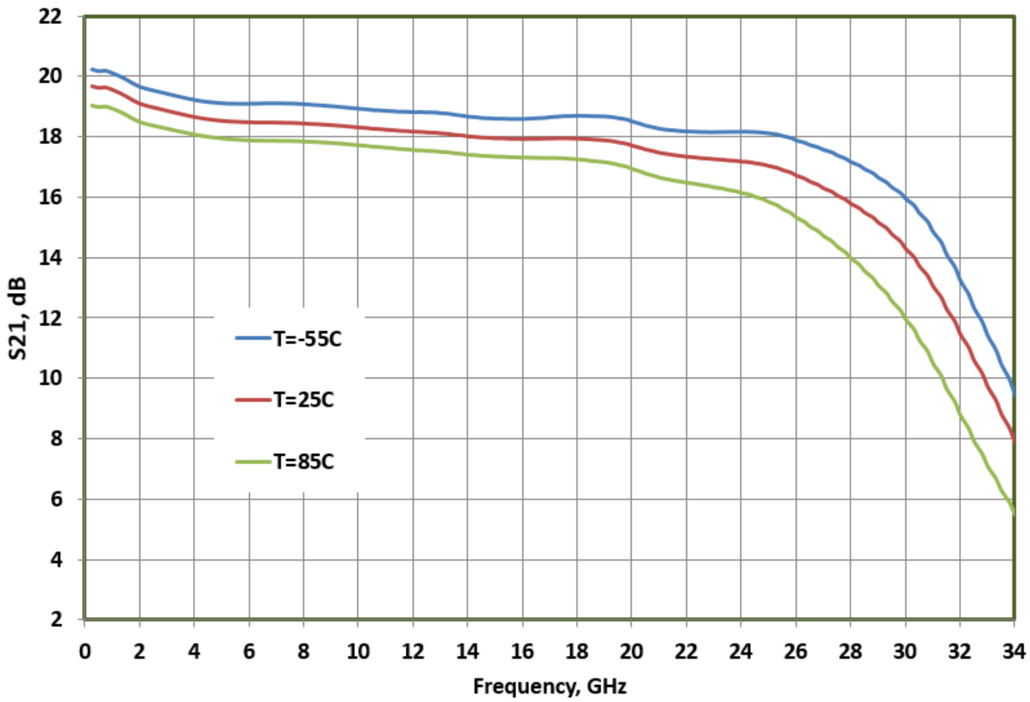


Figure 3 Gain vs V_{DD} (I_{DD} = 150mA, T = 25C)

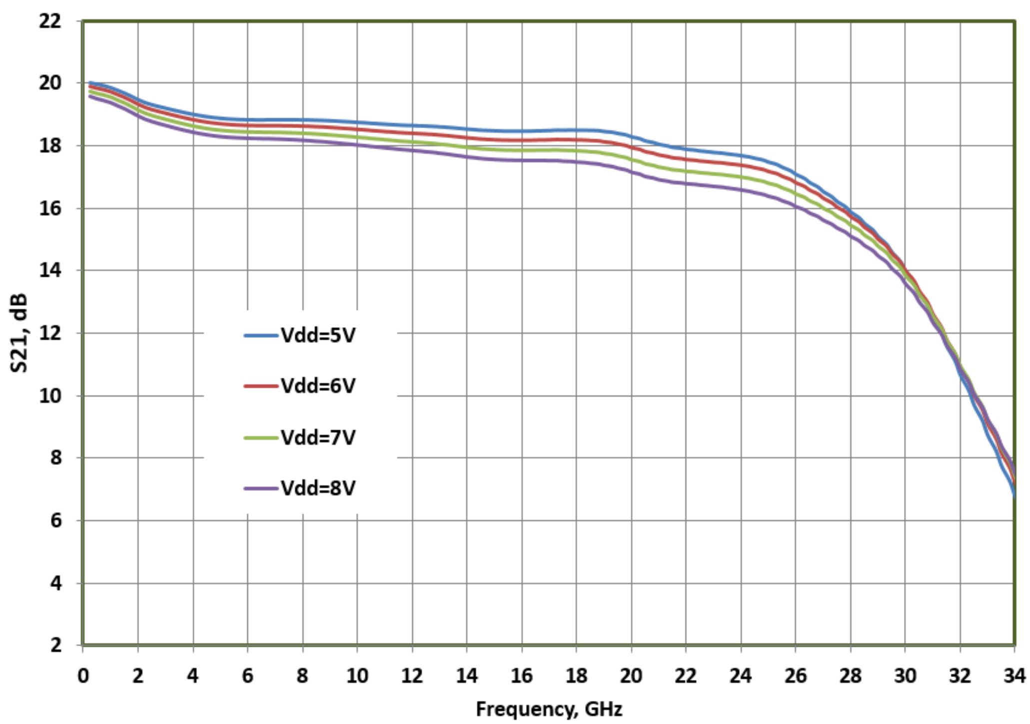


Figure 4 S_{11} vs Temperature (V_{DD} = 7v, I_D = 150mA)

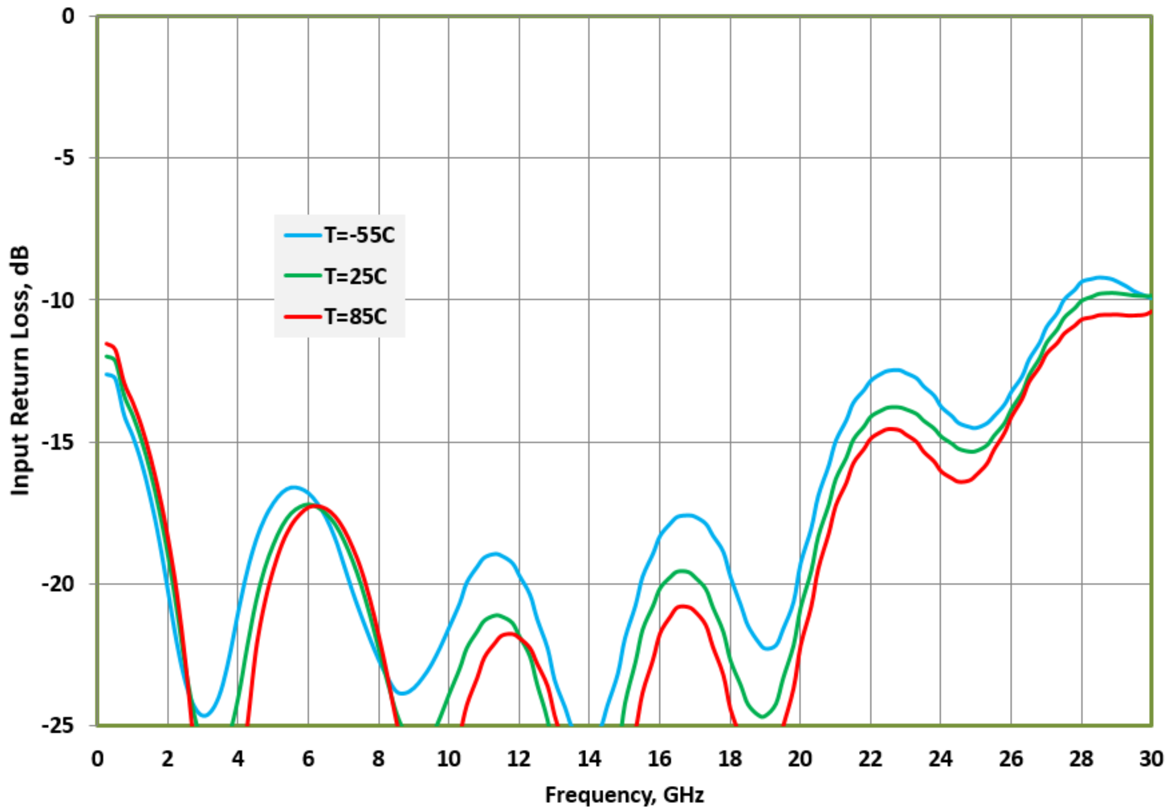


Figure 5 S_{22} vs Temperature (V_{DD} = 7v, I_D = 150mA)

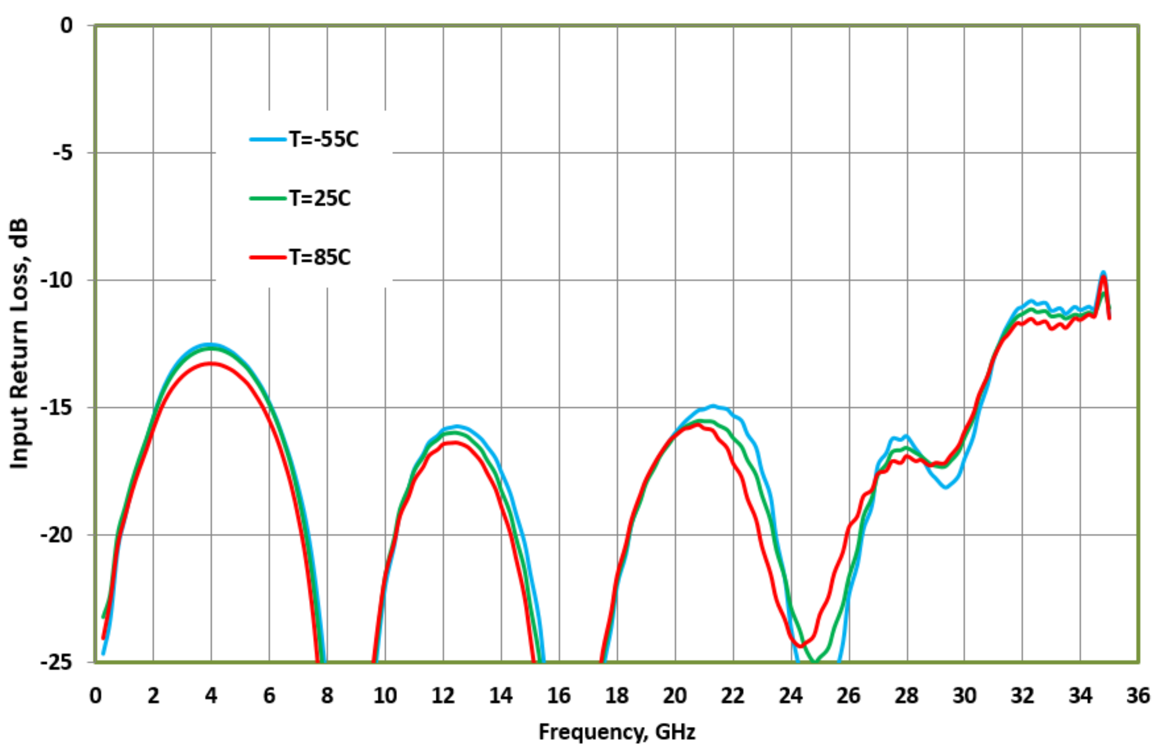


Figure 6 Noise Figure vs. Temperature (V_{DD} = 7v, I_{DD} = 150mA)

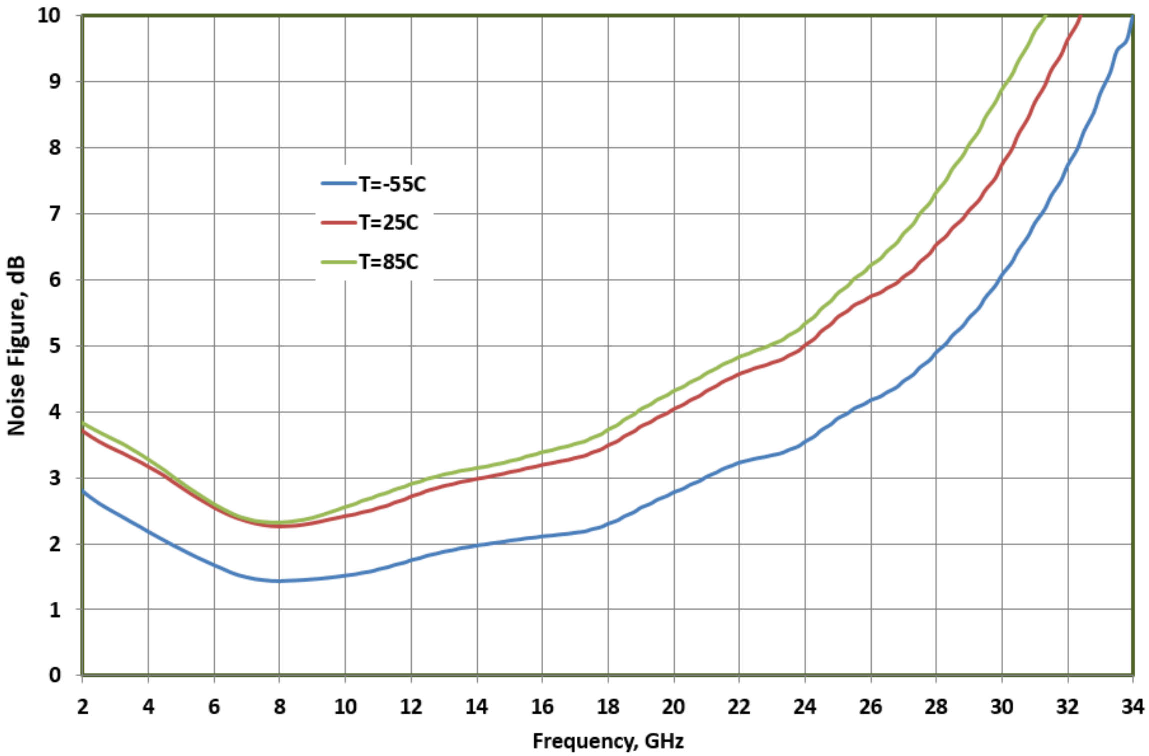


Figure 7 Noise Figure vs Drain Voltage (I_{DD} = 150mA, T = 25C)

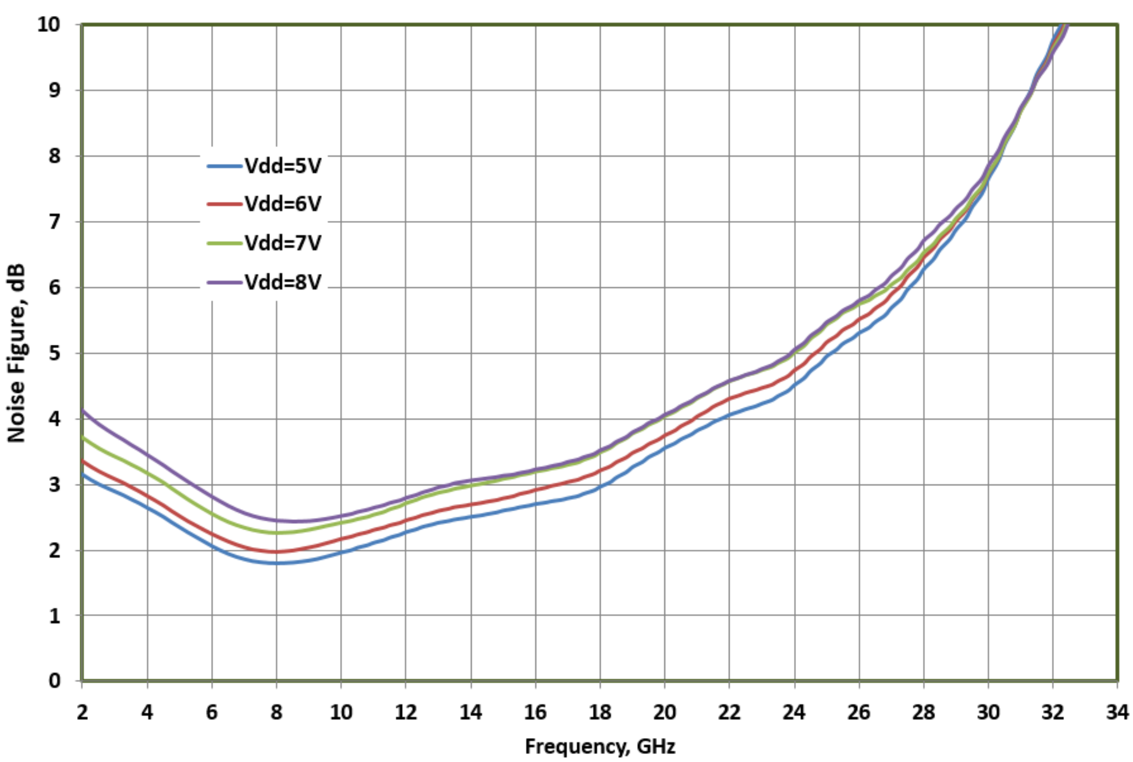


Figure 8 P1dB vs Temperature (V_{DD} = 7v, I_{DD} = 150mA)

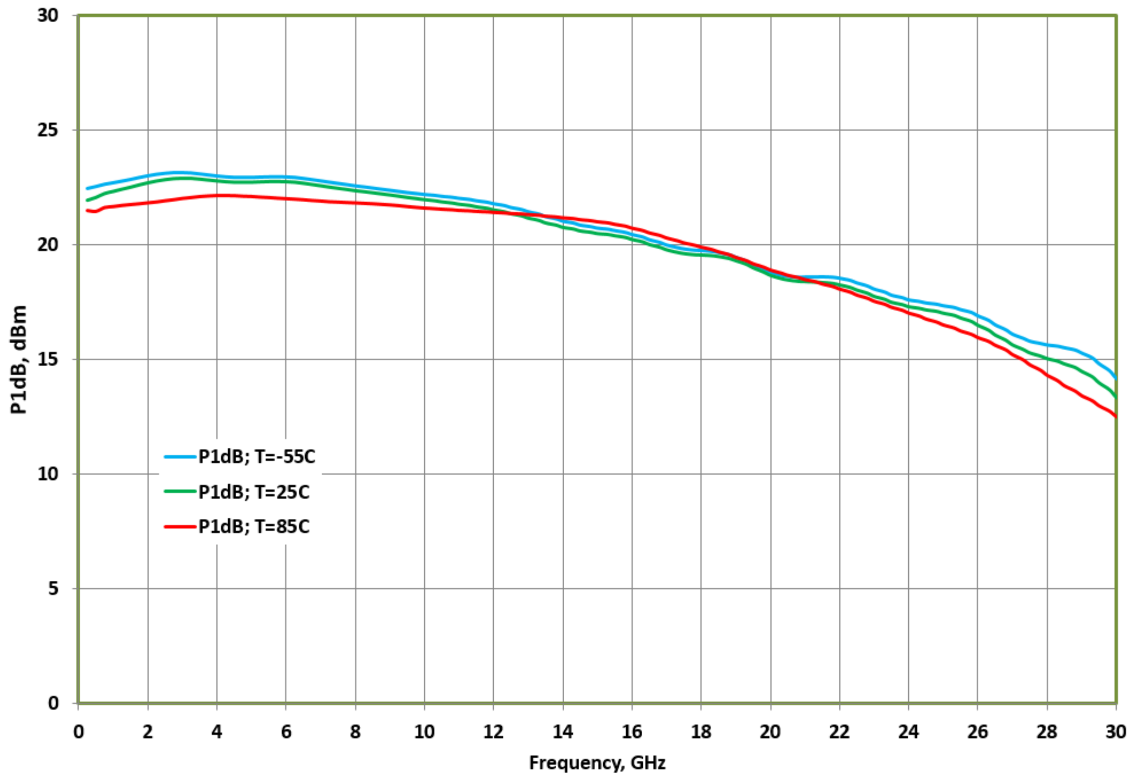


Figure 9 P3dB vs Temperature (V_{DD} = 7v, I_{DD} = 150mA)

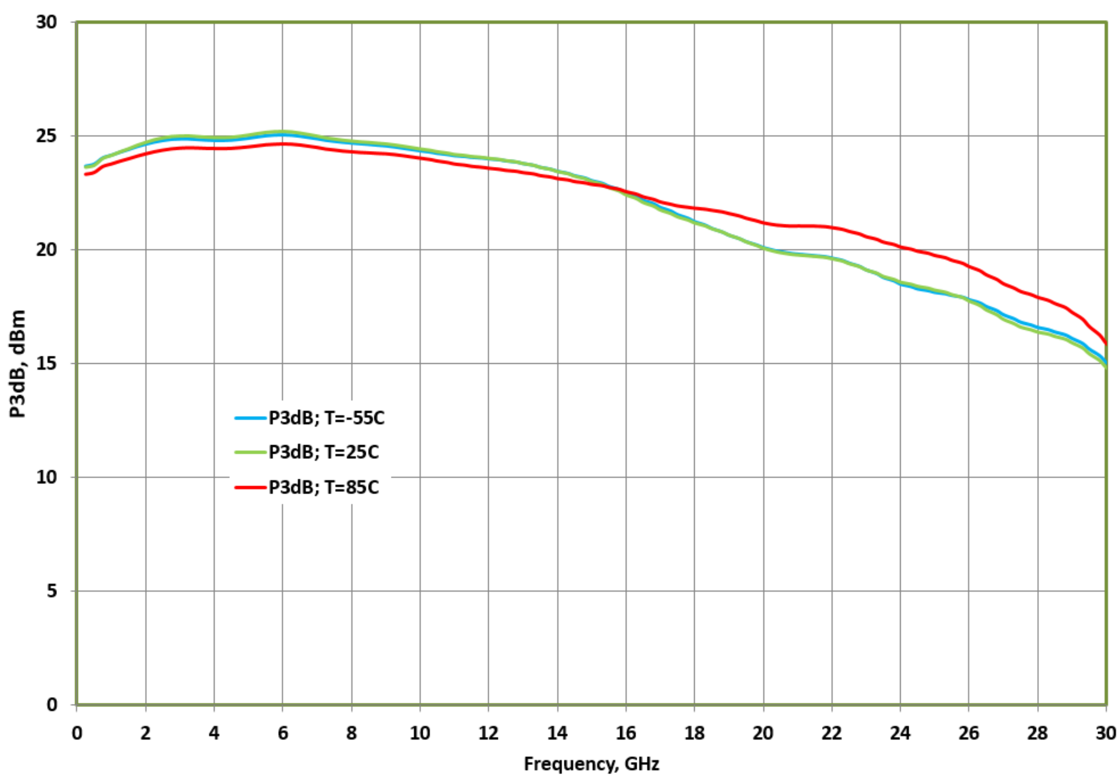


Figure 10 OIP3 vs. Temperature (V_{DD} = 7v, T = 25C)

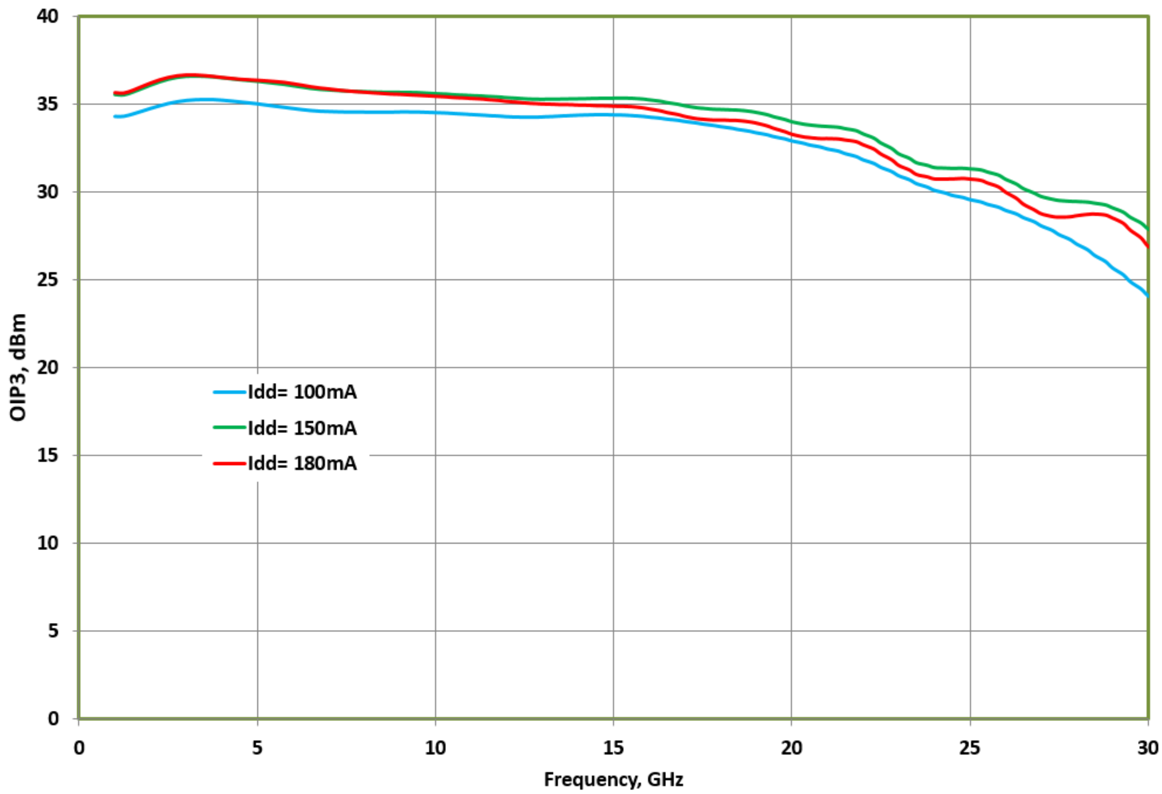
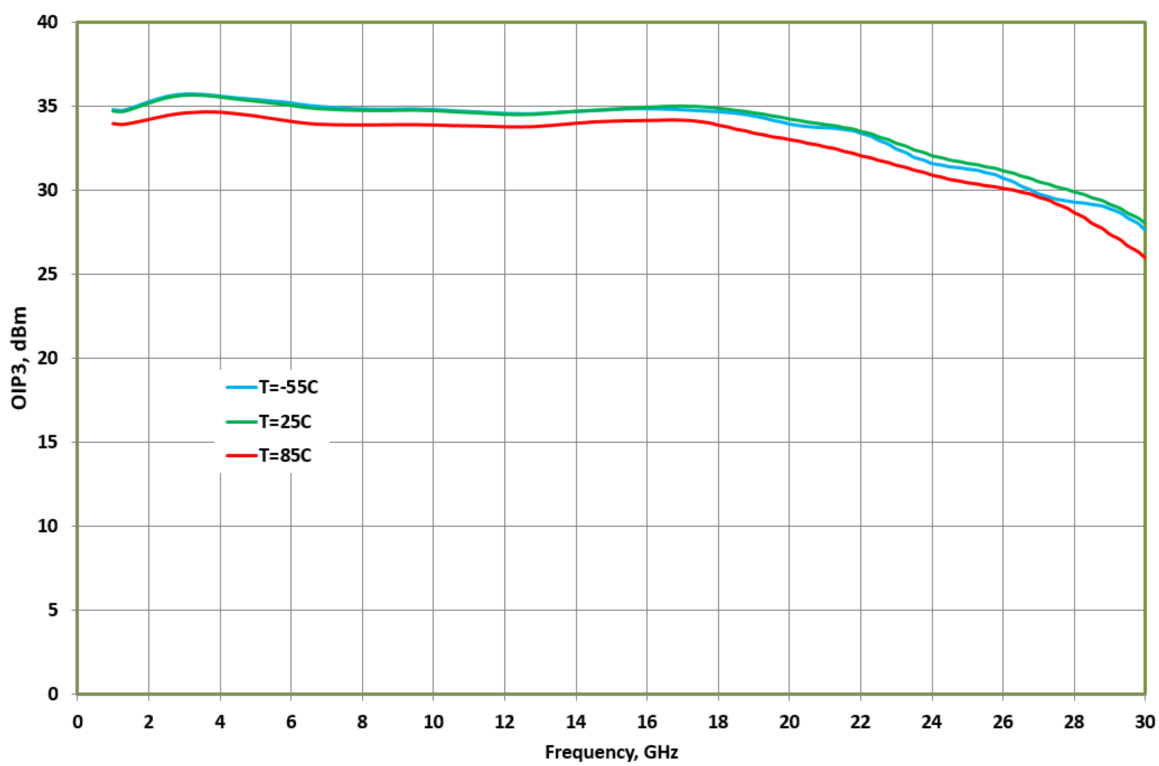


Figure 11 OIP3 vs. Current (V_{DD} = 7v, T = 25C)

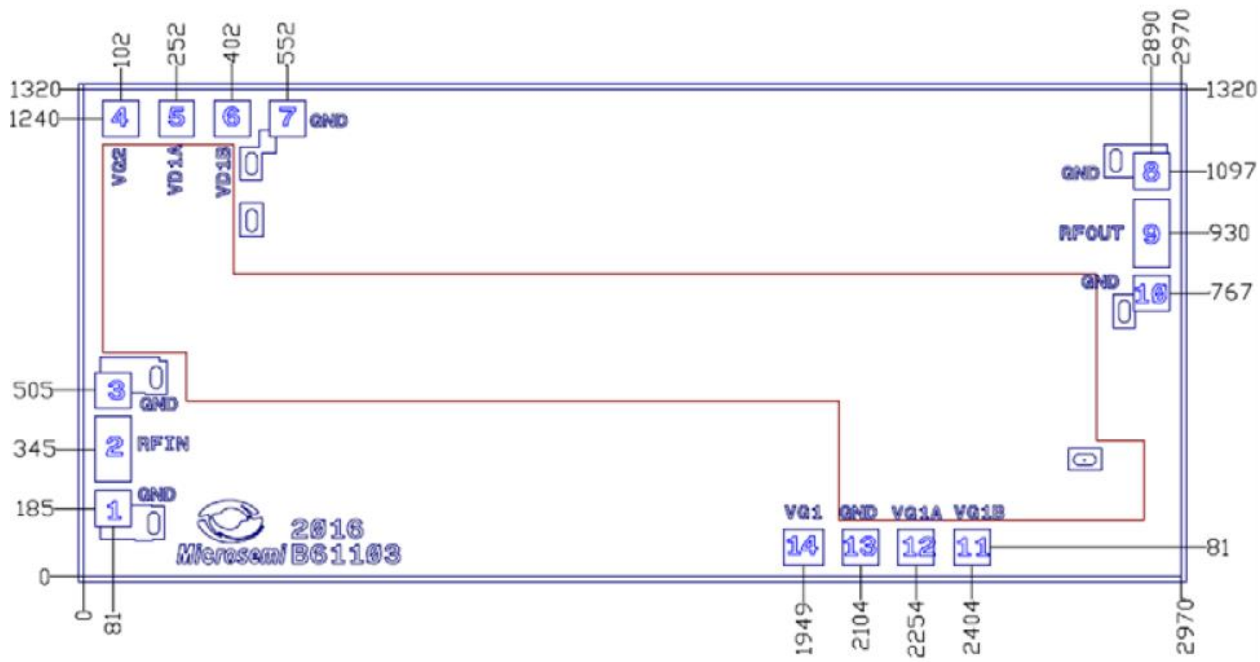


4 Chip Outline Drawing, Die Packaging, Bond Pad, and Assembly Information

4.1 Chip Outline Drawing

The following illustration shows the chip outline of the MMA041AA device. Dimensions are in µm and are relative to the zero datum locations shown in the drawing. The minimum bond pad size is 100 µm × 100 µm. Both the bond pad surface and the backside metal are 3 µm gold. The die thickness is 100 µm. The backside is the DC/RF ground. The airbridge keepout region is in crosshatch, and the unlabeled pads should not be bonded.

Figure 15 Chip Outline



4.2 Die Packaging Information

The following table shows the chip outline of the MMA041AA device. For additional packaging information, contact your Microsemi sales representative.

Table 3 Packaging Information

Standard Format	Option Format
Waffle Pack	Gel Pack
50-100 pieces per pack	50 pieces per pack

4.3 Bond Pad Information

The following table describes the pads of the MMA041AA device.

Table 4 Pad Description

Pad Number	Pin Name	Description
2	RFIN	This pad is DC-coupled and matched to 50 Ω.
9	RFOUT + VDD	This pad is matched to 50 Ω and is used to bias VDD.
14	VG1	Gate control for amplifier. Adjust to achieve IDD = 150 mA.
5, 6	VD1A, VD1B	Low-frequency termination. Connect bypass capacitors per application circuit below. (no bias necessary)
4, 12, 11	VG2, VG1A, VG1B	Low-frequency termination. Connect bypass capacitors per application circuit below. (no bias necessary)
1, 3, 7, 8, 10, 13	GND	Die bottom must be connected to RF/DC ground.
Backside paddle	RF/DC GND	RF/DC ground.

4.4 Assembly Diagram

The following illustration shows the application circuit of the MMA041AA device.

Figure 12 Assembly Diagram

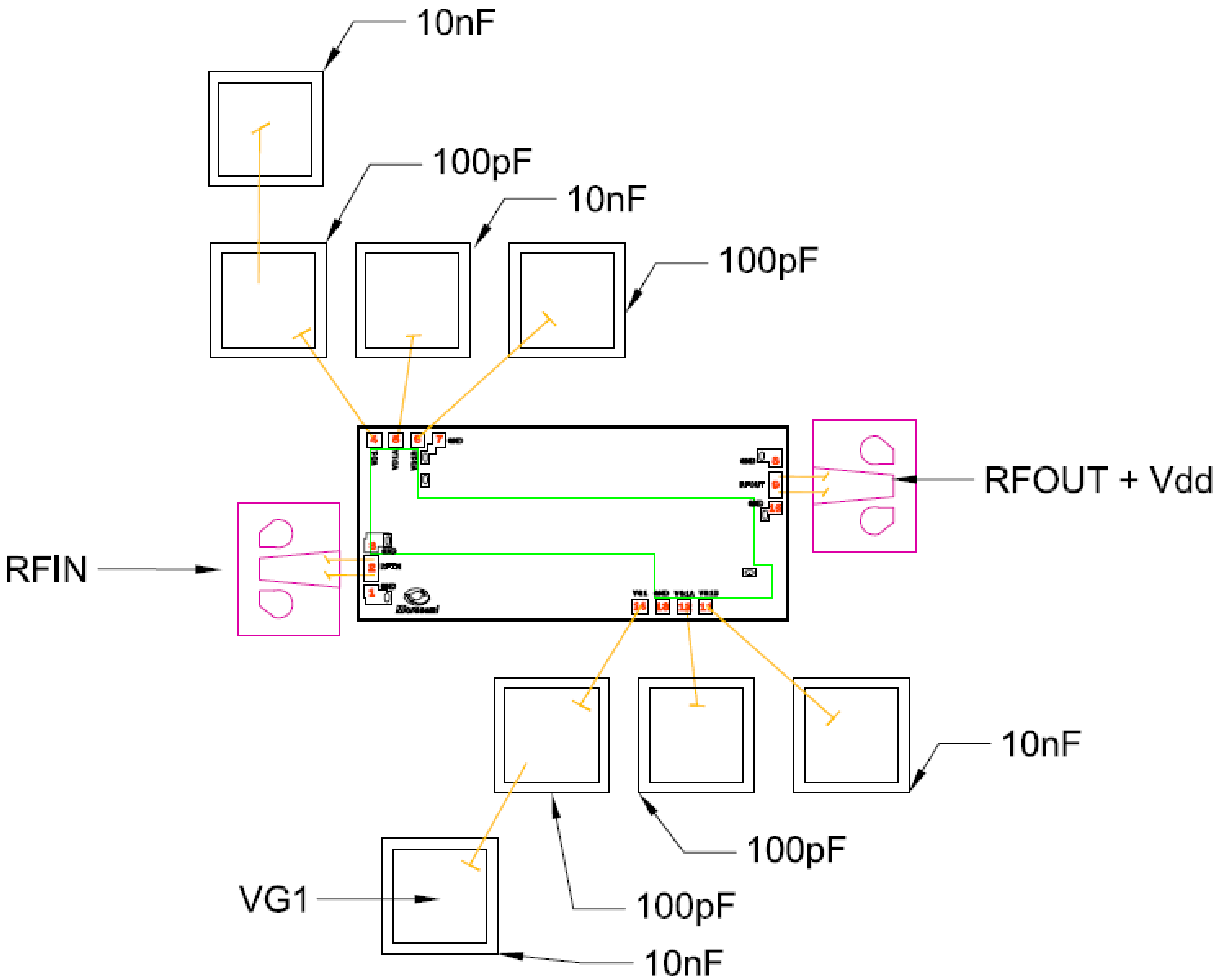


Table 5 Bias Sequence

Bias Sequence
1) Set the gate voltage VG1 to -1V
2) Set drain voltage VDD to 7V
3) Adjust the gate voltage until the drain current is 150mA

5 Handling Recommendations

Gallium arsenide integrated circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. It is recommended to follow all procedures and guidelines outlined in the Microsemi application note AN01 GaAs MMIC Handling and Die Attach Recommendations.

6 Ordering Information

The following table shows the ordering information for the MMA041AA device.

Table 6 Ordering Information

Part Number	Package
MMA041AA	Die