LX7720 Daughter Board User's Manual

Introduction

The LX7720 provides four half-bridge drivers with floating current sense for motor coil driving, six bi-level inputs for position sensing, and a resolver to digital interface with primary coil driver. The LX7720 supports a ground potential difference between the motor and signal grounds of up to 10V and motor supply voltages up to 60V.

When used with an FPGA or MCU controller, the LX7720 provides a complete open- or closed-loop motor driver with coil current feedback and rotation or linear position sensing for stepper motors, brushless DC and permanent magnet motors.

Position sensing supports encoders, hall sensors, resolvers, synchros, and LVDTs. Resolver carrier frequencies from 360Hz to 20kHz are supported. FPGA IP modules are available to support motor driving functions from open loop cardinal step driving to space vector modulation using field oriented control.

The LX7720 contains 7 sigma delta modulators for analog acquisition. Sinc filtering and decimation is performed in the FPGA or MCU controller. Four modulators sample the voltage across floating current sense inputs. The remaining three modulators sample differential analog inputs such as the filtered drive waveform and output waveforms of a resolver.

The LX7720 daughter board uses an FMC connector for plug-in connection to the RTG4 FPGA DEV-KIT (Figure 1) and PolarFire FPGA MPF300-EVAL-KIT (Figure 2 on page 2) development boards. A 40-way header provides the same signals for connection to other boards such as the ProASIC3 FPGA Starter Kit (Figure 3 on page 2), the SAMRH71F20 MCU Evaluation Kit (Figure 4 on page 2), and the SAMV71Q21RT MCU SAM V71 Xplained evaluation kit.

Kit Contents

- LX7720 evaluation board SOL-12-000003-11 with soldered-in-place LX7720-ES engineering sample
- Engineering sample (-ES marking suffix) explanation sheet
- 24V 1.5A universal input AC adapter
- 20x 0.1" pitch shorting jumpers
- 4x 2-position 5mm pitch terminal block sockets, EB9A-02-C or equivalent to mate J12, J18, J30, and J31
- 4-position 5mm pitch terminal block sockets, OSTTJ047150 or equivalent, to mate J9
- 3-position Molex 50-57-9403 2.54mm pitch wire housing latching header to mate J13
- 6-position Molex 50-57-9406 2.54mm pitch wire housing latching header to mate J14
- 8-position Molex 50-57-9408 2.54mm pitch wire housing latching header to mate J15
- 20x Molex 16-02-0096 crimp sockets to suit 24 - 30AWG wire, for J13, J14, and J15 housings
- USB stick with documentation (see section 1 on page 3)

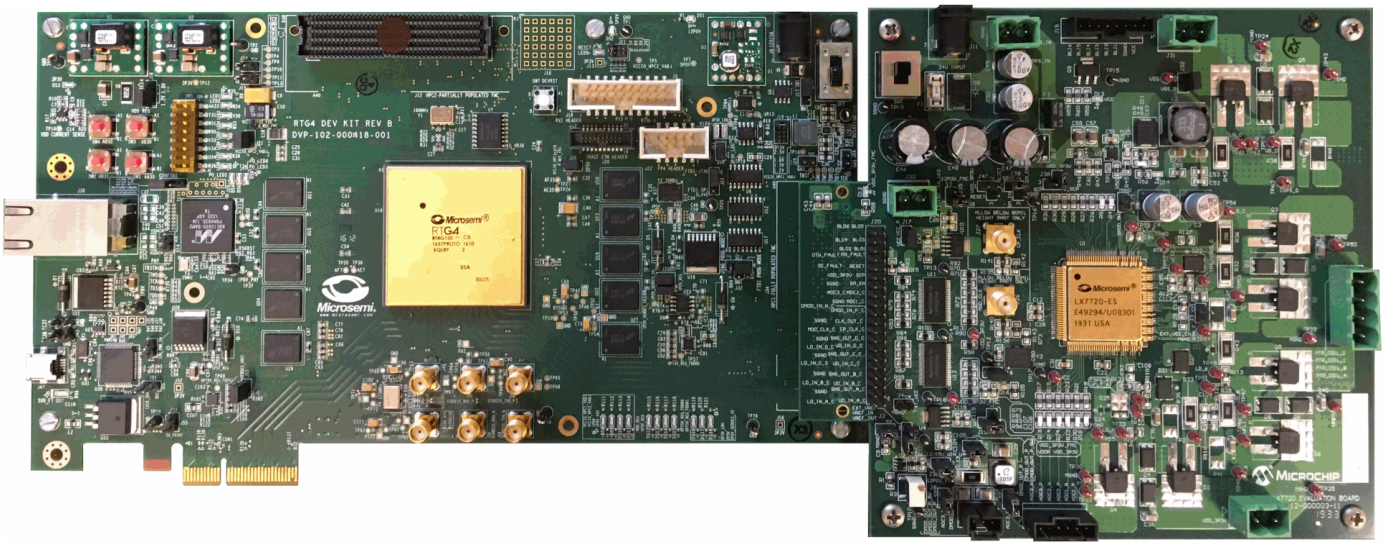


Figure 1. LX7720 Daughter Board Connected to RTG4 DEV-KIT using the FMC Connector

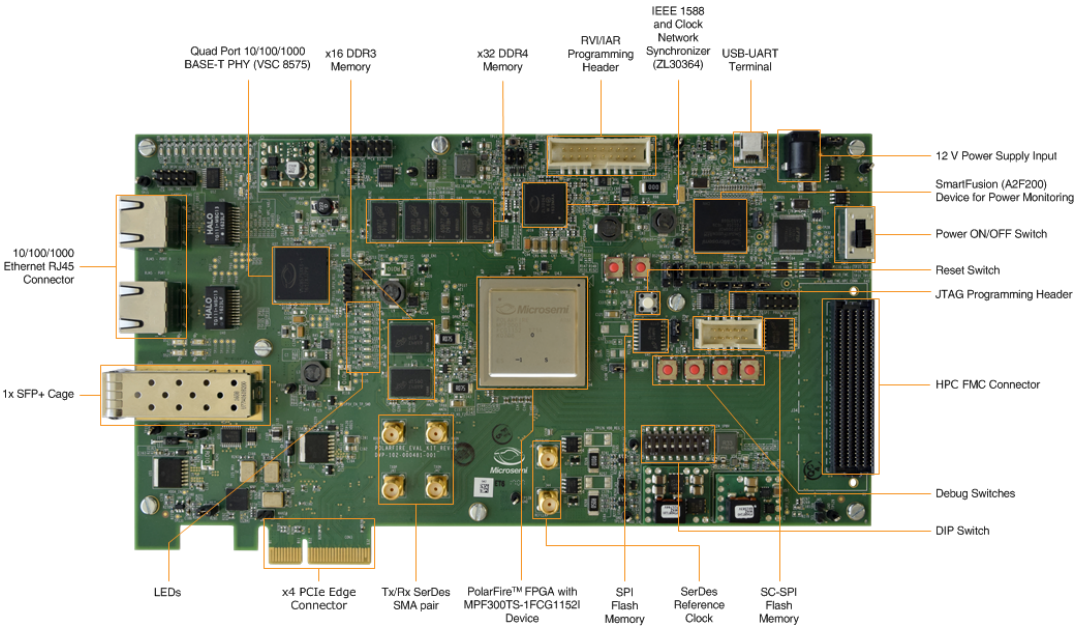


Figure 2. PolarFire MPF300-EVAL-KIT Evaluation Kit Board with 300K LE PolarFire FPGA in an FCG1152 Package

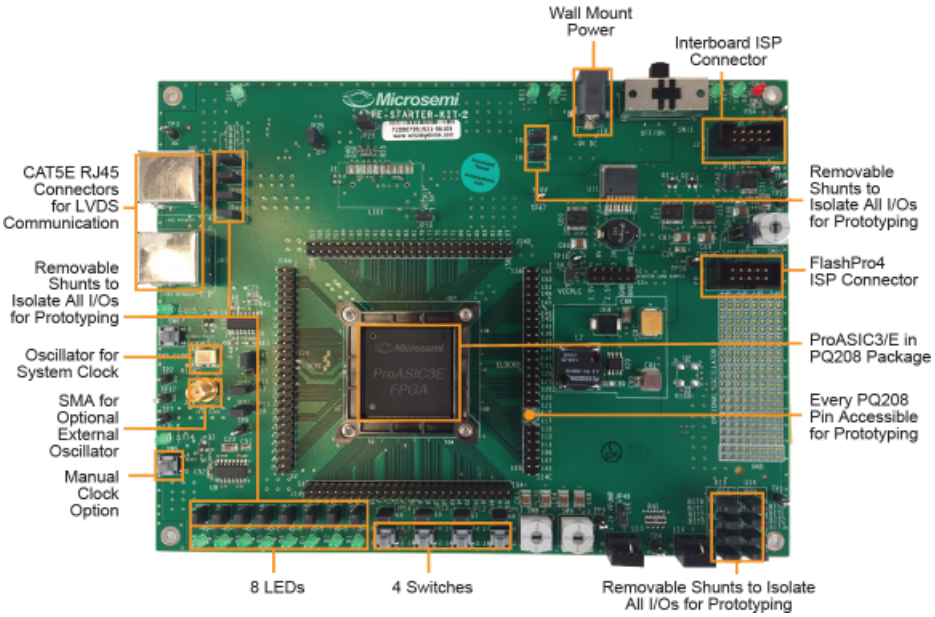
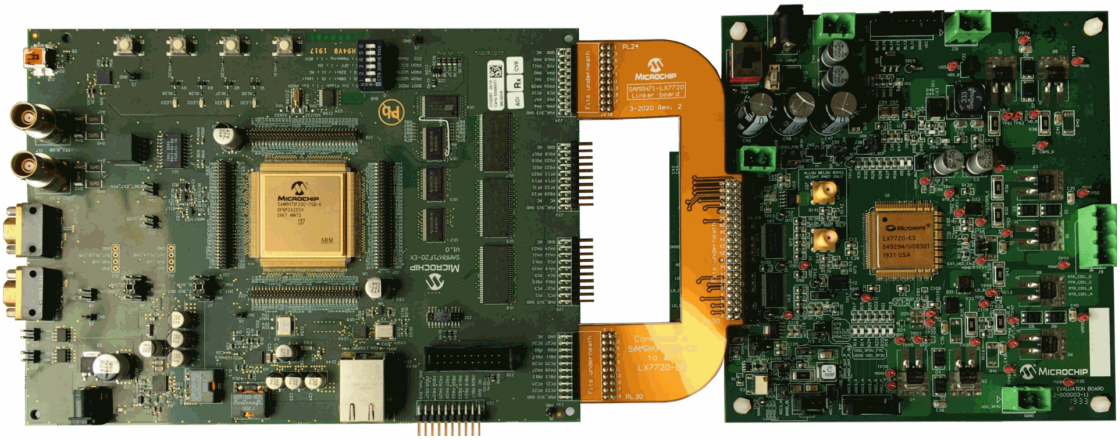


Figure 3. ProASIC3E Starter Kit with A3PE1500-PQ208 FPGA



Contact factory to obtain a flexible circuit to connect a SAMRH71F20-EK to the LX7720 daughter board as shown on the left

Figure 4. SAMRH71F20-EK Evaluation Kit with SAMRH71F20 Arm Cortex M7 (100MHz/200Dmips) microcontroller

1 Documentation and Support

The USB stick included with the LX7720 daughter board includes the following:

- RTG4 targeted binaries and Libero projects for the following motor control systems:
  - BLDC motor with resolver
  - BLDC motor, sensorless
  - Stepper motor
- GUI binaries and source for sensorless or resolver-feedback BLDCs (BLDC motor v4.1) and stepper motors (Stepper motor v1.0) for the setup of LX7720 daughter board connected to RTG4 Development Board
  - GUIs use the National Instruments Labview run-time engine, installer included on USB stick
  - GUIs use the FTDI USB driver to connect to the FT4232 USB interface on the RTG4 development board, installer included on USB stick
- Altium schematic and PCB files
- FPGA IP user guides on the USB stick are from https://www.microsemi.com/applications/motor-control#ip-suite. The Microsemi Libero library offers IP for use with LX7720 that can be downloaded with the Libero license. Further information is available at https://www.microsemi.com/applications/motor-control#resources
- For application support of radiation hardened mixed signal components such as LX7720, email AMSTech@microsemi.com
- For application support of radiation hardened FPGAs such as RTG4 and PolarFire, please register at the Microsemi SoC Customer Portal. Once registered and logged in, open a case with FPGA Technical Support

2 LX7720 Daughter Board to RTG4 Development Kit Setup Example

These instructions cover driving a BLDC (with or without a resolver) to a combined LX7720-RTG4 system using the included RTG4 firmware and GUI.

2.1 GUI Driver Software Installation

- Install the National Instruments Labview run-time engine
- Install the FTDI USB driver

2.2 RTG4 Hardware Connections

- Connect the LX7720 daughter board to the RTG4 board through the FMC connectors (Figure 1 on page 1)
- Check that the power slide switch on the RTG4 board is off (bottom/down position)
- Check that the power slide switch on the LX7720 board is off (top/up position)
- Power the RTG4 board with its 12V output AC adaptor, and the LX7720 board with its 24V output AC adaptor (Figure 5 below)
- Connect the RTG4 Development Kit to your host PC through a USB cable
- Connect a BLDC motor to connectors J9 on the LX7720 board (section 4.13 on page 16 has connection details)
  - The Trinamic QBL4208-41-04-006 24V, 8 phase, 3 pole BLDC motor was used to develop the RTG4 programming
- Connect optional resolver to connectors J13 and J14 on the LX7720 board if desired (section 4.13 on page 16 has connection details)
  - The AMCI R11X-A10/7 resolver was used to develop the RTG4 programming
- Turn on the power switches on the RTG4 board and the LX7720 daughter board

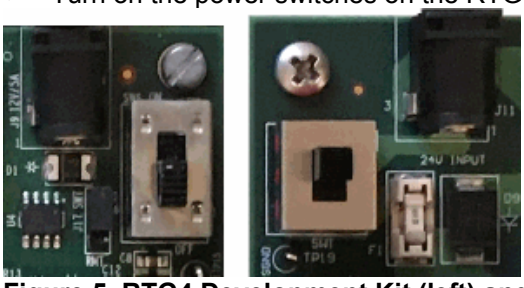


Figure 5. RTG4 Development Kit (left) and LX7720 Daughter Board (right) power switches in OFF positions

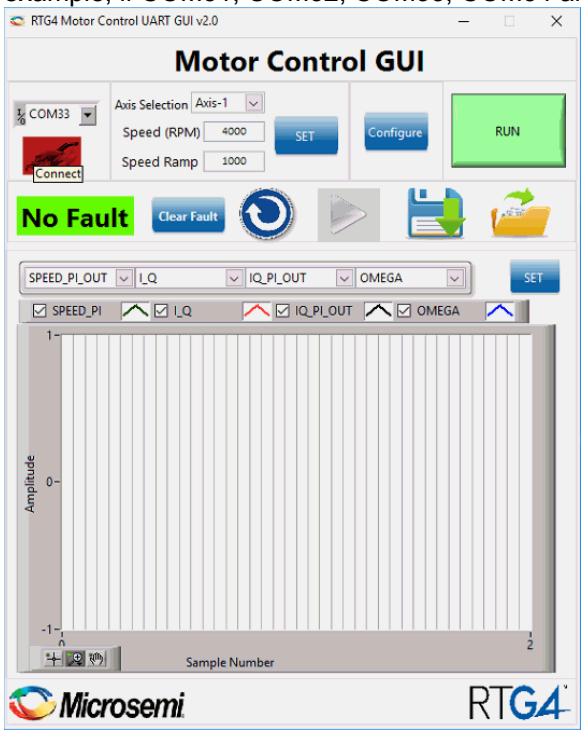
2.3 Program RTG4 Firmware

Run Flashpro to program RTG4 using one of the following binaries as appropriate:

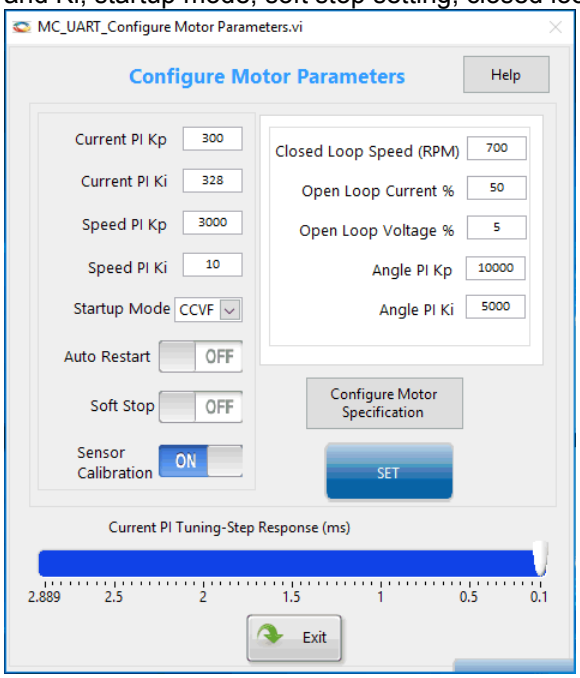
- For BLDC with resolver, use **Top_RS.stp** in **RTG4 Programming Binaries\BLDC motor Resolver** directory
- For sensorless BLDC, use **Top_SL.stp** in **RTG4 Programming Binaries\BLDC motor Sensorless** directory

2.4 Using the GUI

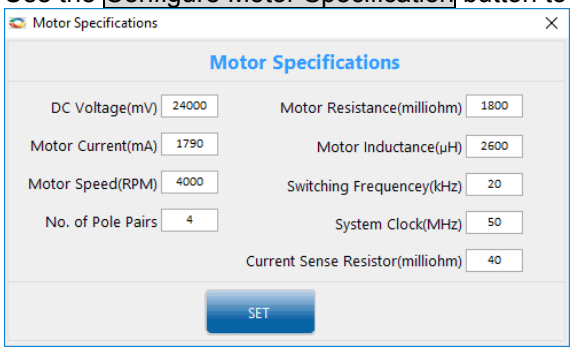
- Run **MC_UART.exe** in the **GUIs\BLDC motor v4.1** directory
- Select the third COM port from the top left drop down menu, and click the red connect button immediately below. For example, if COM31, COM32, COM33, COM34 are detected, then choose COM33



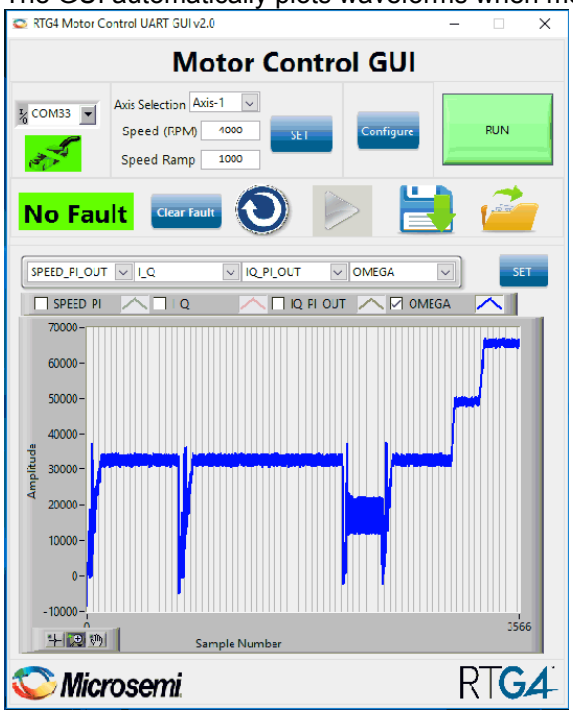
- Leave axis selection to its default value
- Use the SET button to configure motor speed, motor ramp rate, current and speed loop PI controller parameters
- Use the Configure button to open the Configure Motor Parameters window, and change PI controller constants Kp and Ki, startup mode, soft stop setting, closed loop speed threshold, open loop current and voltage



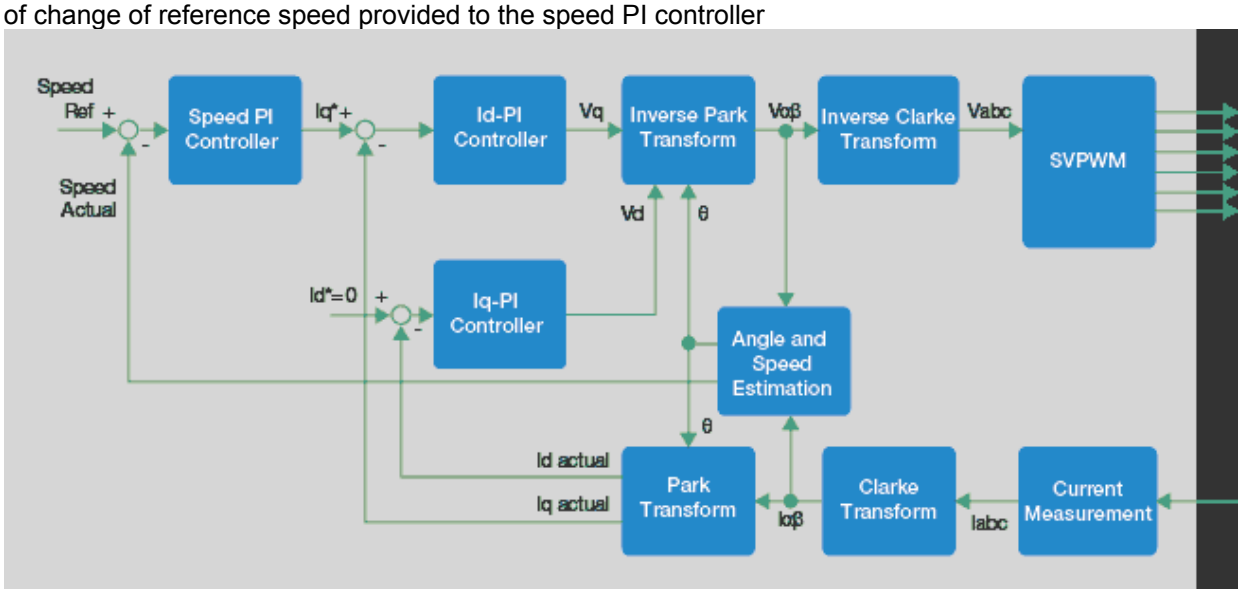
- Use the Configure Motor Specification button to change the motor specifications



- The GUI automatically plots waveforms when motor starts running



- The block diagram below shows the input and output parameters
- Parameter OMEGA is used to check speed
- The rate limiter block (not shown in the block diagram below) takes the speed input from the GUI and controls the rate of change of reference speed provided to the speed PI controller



3 Board Sockets and Link Configuration

Figure 6 below identifies major circuit blocks, LEDs, and connectors.

Figure 7 on page 7 identifies link headers that configure signal and power supply options on the board, and set LX7720 pin configurations.

Table 1 on page 7 summarizes the functions of all connectors and link headers, and provides clickable links to the appropriate parts of section 4 starting on page 10, which provides more detail and schematic around each one.

Default settings in Table 1 are highlighted in grey, and indicated in Figure 8 on page 9 for quick identification. These defaults configure the board's power supplies to be generated internally from the 24V external DC supply plugged into J11 (VGS = 15V, VCC = 5V, VDD = 3.3V, VEE = internal), and selects control signals to be those provided at J10 (RTG4 FMC connector) or J20 (40-way controller header).

Section 5 on page 17 provides pinouts for the controller interface connectors J10 and J20.

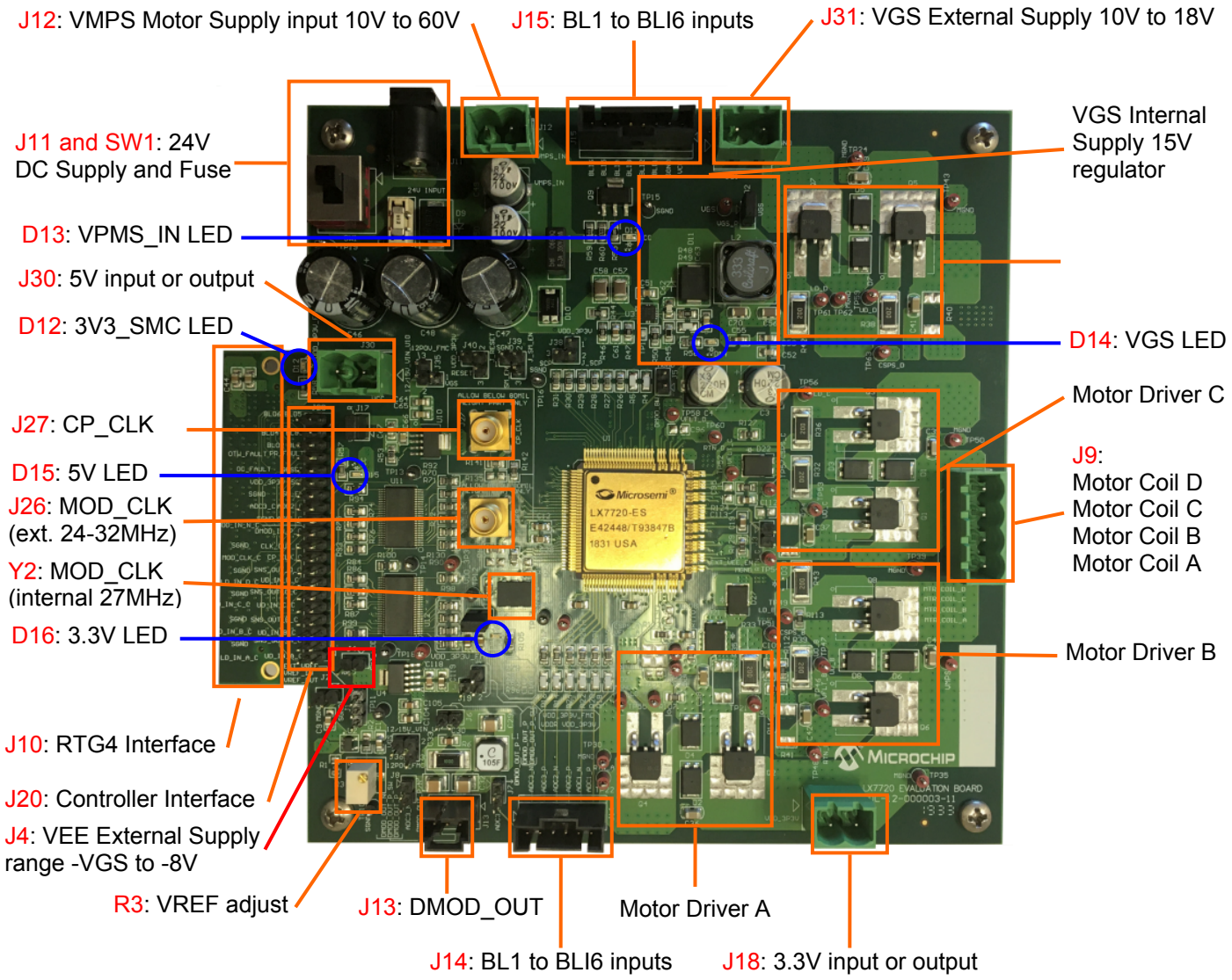


Figure 6. Location Diagram for Connectors, Circuit Blocks, and Power Rail Status LEDs

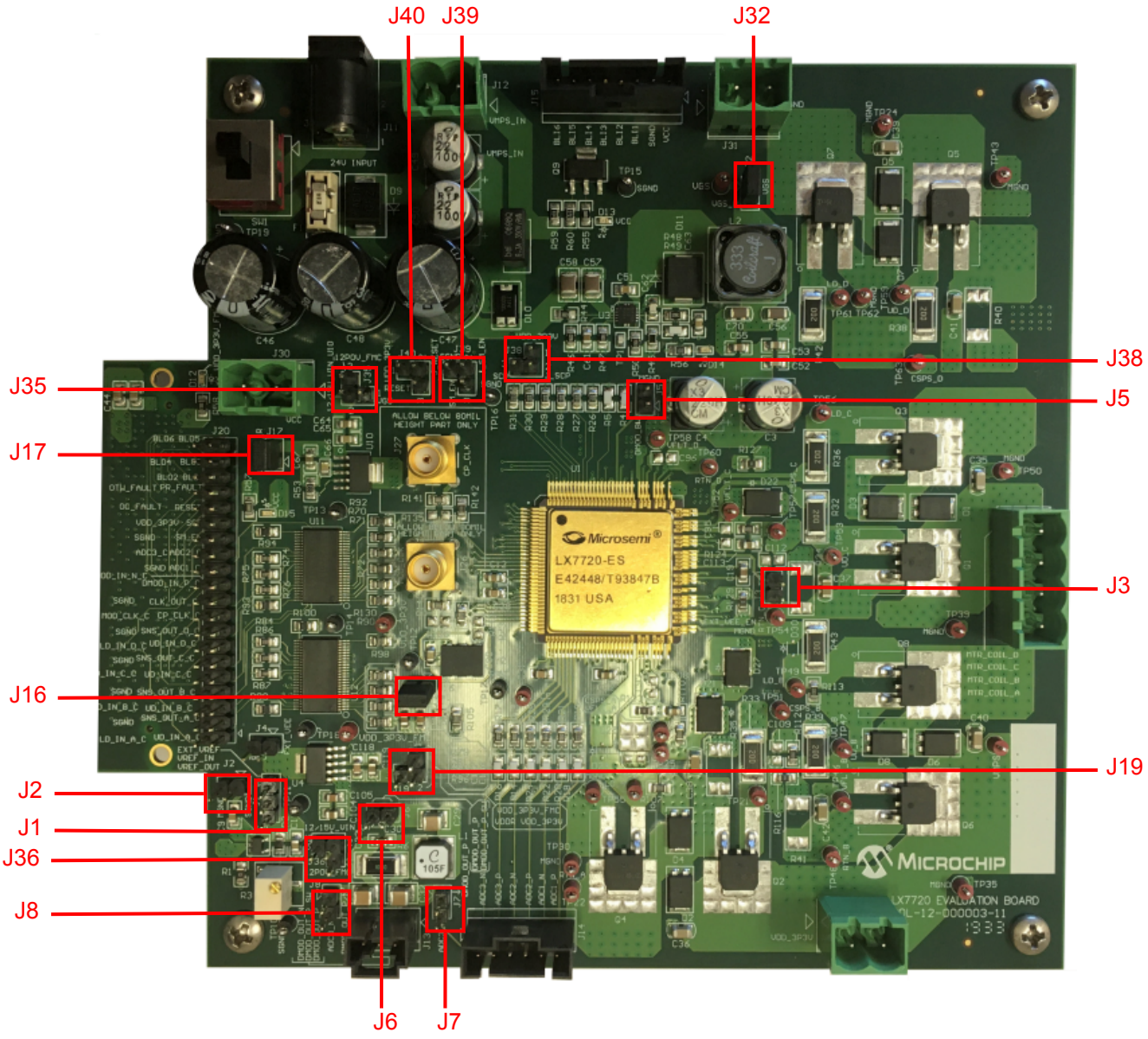


Figure 7. Location Diagram for Configuration Links

Table 1. Configuration Link and Connector Settings Summary

	Fitment	Selection	See Section	Notes
J1	Link 2 to 1	Use on-board adjustable voltage reference U2	4.6, page 12	Voltage reference
	Link 2 to 3	Use LX7720's internal 2.5V ±0.8% voltage reference		
J2	Link 1 to 2	Connect signal ground SGND to motor ground MGND	4.5, page 12	SGND to MGND link
	Open	Signal ground SGND is isolated from motor ground MGND		
J3	Link 1 to 2	Fit when using external negative VEE supply via the J4 header	4.4, page 12	VEE select
	Open	Internal VEE supply is used. Do not attach an external supply to the J4 header		
J4	Pin 1: VEE Pin 2: GND	When using external VEE supply in the range -VGS to -8V, apply VEE to header J4, and ensure that J3 is fitted with a link to select the external VEE supply option	4.4, page 12	External -VGS to -8V VEE
	Open	Internal VEE supply is used. J4 is available to monitor the VEE voltage		Internal VEE
J5	Open, or Link 1 to 2	Select longer DMOD_OUT_N pin 44 and DMOD_OUT_P pin 46 driver propagation delay by setting LX7720 DMOD_BW pin 114 = low	4.13, page 16	Resolver/LVDT driver propagation delay
	Pin 1 to VDD	Select shorter DMOD_OUT_N pin 44 and DMOD_OUT_P pin 46 driver propagation delay by setting LX7720 DMOD_BW pin 114 = high. Nearby VDD points include J38 pin 1 and J40 pin 1		

	Fitment	Selection	See Section	Notes
J6	Link 1 to 2	Enables the LC filter comprising L1, C29, C30, and R6 between LX7720 DMOD_OUT_N pin 44 and DMOD_OUT_P pin 46 outputs. The filter shapes the PWM output waveform to drive a resolver or LVDT primary	4.13, page 16	Resolver/LVDT driver filter
	Open	The LX7720 DMOD_OUT_N pin 44 and DMOD_OUT_P pin 46 outputs remain unfiltered PWM		
J7, J8	Link 1 to 2	Couple the filtered resolver/LVDT driver outputs LX7720 DMOD_OUT_N pin 44 and DMOD_OUT_P pin 46 to LX7720 ADC3_N pin 36 and ADC3_P pin 37 for measurement of the drive amplitude and fault detection	4.13, page 16	Resolver/LVDT driver measurement
	Open	LX7720 ADC3_N pin 36 and ADC3_P pin 37 are available for other purposes		ADC3 inputs
J10	HPC1-FMC connector	HPC1-FMC connector to RTG4 Development Kit board. The same signals are provided to this FMC connector and the 40-pin header J20, so connect to one or the other but not both	5, page 17	RTG4 interface
J13	DMOD outputs	Resolver/LVDT driver outputs LX7720 DMOD_OUT_N pin 44 and DMOD_OUT_P pin 46 outputs. If J6 is linked to enable the on-board LC filter, then the filtered drive outputs are available at J13 pins 2 and 3. If J6 is open, then the raw PWM drive outputs are available at J13 pins 1 and 3	4.13, page 16	Resolver/LVDT driver outputs
J14	ADC Inputs	The 3 differential inputs {ADC1_P, ADC1_N}, {ADC2_P, ADC2_N}, and {ADC3_P, ADC3_N} feed the ADC1, ADC2, and ADC3 sigma delta modulators	4.13, page 16	ADC1 to ADC3
J15	BLI Inputs	BLI1 to BLI6 inputs, VCC, and GND. BLI_TH is set to VCC/2 by R4 & R5	4.12, page 15	BLI inputs
J16	Link 1 to 2	Fit when not using J16 to measure VDD (nominally 3.3V) supply current	4.3, page 11	Normal usage
	Shunt resistor or ammeter	Replace link with current measuring device if desired for VDD from regulator U4		Measure V current
	Open	External VDD supply in the range 2.75V to 3.6V at connector J18		External 2.75V to 3.6V VDD
J17	Link 1 to 2	Fit when not using J17 to measure VCC (nominally 5V) supply current from regulator U10	4.3, page 11	Normal usage
	Shunt resistor or ammeter	Replace link with current measuring device if desired for VCC from regulator U10		Measure VCC current
	Open	External VCC supply in the range 4.5V to 5.5V at connector J30		External 4.5V to 5.5V VCC
J18	Pin 1: VDD Pin 2: GND	When using external VDD supply in the range 2.75V to 3.6V, apply the VDD supply to J18, and ensure that J16 is open so that regulator U4 is not back-driven	4.2, page 10	External 2.75V to 3.6V VDD
J19	Link 2 to 1	VDD supply is 3.3V from FMC connector J10 pins C39, D32, D36, D38, and D40. J16 also needs to be linked. Do not apply an external VDD supply to either J18 or J20 pin 30 with an RTG4 Development Kit board plugged into J10, because this will back-drive the RTG4 Development Kit's 3.3V supply	4.2, page 10	VDD = 3.3V from J10
	Link 2 to 3	VDD supply is from 3.3V regulator U4. Configure J36 for desired U4 voltage source also		VDD = internal 3.3V
	Open	VDD supply is 2.75V to 3.6V from either 40-pin header J20 pin 30 or from J18. Ensure that J16 is also open so that regulator U4 or an RTG4 Development Kit board plugged into J10 are not back-driven		2.75V to 3.6V VDD from J20 pin 30 or J18
J20	Controller connector	40 pin header to external MCU or FPGA controller. The same signals are provided to this 40-pin header and the FMC connector J10, so connect to J10 or to J20, but not to both	5, page 17	Controller interface
J26	SMA socket	External 24MHz to 32MHz MOD_CLK. R136 = 33Ω must be fitted	4.7, page 13	MOD_CLK
J27	SMA socket	External 100kHz to 300kHz CP_CLK. R135 = 33Ω must be fitted	4.8, page 13	Charge pump
J30	Pin 1: VCC Pin 2: GND	When using external VCC supply in the range 4.5V to 5.5V, apply the VCC supply to J30, and ensure that J17 is open so that regulator U10 is not back-driven	4.3, page 11	External 4.5V to 5.5V VCC
J31	Pin 1: VGS Pin 2: GND	When using external VGS supply in the range 10V to 18V, apply the VGS supply to J31, and ensure that link J32 is open so that regulator U3 is not back-driven	4.1, page 10	External 10V to 18V VGS
J32	Link 1 to 2	Fit when using internal 15V supply for VGS, and not using J32 to measure 15V supply current	4.1, page 10	Normal usage
	Shunt resistor or ammeter	Replace link with current measuring device if desired when using internal 15V supply for VGS		Measure VGS current
	Open	Omit link when using external VGS supply in the range 10V to 18V at connector J31		External 10V to 18V VGS
J35	Link 2 to 1	VCC (5V) regulator U10 source is the VGS rail selected by J32	4.1, page 10	Normal usage
	Link 2 to 3	VCC (5V) regulator U10 source is 12V from FMC connector J10 pins C35 and C37		RTG4 source
	Open	VCC (5V) regulator U10 source is unpowered. Provide an external 4.5V to 5.5V at connector J30, and ensure that link J17 is open so that regulator U10 is not back-driven		External 4.5V to 5.5V VCC

	Fitment	Selection	See Section	Notes
J36	Link 2 to 1	VDD (3.3V) regulator U4 source is the VGS rail selected by J32	4.3, page 11	Normal usage
	Link 2 to 3	VDD (3.3V) regulator U4 source is 12V from FMC connector J10 pins C35 and C37		RTG4 source
	Open	VDD (3.3V) regulator U4 source is unpowered. Provide an external 2.7V to 3.6V at connector J18, and leave link J16 open so that regulator U4 is not back-driven		External 2.75V to 3.6V VDD
J38	Link 2 to 1	Put LX7720 into reset condition by setting LX7720 RESET pin 18 = low. Reset clears latched OC_FAULT, PR_FAULT, and/or over-temperature shutdown faults	4.10, page 14	Reset on
	Link 2 to 3	LX7720 RESET pin 18 is controlled by an external signal on FMC connector J10 pin G16 or 40 pin header J20 pin 31. A pull-down resistor ensures that LX7720 remains out of reset condition if the external signal is open		Managed by controller on J10 or J20
	Open	Lock LX7720 out of reset condition by setting RESET pin 18 = low		Reset off
J39	Link 2 to 1	Disable Safe Mode by setting LX7720 SM_EN pin 17 = low	4.11, page 15	Safe Mode on
	Link 2 to 3	LX7720 SM_EN pin 17 is controlled by an external signal on FMC connector J10 pin H17 or 40 pin header J20 pin 27. A pull-up resistor ensures that Safe Mode is enabled by default if the external signal is open		Managed by controller on J10 or J20
	Open	Enable Safe Mode by setting LX7720 SM_EN pin 17 = high		Safe Mode off
J40	Link 2 to 1	Enable Simultaneous Conduction Protection by setting LX7720 SCP pin 117 = high	4.9, page 14	SCP on
	Link 2 to 3	LX7720 SCP pin 117 is controlled by an external signal on FMC connector J10 pin K23 or 40 pin header J20 pin 29. A pull-down resistor ensures that Simultaneous Conduction Protection is disabled by default if the external signal is open		Managed by controller on J10 or J20
	Open	Disable Simultaneous Conduction Protection by setting LX7720 SCP pin 117 = low		SCP off

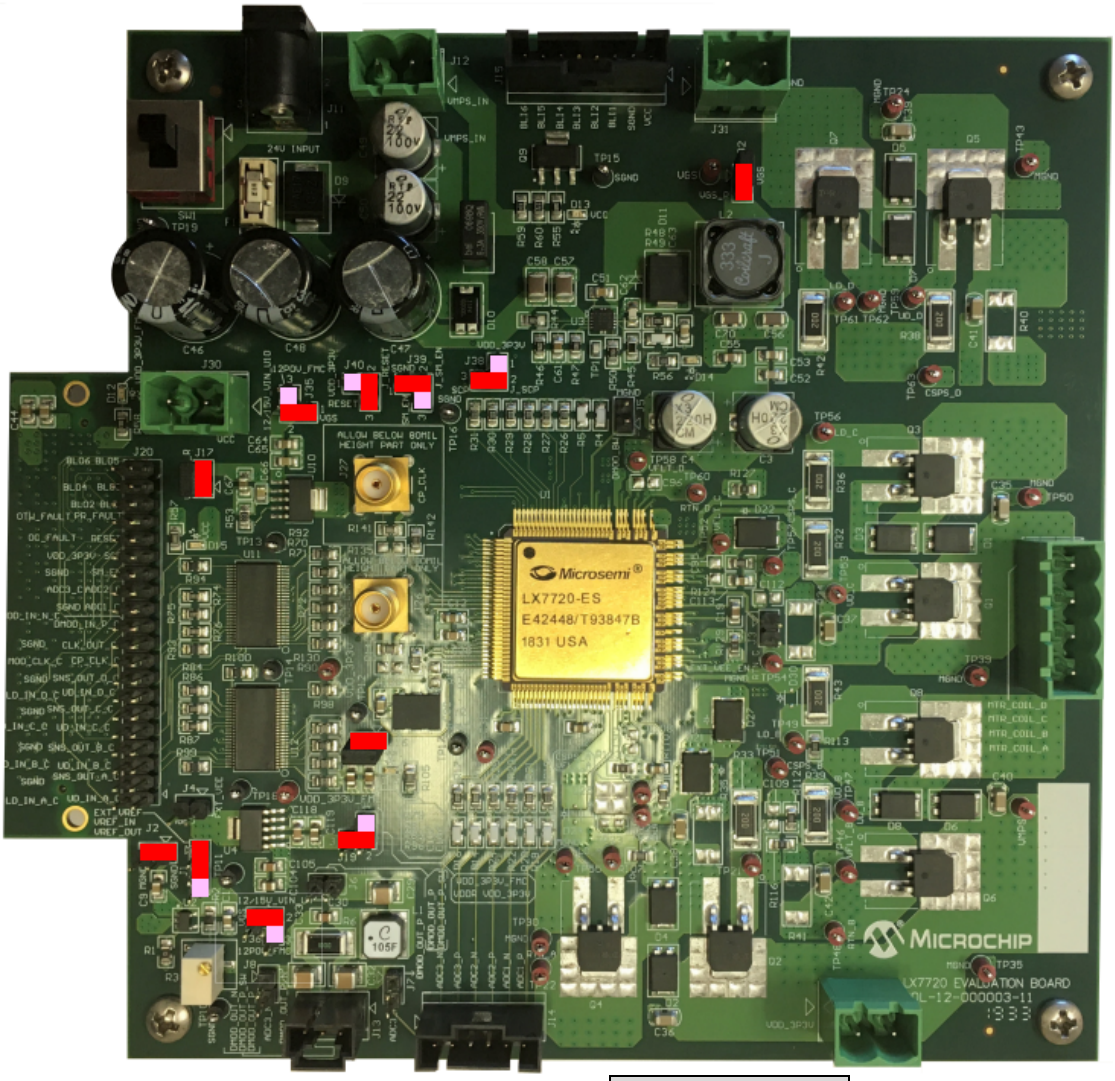


Figure 8. Default Shorting Jumper Positions, as highlighted in grey in Table 1

4 LX7720 Daughter Board Configuration Options

4.1 VGS Gate Driver Supply (15V) Regulator Settings

The header J32 selects either the on-board 15V regulator, or an external 10V to 18V power supply connected to J31 (Table 2, Figure 9).

Table 2. VGS Gate Driver Supply (15V) Link Settings

VGS Regulator Source	J32 Link	J31 Connector
VGS is 15V using on-board regulator U3 supplied by external 24V AC adapter connected to DC power socket J11	Link 1 to 2 or insert ammeter to measure VGS current	Open
VCC is external 4.5V to 5.5V at connector J30	Open	External 10V to 18V power supply

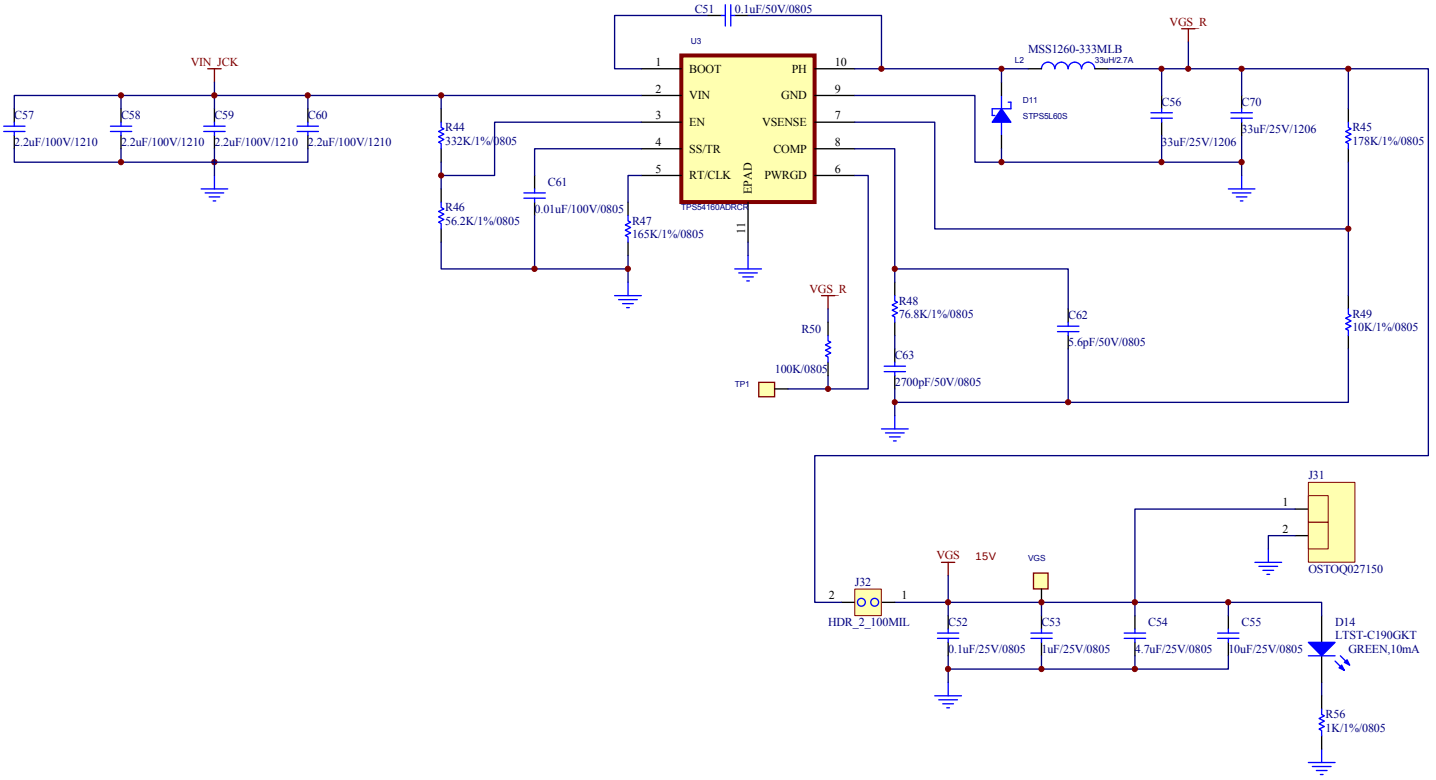


Figure 9. VGS Gate Driver Supply (15V) Regulator Schematic

4.2 VDD Logic Supply (3.3V) Regulator Settings

The headers J36, J19, and J16 select either the on-board 3.3V regulator and its power source, or an external 2.7V to 3.6V power supply connected to J18 (Table 3, Figure 10).

While the LX7720 allows a logic supply range of 2.1V to 5.5V, the LX7720 daughter board's allowed range is 2.7V to 3.6V. This limitation is due to the supply range of the ASVMPC-27.000MHZ-LR-T 27MHz oscillator module Y2, and the SN74LVTH16245A bus transceivers that interface both the 2x20 pin controller interface header J20 and the RTG4 interface FMC connector J10.

Table 3. VDD Logic Supply (3.3V) Regulator Link Settings

VDD Regulator Source	J36 Link	J19 Link	J16 Link	J18 Connector
VDD is on-board 3.3V using regulator U4 supplied by VGS rail	Link 2 to 1	Link 2 to 3	Link 1 to 2 or insert ammeter to measure VDD current	Open
VDD is on-board 3.3V using regulator U4 supplied by 12V from FMC connector J10 pins C35 and C36 (RTG4 board)	Link 2 to 3			Open
VDD is external 3.3V from FMC connector J10 pins C39, D32, D36, D38, and D40 (RTG4 board) Regulator U4 is unpowered	Open	Link 2 to 1		Open
VDD is external 2.7V to 3.6V at connector J18 Regulator U4 is unpowered	Open	Open	Open	External 2.7V to 3.6V power supply

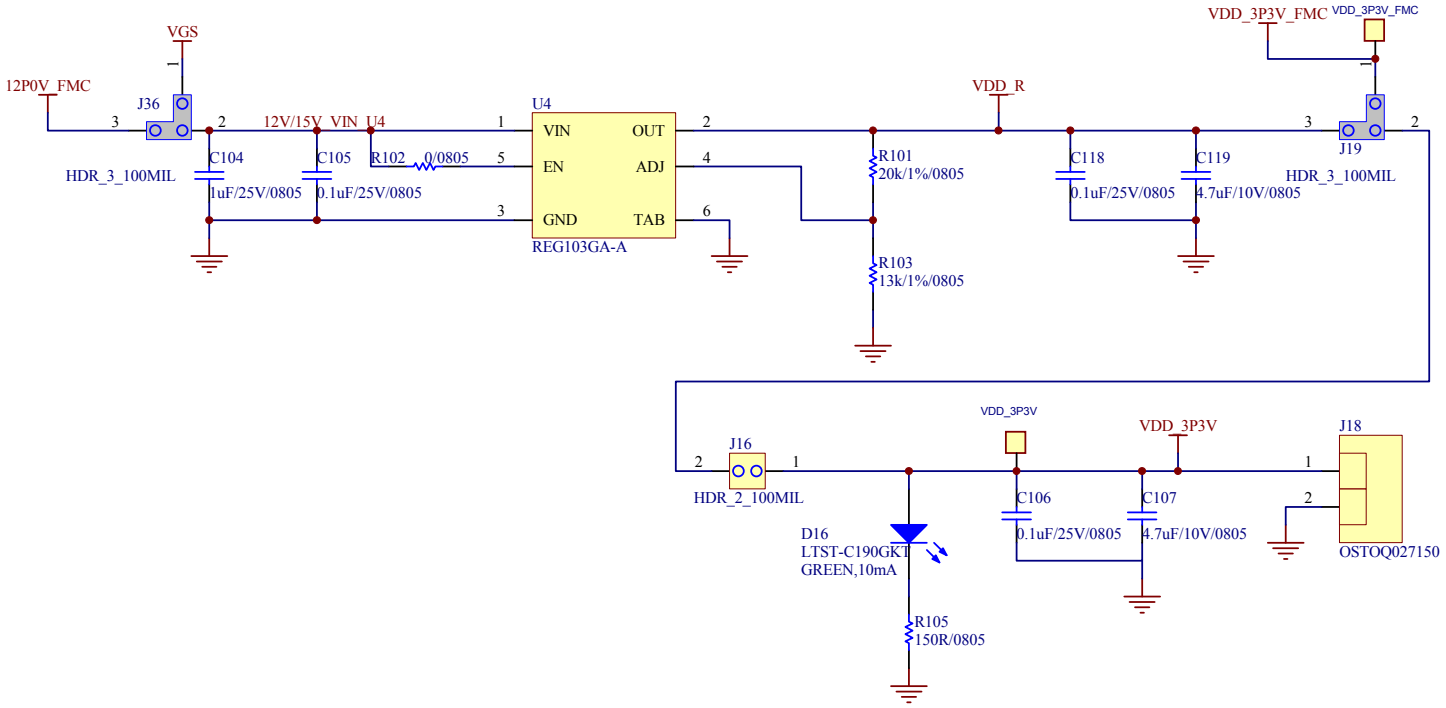


Figure 10. VDD Logic Supply (3.3V) Regulator Schematic

4.3 VCC Signal Supply (5V) Regulator Settings

The headers J35 and J17 select either the on-board 5V regulator and its power source, or an external 4.5V to 5.5V power supply connected to J30 (Table 4, Figure 11).

Table 4. VCC Signal Supply (5V) Regulator Link Settings

VCC Regulator Source	J35 Link	J17 Link	J30 Connector
VCC is on-board 5V using regulator U10 supplied by VGS rail	Link 2 to 1	Link 1 to 2 or insert ammeter to measure VCC current	Open
VCC is on-board 5V using regulator U10 supplied by 12V from FMC connector J10 pins C35 and C36 (RTG4 board)	Link 2 to 3		Open
VCC is external 4.5V to 5.5V at connector J30 Regulator U10 is unpowered	Open	Open	External 4.5V to 5.5V power supply

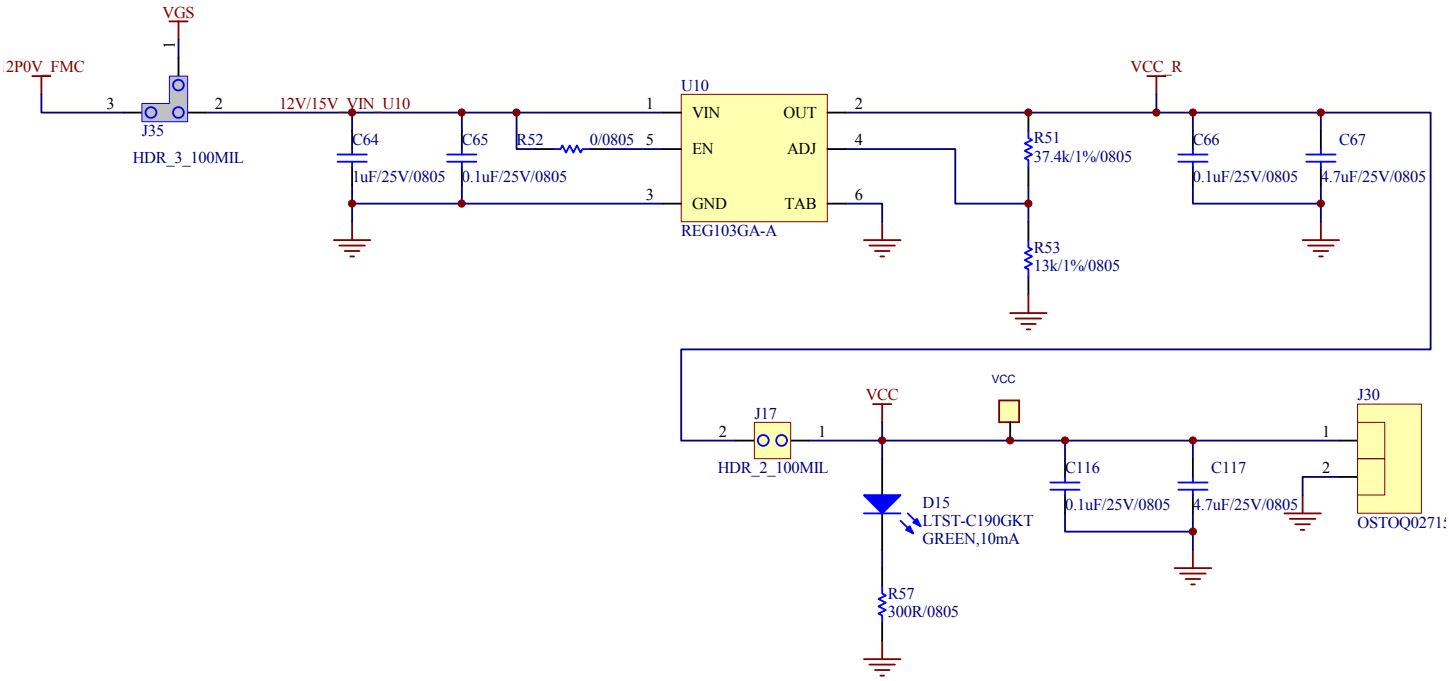


Figure 11. 5V Regulator Schematic

4.4 VEE Negative Supply Settings

The header J3 selects either the LX7720's internal VEE charge pump, or an external -8V to -VGS power supply connected to J4 (Table 5, Figure 12).

Table 5. VEE Negative Supply Link Settings

VEE Regulator Source	J3 Link Fitment	J4 Connector Usage
Use LX7720's internal VEE charge pump	Open	Open
Use external -8V to -VGS power supply	Link 1 to 2	-8V to -VGS power supply

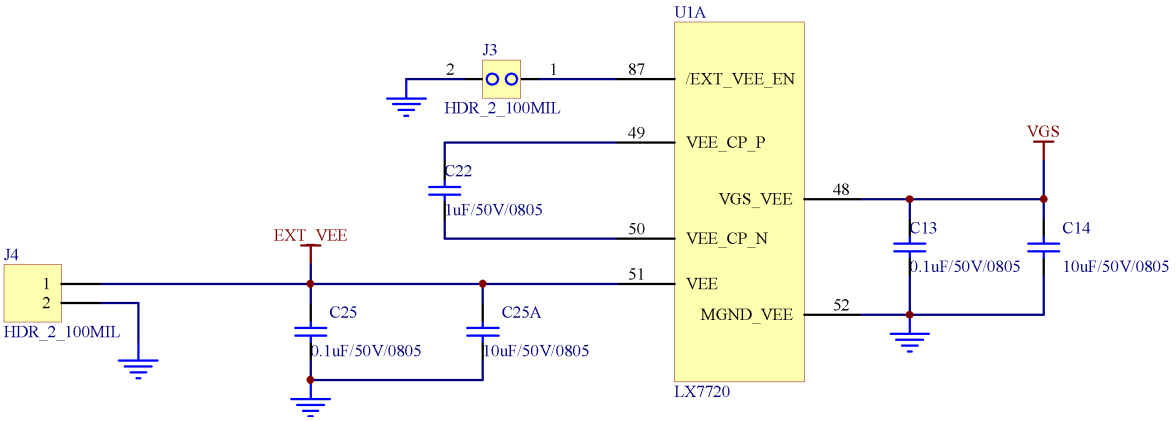


Figure 12. VEE Regulator Schematic

4.5 Motor Ground MGND to Signal Ground SGND Connection

The 2-pin header J2 joins MGND to SGND on the PCB. If the link is open, ensure that there is a reliable DC path in the system under evaluation between MGND to SGND. The absolute maximum potential difference allowed between MGND and SGND is ±10V.

Table 6. LX7720 Reference Voltage Selection Link Settings

Voltage Reference Source	J1 Link
Signal ground SGND is isolated from motor ground MGND	Open
Signal ground SGND is connected to the motor ground MGND on the PCB	Link 1 to 2

4.6 Reference Voltage Selection

The 3-pin header J1 selects either the LX7720's internal 2.5V ±0.8% reference or an external reference U2, adjustable by potentiometer R3 (Table 7, Figure 13). The adjustment range is 2.3V to 2.7V.

Table 7. LX7720 Reference Voltage Selection Link Settings

Voltage Reference Source	J1 Link
Use the LX7720's internal 2.5V ±0.8% voltage reference	Link 2 to 1
Use external adjustable reference U2. Use R3 to adjust the voltage within the range 2.3V to 2.7V	Link 2 to 3

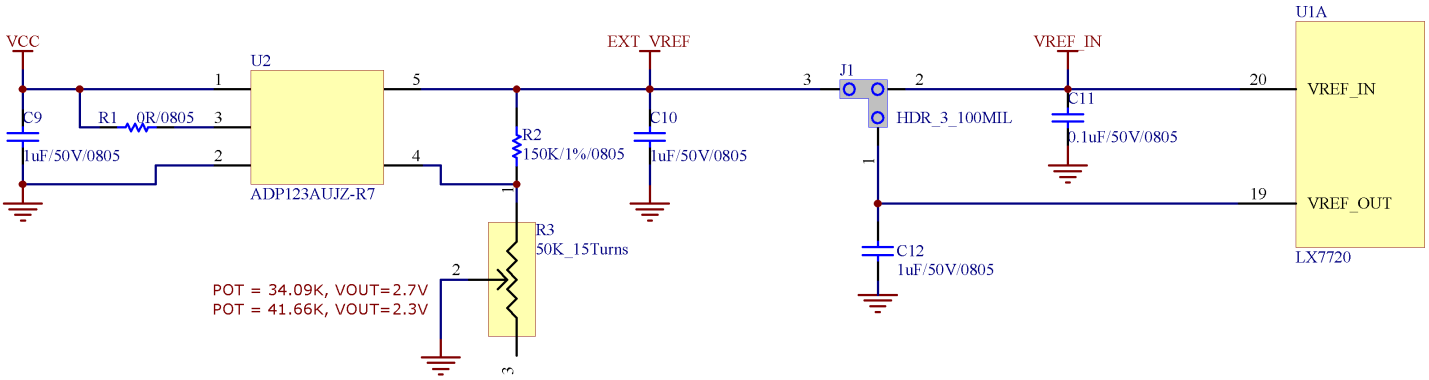


Figure 13. Reference Voltage Selection Schematic

4.7 MOD_CLK Input Selection

There are 4 possible sources for the 24MHz to 32MHz modulator clock, MOD_CLK_D at LX7720 pin 31. The 2x20 pin controller interface header J20 and RTG4 Interface FMC connector J10 are wired in parallel to deliver an external modulator clock MOD_CLK_C, which is buffered by a gate in U11 (SN74LVTH16245A) to become MOD_CLK. As shown in Figure 14 below, MOD_CLK, a 27MHz oscillator module Y2, and an external clock at SMA connector J26 are summed through resistors to become the final MOD_CLK_D delivered to the LX7720.

Factory build has both R73 and R136 not fitted, so the default clock source is from headers J20 and J10 (Table 8).

The modulator clock should be in the frequency range 24MHz to 32MHz, with a logic swing of 0V to VDD (default 3.3V).

Table 8. LX7720 MOD_CLK Input Selection

MOD_CLK Input Source	R73	R136	R143
External 24MHz to 32MHz square wave clock on either J20 pin 18 or J10 pin H8 (drive one pin, leave the other pin Hi-Z). Ideal logic swing is 0V to VDD, but the SN74LVTH16245A buffer is over-voltage tolerant to 5.5V	Not fitted (default)	Not fitted (default)	33Ω (default)
External 24MHz to 32MHz square wave clock on SMA connector J26 delivering a logic swing of 0V to VDD into 50Ω	Not fitted (default)	33Ω	Not fitted
Internal 27MHz square wave clock from oscillator module Y2	0Ω	Not fitted (default)	Not fitted

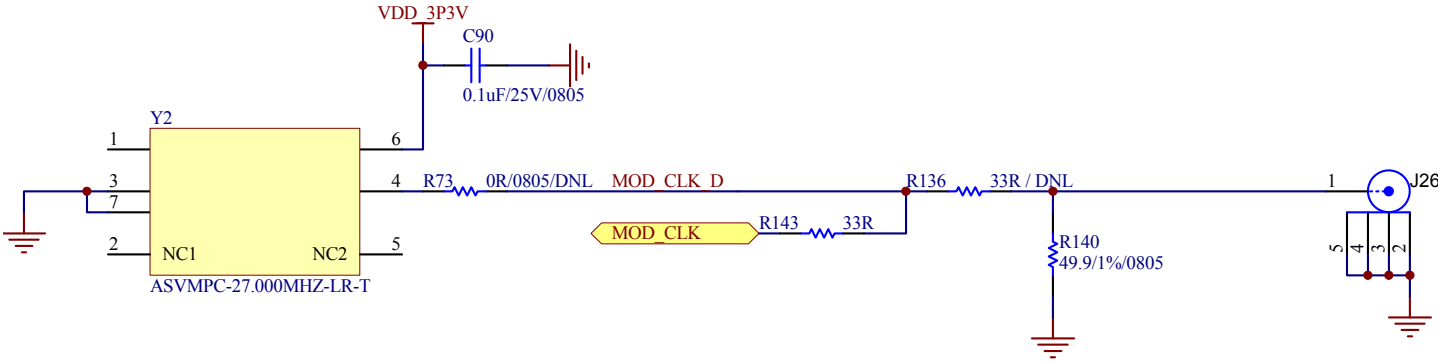


Figure 14. MOD_CLK Internal 27MHz Oscillator and External SMA Input Schematic

4.8 Charge Pump CP_CLK Selection

There are 4 possible sources for the 100kHz to 300kHz charge pump clock, CP_CLK_D at LX7720 pin 13. The 2x20 pin controller interface header J20 and RTG4 Interface FMC connector J10 are wired in parallel to deliver an external clock CP_CLK_C, which is buffered by a gate in U12 (SN74LVTH16245A) to become CP_CLK. As shown in Figure 15 below, CP_CLK and an external clock at SMA connector J27 are summed through resistors to become the final CP_CLK_D delivered to the LX7720.

Factory build has R135 not fitted, so the default clock source is from headers J20 and J10 (Table 9).

The charge pump clock should be in the frequency range 100kHz to 300kHz, with a logic swing of 0V to VDD (default 3.3V).

Table 9. LX7720 CP_CLK Input Selection

CP_CLK Input Source	R135	R142
External 100kHz to 300kHz square wave clock on either J20 pin 17 or J10 pin G21 (drive one pin, leave the other pin Hi-Z). Ideal logic swing is 0V to VDD, but the SN74LVTH16245A buffer is over-voltage tolerant to 5.5V	Not fitted (default)	33Ω (default)
External 100kHz to 300kHz square wave clock on SMA connector J27 delivering a logic swing of 0V to VDD into 50Ω	33Ω	Not fitted

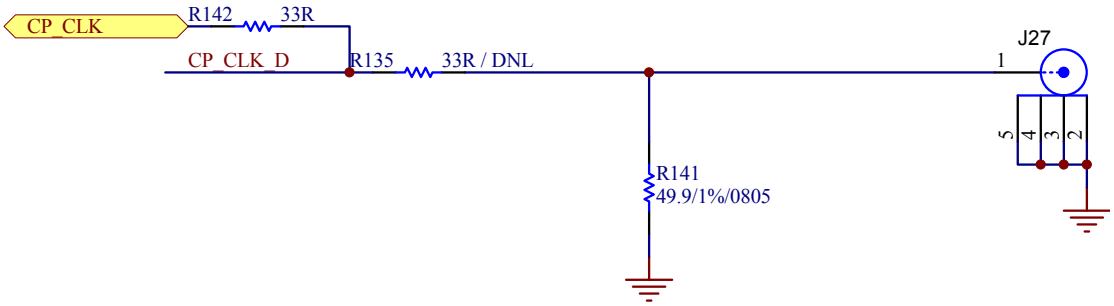


Figure 15. CP_CLK Selection and External SMA Input Schematic

4.9 Simultaneous Conduction Protection (LX7720 SCP pin 117)

Simultaneous conduction protection prevents the upper and lower driver for each half-bridge being on simultaneously. When disabled, the upper and lower drivers are operated independently with no overlap prevention.

Table 10. Simultaneous Conduction Protection Link Settings

Simultaneous Conduction Protection	J38 Link
Simultaneous Conduction Protection is enabled (LX7720 SCP pin 117 = high)	Link 2 to 1
Simultaneous Conduction Protection is controlled by an external signal on FMC connector J10 pin K23 (RTG4 board) or 40 pin header J20 pin 29 (other controller). A pull-down resistor ensures that Simultaneous Conduction Protection is disabled by default if the external signal is open	Link 2 to 3
Simultaneous Conduction Protection is disabled (LX7720 SCP pin 117 = low)	Open

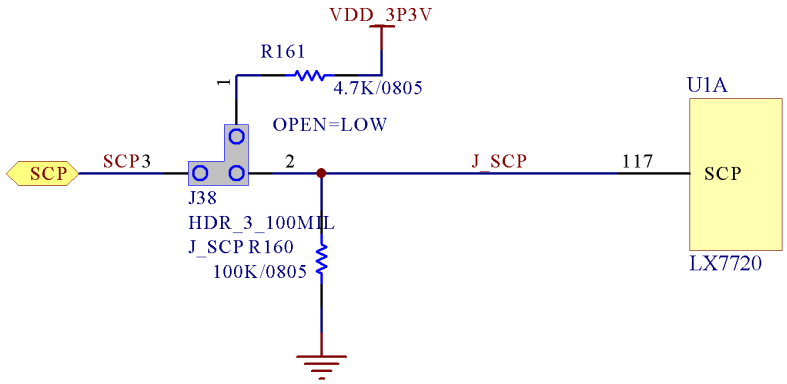


Figure 16. Simultaneous Conduction Protection Schematic

4.10 Reset (LX7720 RESET pin 18)

The LX7720's active-high reset input clears latched OC_FAULT, PR_FAULT, and/or over-temperature shutdown faults.

Table 11. Reset Link Settings

Reset	J40 Link
Put LX7720 into reset condition by setting LX7720 RESET pin 18 = low. Reset clears latched OC_FAULT, PR_FAULT, and/or over-temperature shutdown faults	Link 2 to 1
LX7720 RESET pin 18 is controlled by an external signal on FMC connector J10 pin G16 (RTG4 board) or 40 pin header J20 pin 31 (other controller). A pull-down resistor ensures that LX7720 remains out of reset condition if the external signal is open	Link 2 to 3
Lock LX7720 out of reset condition by setting RESET pin 18 = low	Open

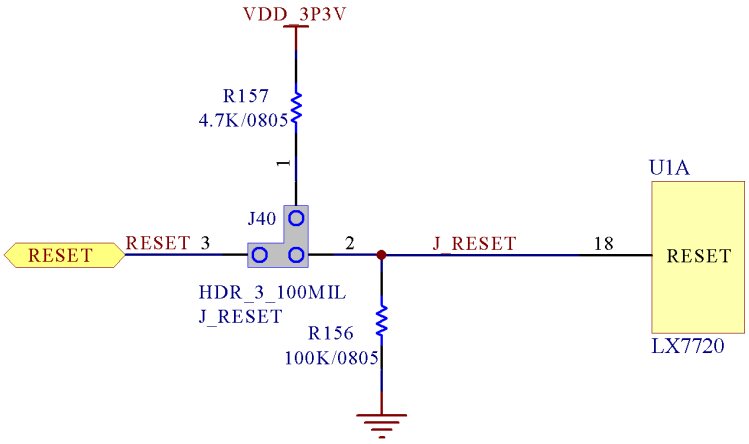


Figure 17. Reset Schematic

4.11 Safe Mode (LX7720 SM_EN pin 17)

The LX7720's active-high Safe Mode input enables protection countermeasures when faults are detected.

Table 12. Safe Mode Link Settings

Safe Mode	J39 Link
Disable Safe Mode by setting LX7720 SM_EN pin 17 = low	Link 2 to 1
LX7720 SM_EN pin 17 is controlled by an external signal on FMC connector J10 pin H17 or 40 pin header J20 pin 27. A pull-up resistor ensures that Safe Mode is enabled by default if the external signal is open	Link 2 to 3
Enable Safe Mode by setting LX7720 SM_EN pin 17 = high	Open

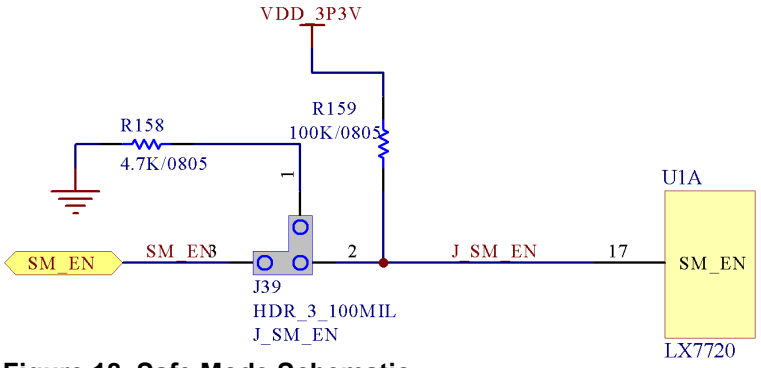


Figure 18. Safe Mode Schematic

4.12 Bi-Level Comparator Inputs BL1 to BL6

The LX7720's 6 bi-level comparator inputs BLI1 to BLI6 are routed to connector J15 pins 3 to 8 respectively. The common comparator threshold LX7720 BLI_TH pin 119 is set to VCC/2 by R4 & R5.

The LX7720's 6 bi-level comparator outputs BLO1 to BLO6 are routed to the FMC connector (Table 16 on page 19) and to the 40-way header J20 (Table 17 on page 19).

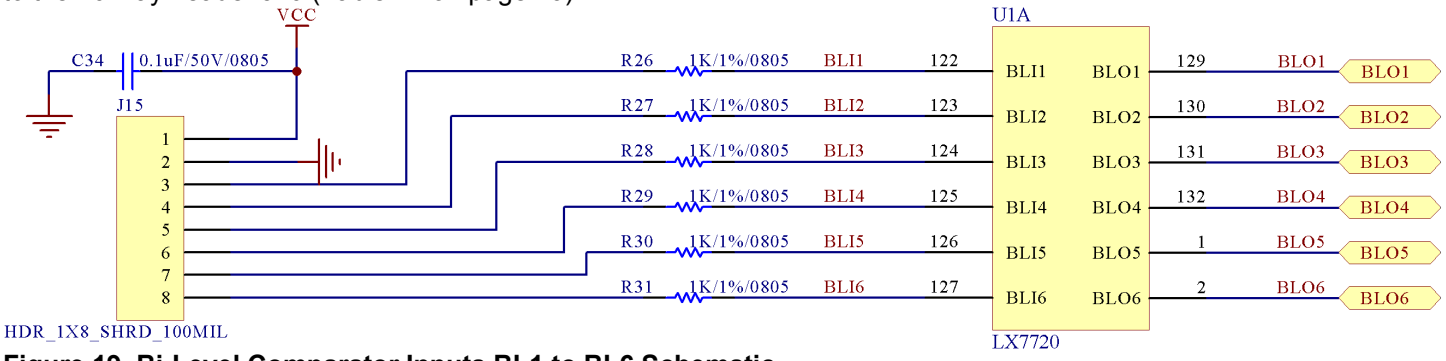


Figure 19. Bi-Level Comparator Inputs BL1 to BL6 Schematic

4.13 Resolver/LVDT Interface

Links J5 to J8 configure the resolver/LVDT driver outputs with or without LC filtering for primary drive wave shaping.

Link J5 is left open by default to set LX7720 DMOD_BW pin 114 = low, selecting the longer DMOD_OUT_N pin 44 and DMOD_OUT_P pin 46 driver propagation delay. To select the shorter driver propagation delay, set LX7720 DMOD_BW pin 114 = high by connecting J5 pin 1 to VDD. Nearby VDD points include J38 pin 1 and J40 pin 1.

Standard connections for the AMCI R11X-A10/7 resolver used to develop the RTG4 programming are:

- Links J5 to J8: all open
- Primary: J13 pin 1: black/white, J13 pin 2: n/c, J13 pin 3: red/white
- Secondary 1: J14 pin 3: red, J14 pin 4: black
- Secondary 2: J14 pin 5: blue, J14 pin 6: yellow

Table 13. Resolver/LVDT Link Settings

Resolver/LVDT Options	J6 Link	J7 Link	J8 Link	J14 Connector	J13 Connector
Resolver/LVDT driver outputs DMOD_OUT_P and DMOD_OUT_N routed directly to J13 without filtering	Open	Open	Open	ADC1, ADC2, and ADC3 available for general use	DMOD_OUT_P: pin 1 DMOD_OUT_N: pin 3
Resolver/LVDT driver outputs DMOD_OUT_P and DMOD_OUT_N routed to J13 with LC filtering. The filter shapes the PWM output waveform	Link 1 to 2				DMOD_OUT_P: pin 2 DMOD_OUT_N: pin 3
Resolver/LVDT driver outputs DMOD_OUT_P and DMOD_OUT_N routed to J13 with LC filtering. The filter shapes the PWM output waveform. ADC_3 is used to monitor the filtered drive output for closed loop control of the drive amplitude and for fault detection	Link 1 to 2	Link 1 to 2	Link 1 to 2	Only ADC1 and ADC2 available for general use	

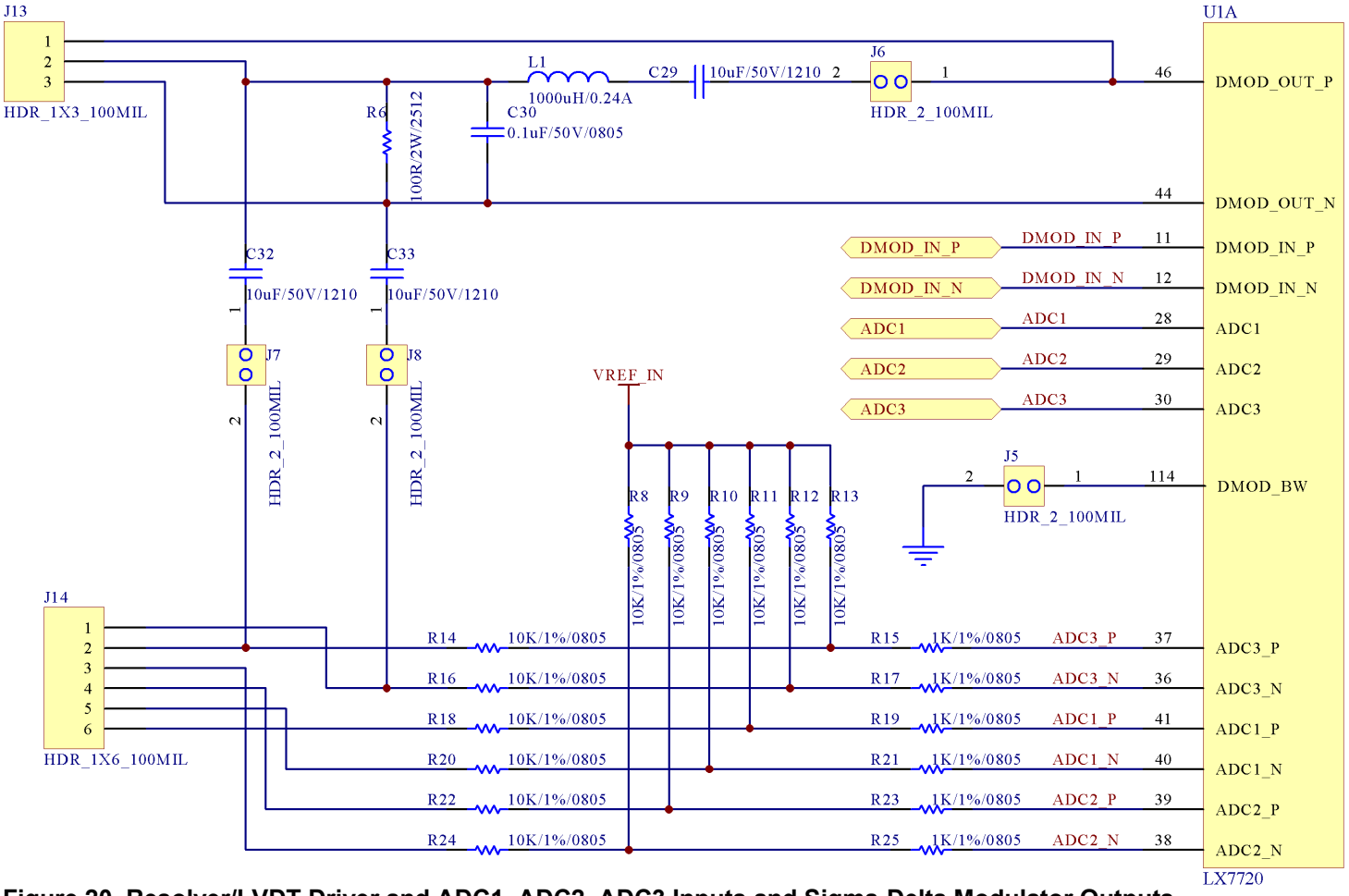


Figure 20. Resolver/LVDT Driver and ADC1, ADC2, ADC3 Inputs and Sigma-Delta Modulator Outputs

4.14 Motor Connections

Standard connections for the Trinamic QBL4208-41-04-006 24V, 8 phase, 3 pole BLDC motor used to develop the RTG4 programming are J9 pin 1: yellow (coil A), pin 2: red (coil B), pin 3: black (coil C).

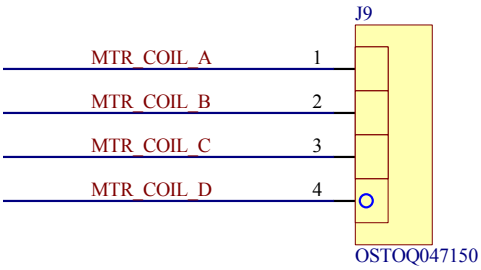


Figure 21. Motor Winding Connections Schematic

5 Control and Acquisition Signals Headers J10 and J20

J20 is a 2x20 pin 0.1" pitch pin header which provides buffered control signals to an external controller (such as SAMRH71) or FPGA (such as RTG4 or RTAX-S/SL).

J10 provides direct connection to the HPC1-FMC (FPGA Mezzanine Card) connectors on the RTG4 Development Kit and the PolarFire MPF300-EVAL-KIT. Table 14 below shows the FPGA pin routing for each LX7720 pin on these kits.

FMC Pin	LX7720 Signal Name	LX7720 Signal Type and Function	RTG4 Pin Number	RTG4 Pin Name	PolarFire Pin Number	PolarFire Pin Name
C11	ADC1_C	Buffered ADC2 bit stream output	J11	MSIO248NB6	G16	GPIO5NB2
C27	UD_IN_A_C	Buffered UD_IN_A FET drive input	A8	MSIO261NB6	D6	GPIO13NB2
D27	LD_IN_C_C	Buffered LD_IN_C FET drive input	B8	MSIO252NB6	G11	GPIO18NB2
E10	UD_IN_B_C	Buffered UD_IN_B FET drive input	F18	MSIO287NB5	T4	GPIO217NB4
F7	UD_IN_C_C	Buffered UD_IN_C FET drive input	J19	MSIO296PB5	AB9	GPIO183PB4
F8	LD_IN_B_C	Buffered LD_IN_B FET drive input	H19	MSIO296NB5	AA8	GPIO183NB4
F11	LD_IN_A_C	Buffered LD_IN_A FET drive input	F20	MSIO299NB5	AB6	GPIO179NB4
F13	SNS_OUT_A_C	Buffered SNS_OUT_A bit stream output	D19	MSIO294PB5	T7	GPIO218PB4
F14	SNS_OUT_B_C	Buffered SNS_OUT_B bit stream output	C19	MSIO294NB5	U7	GPIO218NB4
F19	BLO4	Bi-Level Detector output 4	C13	MSIO277PB5	AB4	GPIO177PB4
G9	ADC3_C	Buffered ADC3 bit stream output	K10	MSIO242PB6	H16	GPIO32PB2
G16	RESET	RESET input via J40 link header	G15	MSIO269NB6	E12	GPIO23NB2
G18	OTW_FAULT	OTW_FAULT output	D11	MSIO268PB6	D10	GPIO26PB2
G21	CP_CLK_C	Buffered 150kHz ±50kHz CP_CLK charge pump clock input	B10	MSIO270PB6	B9	GPIO25PB2
G24	DMOD_IN_P_C	Buffered DMOD_IN_P drive input	B5	MSIO255PB6	D8	GPIO14PB2
G25	UD_IN_D_C	Buffered UD_IN_D FET drive input	B6	MSIO255NB6	C8	GPIO14NB2
G28	BLO6	Bi-Level Detector output 6	C6	MSIO246NB6	H11	GPIO4NB2
G30	BLO5	Bi-Level Detector output 5	C3	MSIO243PB6	B10	GPIO28PB2
G31	BLO3	Bi-Level Detector output 3	B3	MSIO243NB6	A10	GPIO28NB2
H7	CLK_OUT_C	Buffered CLK_OUT Σ-Δ mod clock output	H8	MSIO245PB6	L19	GPIO34PB2
H8	MOD_CLK_C	Buffered 24MHz to 32MHz MOD_CLK Σ-Δ modulator clock input	H9	MSIO245NB6	L18	GPIO34NB2
H10	ADC2_C	Buffered ADC2 bit stream output	F9	MSIO258PB6	J18	GPIO33PB2
H13	SNS_OUT_D_C	Buffered SNS_OUT_D bit stream output	G10	MSIO257PB6	K15	GPIO0PB2
H14	SNS_OUT_C_C	Buffered SNS_OUT_C bit stream output	G11	MSIO257NB6	J15	GPIO0NB2
H17	SM_EN	SM_EN input via J39 link header	D14	MSIO273NB6	K17	GPIO35NB2
H19	OC_FAULT	OC_FAULT output	E9	MSIO259PB6	A7	GPIO16PB2
H20	PR_FAULT	PR_FAULT output	D9	MSIO259NB6	A8	GPIO16NB2
H23	DMOD_IN_N_C	Buffered DMOD_IN_N drive input	C9	MSIO256NB6	B6	GPIO17NB2
H25	LD_IN_D_C	Buffered LD_IN_D FET drive input	A4	MSIO247PB6	H13	GPIO1PB2
H34	BLO2	Bi-Level Detector output 2	F7	MSIO249PB6	G10	GPIO21PB2
H35	BLO1	Bi-Level Detector output 1	F8	MSIO249NB6	F10	GPIO21NB2
K23	SCP	SCP input via J38 link header	C16	MSIO282NB5	AB1	GPIO176NB4

Table 14. Mapping of HPC1-FMC pins, LX7720 pins, and RTG4 and PolarFire FPGA pins on the EVBs

Signals described as buffered in Table 14 above and Table 17 on page 19 are passed through one of the two on-board SN74LVTH16245A bus buffers U11 and U12. Buffer output voltage swing is GND to VDD. VDD is normally 3.3V supplied by on-board regulator U4. See section 4.2 on page 10 for details on selecting an alternative VDD supply voltage in the range 2.75V to 3.6V. Buffered signals are highlighted in blue in Table 14 above, Table 15 below and Table 16 and Table 17 on page 19

Other inputs and outputs are VDD logic level signals directly to and from LX7720 pins, and these signals are highlighted in red, unless the description shows the signal passing through a link header. These signals are highlighted in green. See Table 1 on page 7 for link header configuration details.

Table 15. LX7720 Control and Acquisition Signals HPC1-FMC Connector J10 Pinout (A to E)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	GND	B1	-	C1	GND	D1	-	E1	GND
A2	-	B2	-	C2	-	D2	-	E2	-
A3	-	B3	GND	C3	-	D3	GND	E3	-
A4	GND	B4	GND	C4	GND	D4	GND	E4	GND
A5	GND	B5	-	C5	GND	D5	-	E5	GND
A6	-	B6	-	C6	-	D6	-	E6	-
A7	-	B7	GND	C7	-	D7	GND	E7	-
A8	GND	B8	GND	C8	GND	D8	GND	E8	GND
A9	GND	B9	-	C9	GND	D9	-	E9	-
A10	-	B10	-	C10	-	D10	GND	E10	UD_IN_B_C
A11	-	B11	GND	C11	ADC1_C	D11	-	E11	GND
A12	GND	B12	GND	C12	GND	D12	-	E12	-
A13	GND	B13	-	C13	GND	D13	GND	E13	-
A14	-	B14	-	C14	-	D14	-	E14	GND
A15	-	B15	GND	C15	-	D15	-	E15	-
A16	GND	B16	GND	C16	GND	D16	GND	E16	-
A17	GND	B17	-	C17	GND	D17	-	E17	GND
A18	-	B18	-	C18	-	D18	-	E18	-
A19	-	B19	GND	C19	-	D19	GND	E19	-
A20	GND	B20	GND	C20	GND	D20	-	E20	GND
A21	GND	B21	-	C21	GND	D21	-	E21	-
A22	-	B22	-	C22	-	D22	GND	E22	-
A23	-	B23	GND	C23	-	D23	-	E23	GND
A24	GND	B24	GND	C24	GND	D24	-	E24	-
A25	GND	B25	-	C25	GND	D25	GND	E25	-
A26	-	B26	-	C26	-	D26	-	E26	GND
A27	-	B27	GND	C27	UD_IN_A_C	D27	LD_IN_C_C	E27	-
A28	GND	B28	GND	C28	GND	D28	GND	E28	-
A29	GND	B29	-	C29	GND	D29	-	E29	GND
A30	-	B30	-	C30	-	D30	-	E30	-
A31	-	B31	GND	C31	-	D31	-	E31	-
A32	GND	B32	GND	C32	GND	D32	VDD_3P3V_FMC	E32	GND
A33	GND	B33	-	C33	GND	D33	-	E33	-
A34	-	B34	-	C34	-	D34	-	E34	-
A35	-	B35	GND	C35	12P0V_FMC	D35	-	E35	GND
A36	GND	B36	GND	C36	GND	D36	VDD_3P3V_FMC	E36	-
A37	GND	B37	-	C37	12P0V_FMC	D37	-	E37	-
A38	-	B38	-	C38	GND	D38	VDD_3P3V_FMC	E38	GND
A39	-	B39	GND	C39	VDD_3P3V_FMC	D39	-	E39	VADJ
A40	GND	B40	GND	C40	GND	D40	VDD_3P3V_FMC	E40	GND

Table 16. LX7720 Control and Acquisition Signals HPC1-FMC Connector J10 Pinout (F to K)

Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
F1	-	G1	GND	H1	-	J1	GND	K1	-
F2	GND	G2	-	H2	-	J2	-	K2	GND
F3	GND	G3	-	H3	GND	J3	-	K3	GND
F4	-	G4	GND	H4	-	J4	GND	K4	-
F5	-	G5	GND	H5	-	J5	GND	K5	-
F6	GND	G6	-	H6	GND	J6	-	K6	GND
F7	UD_IN_C_C	G7	-	H7	CLK_OUT_C	J7	-	K7	-
F8	LD_IN_B_C	G8	GND	H8	MOD_CLK_C	J8	GND	K8	-
F9	-	G9	ADC3_C	H9	GND	J9	-	K9	GND
F10	GND	G10	-	H10	ADC2_C	J10	-	K10	-
F11	LD_IN_A_C	G11	GND	H11	-	J11	GND	K11	-
F12	GND	G12	-	H12	GND	J12	-	K12	GND
F13	SNS_OUT_A_C	G13	-	H13	SNS_OUT_D_C	J13	-	K13	-
F14	SNS_OUT_B_C	G14	GND	H14	SNS_OUT_C_C	J14	GND	K14	-
F15	GND	G15	-	H15	GND	J15	-	K15	GND
F16	-	G16	RESET	H16	-	J16	-	K16	-
F17	-	G17	GND	H17	SM_EN	J17	GND	K17	-
F18	GND	G18	OTW_FAULT	H18	GND	J18	-	K18	GND
F19	BLO4	G19	-	H19	OC_FAULT	J19	-	K19	-
F20	-	G20	GND	H20	PR_FAULT	J20	GND	K20	-
F21	GND	G21	CP_CLK_C	H21	GND	J21	-	K21	GND
F22	-	G22	-	H22	-	J22	-	K22	-
F23	-	G23	GND	H23	DMOD_IN_N_C	J23	GND	K23	SCP
F24	GND	G24	DMOD_IN_P_C	H24	GND	J24	-	K24	GND
F25	-	G25	UD_IN_D_C	H25	LD_IN_D_C	J25	-	K25	-
F26	-	G26	GND	H26	-	J26	GND	K26	-
F27	GND	G27	-	H27	GND	J27	-	K27	GND
F28	-	G28	BLO6	H28	-	J28	-	K28	-
F29	-	G29	-	H29	-	J29	GND	K29	-
F30	GND	G30	BLO5	H30	GND	J30	-	K30	GND
F31	-	G31	BLO3	H31	-	J31	-	K31	-
F32	-	G32	GND	H32	-	J32	GND	K32	-
F33	GND	G33	-	H33	GND	J33	-	K33	GND
F34	-	G34	-	H34	BLO2	J34	-	K34	-
F35	-	G35	GND	H35	BLO1	J35	GND	K35	-
F36	GND	G36	-	H36	GND	J36	-	K36	GND
F37	-	G37	-	H37	-	J37	-	K37	-
F38	-	G38	GND	H38	-	J38	GND	K38	-
F39	GND	G39	VADJ	H39	GND	J39	VIO_B_M2C	K39	GND
F40	VADJ	G40	GND	H40	VADJ	J40	GND	K40	VIO_B_M2C

Table 17. LX7720 Control and Acquisition Signals Header J20 Pinout

Pin	Signal Name	Signal Function	Pin	Signal Name	Signal Function
1	UD_IN_A_C	Buffered UD_IN_A FET drive input	2	LD_IN_A_C	Buffered LD_IN_A FET drive input
3	SNS_OUT_A_C	Buffered SNS_OUT_A bit stream output	4	GND	Ground
5	UD_IN_B_C	Buffered UD_IN_B FET drive input	6	LD_IN_B_C	Buffered LD_IN_B FET drive input
7	SNS_OUT_B_C	Buffered SNS_OUT_B bit stream output	8	GND	Ground
9	UD_IN_C_C	Buffered UD_IN_C FET drive input	10	LD_IN_C_C	Buffered LD_IN_C FET drive input
11	SNS_OUT_C_C	Buffered SNS_OUT_C bit stream output	12	GND	Ground
13	UD_IN_D_C	Buffered UD_IN_D FET drive input	14	LD_IN_D_C	Buffered LD_IN_DFET drive input
15	SNS_OUT_D_C	Buffered SNS_OUT_D bit stream output	16	GND	Ground
17	CP_CLK_C	Buffered CP_PLK charge pump clock input	18	MOD_CLK_C	Buffered MOD_CLK mod clock input
19	CLK_OUT_C	Buffered CLK_OUT mod clock output	20	GND	Ground
21	DMOD_IN_P_C	Buffered DMOD_IN_P drive input	22	DMOD_IN_N_C	Buffered DMOD_IN_N drive input
23	ADC1_C	Buffered ADC1 bit stream output	24	GND	Ground
25	ADC2_C	Buffered ADC2 bit stream output	26	ADC3_C	Buffered ADC3 bit stream output
27	SM_EN	SM_EN input via J39 link header	28	GND	Ground
29	SCP	SCP input via J38 link header	30	VDD_3P3V	VDD supply, normally 3.3V
31	RESET	RESET input via J40 link header	32	OC_FAULT	OC_FAULT output
33	PR_FAULT	PR_FAULT output	34	OTW_FAULT	OTW_FAULT output
35	BLO1	Bi-Level Detector output 1	36	BLO2	Bi-Level Detector output 2
37	BLO3	Bi-Level Detector output 3	38	BLO4	Bi-Level Detector output 4
39	BLO5	Bi-Level Detector output 5	40	BLO6	Bi-Level Detector output 6

6 Complete Schematics

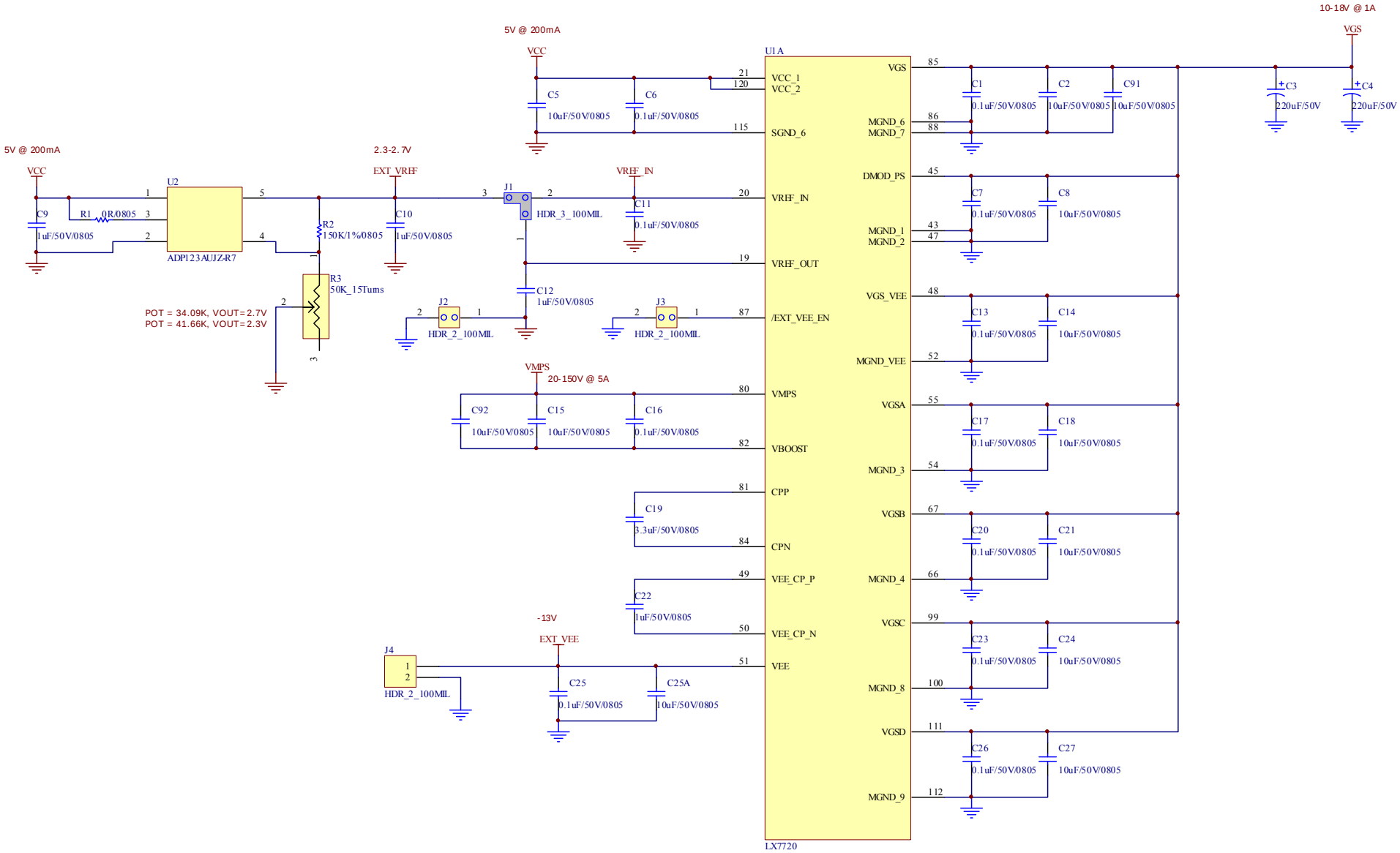


Figure 22. Power Connection

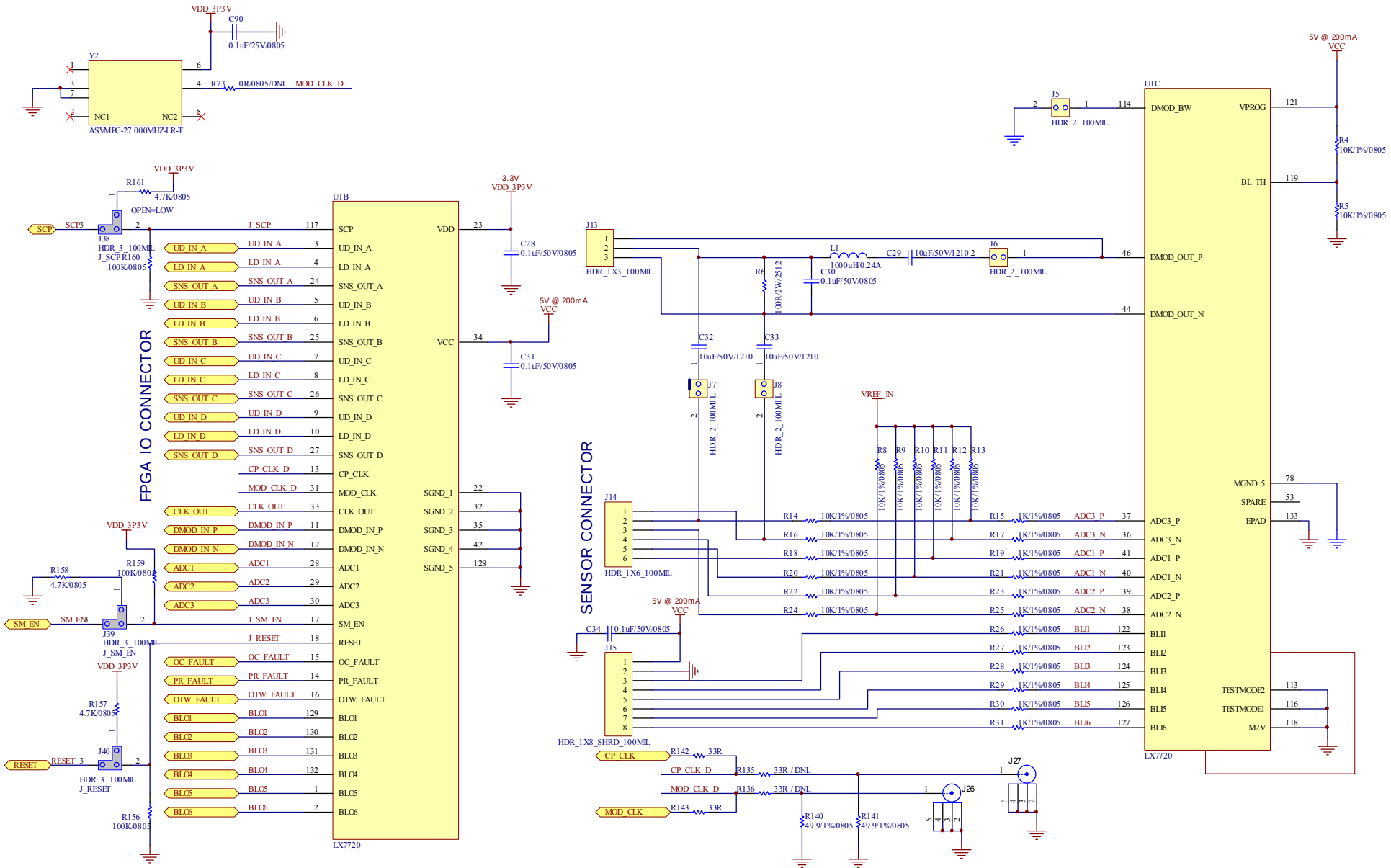


Figure 23. FPGA and Sensor Connection

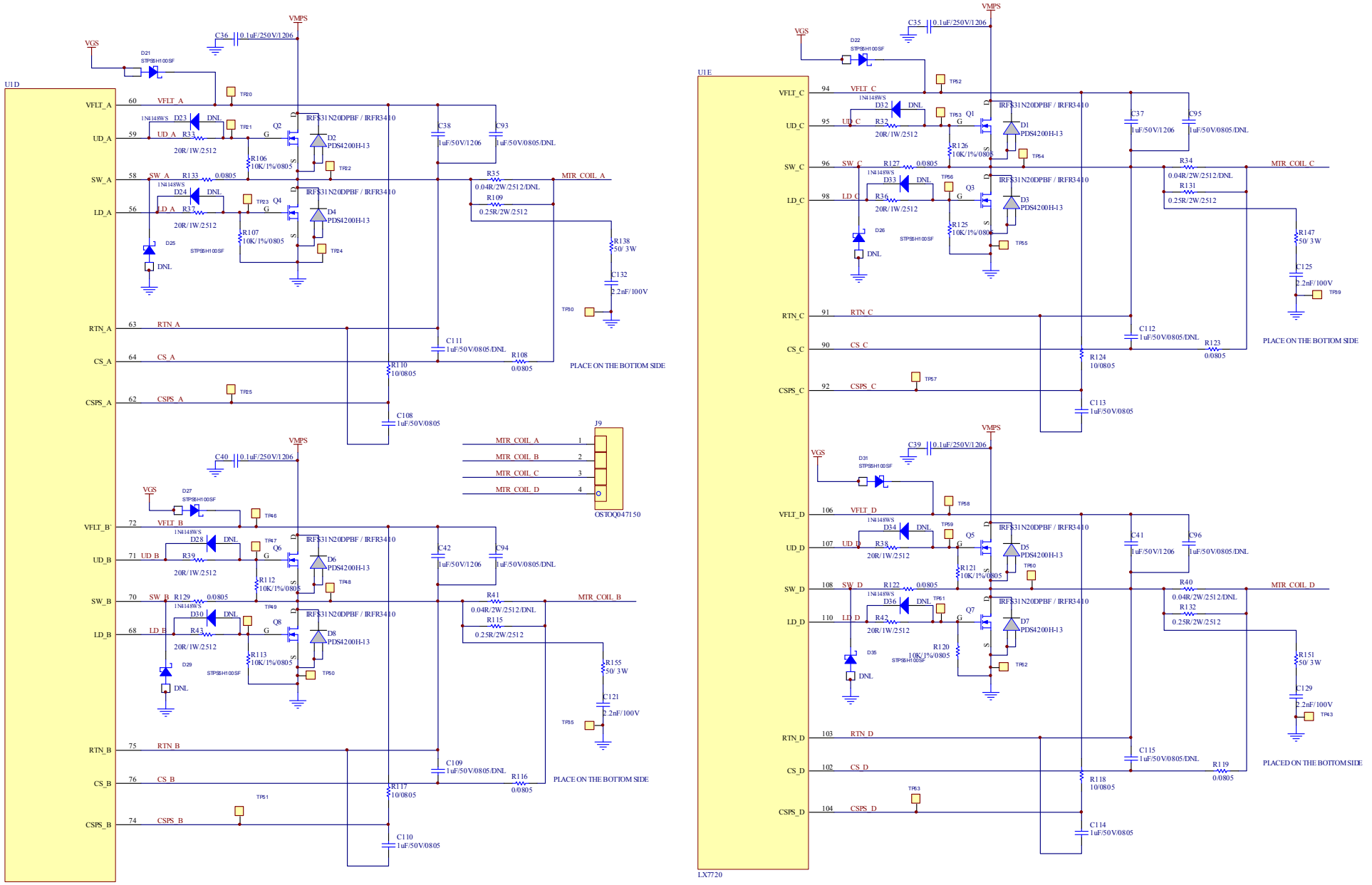


Figure 24. Motor/Driver Connection

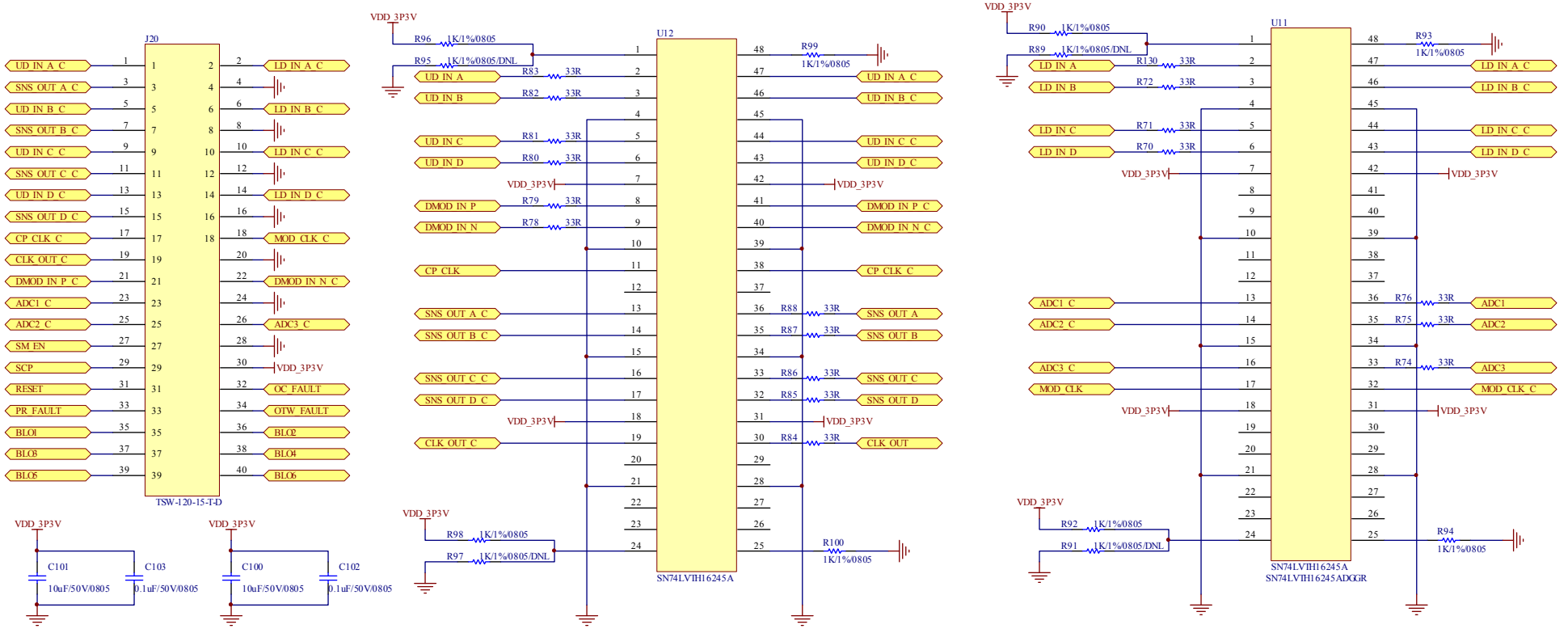


Figure 25. Line Drivers and Dual Row Header

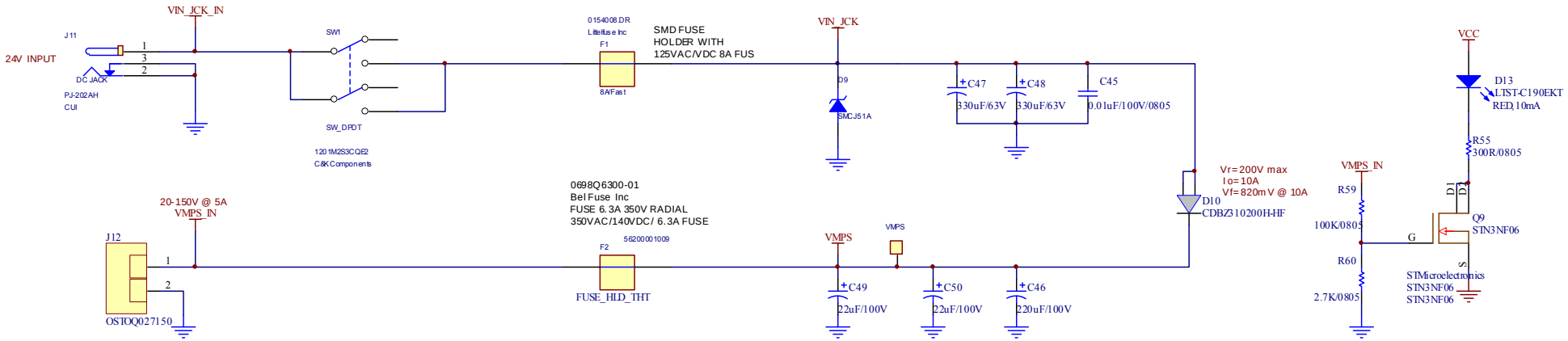


Figure 26. Power Section

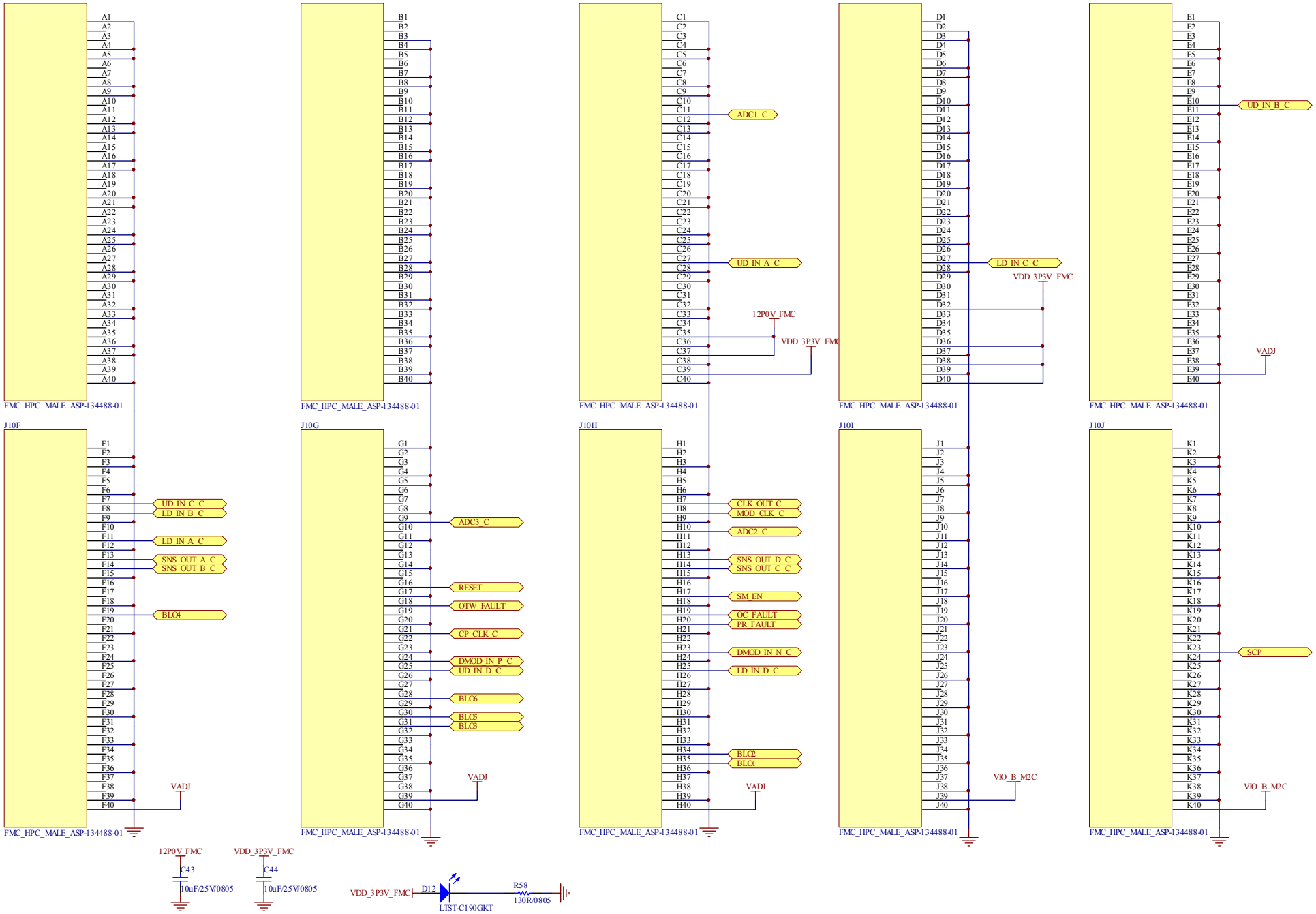


Figure 27. FMC Connector to RTG4 Board

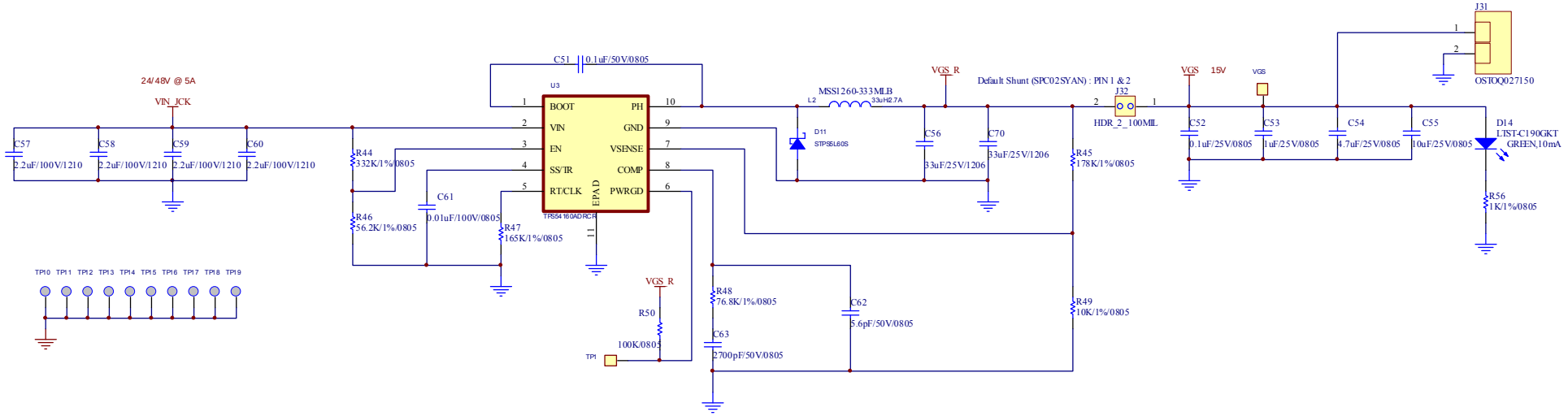


Figure 28. 50V Input to 15V Regulator

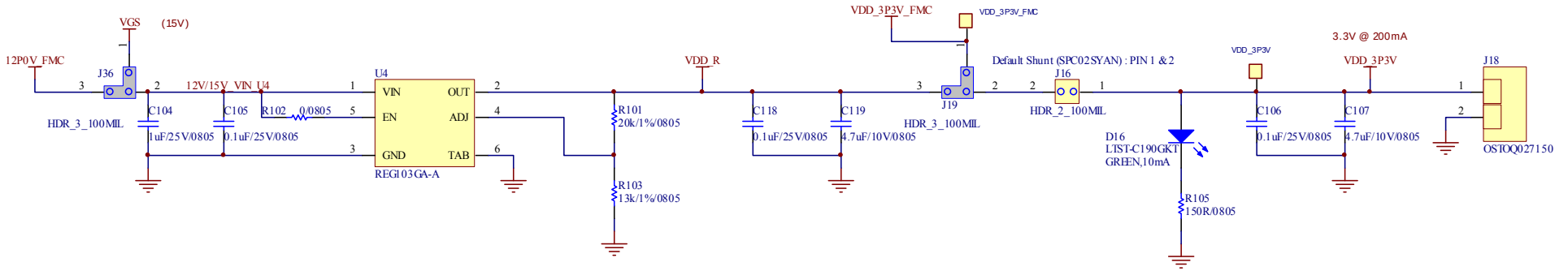


Figure 29. 12V to 15V Input to 3.3V Regulator

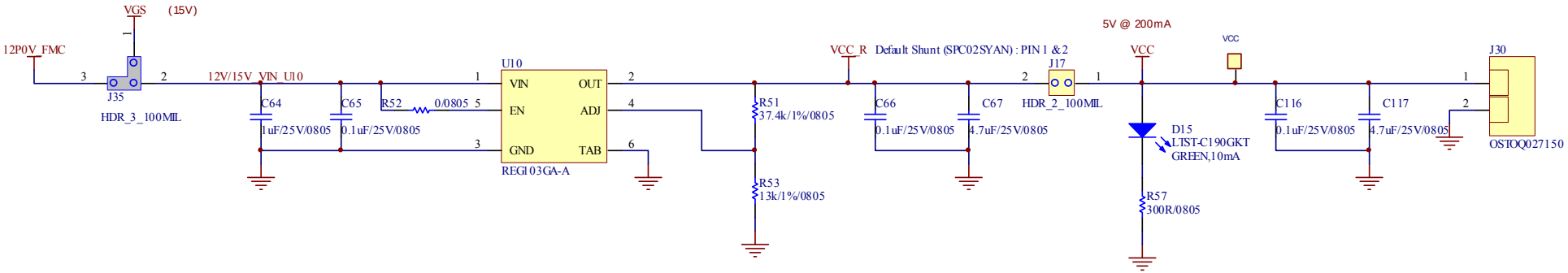


Figure 30. 12V to 15V Input to 5V Regulator

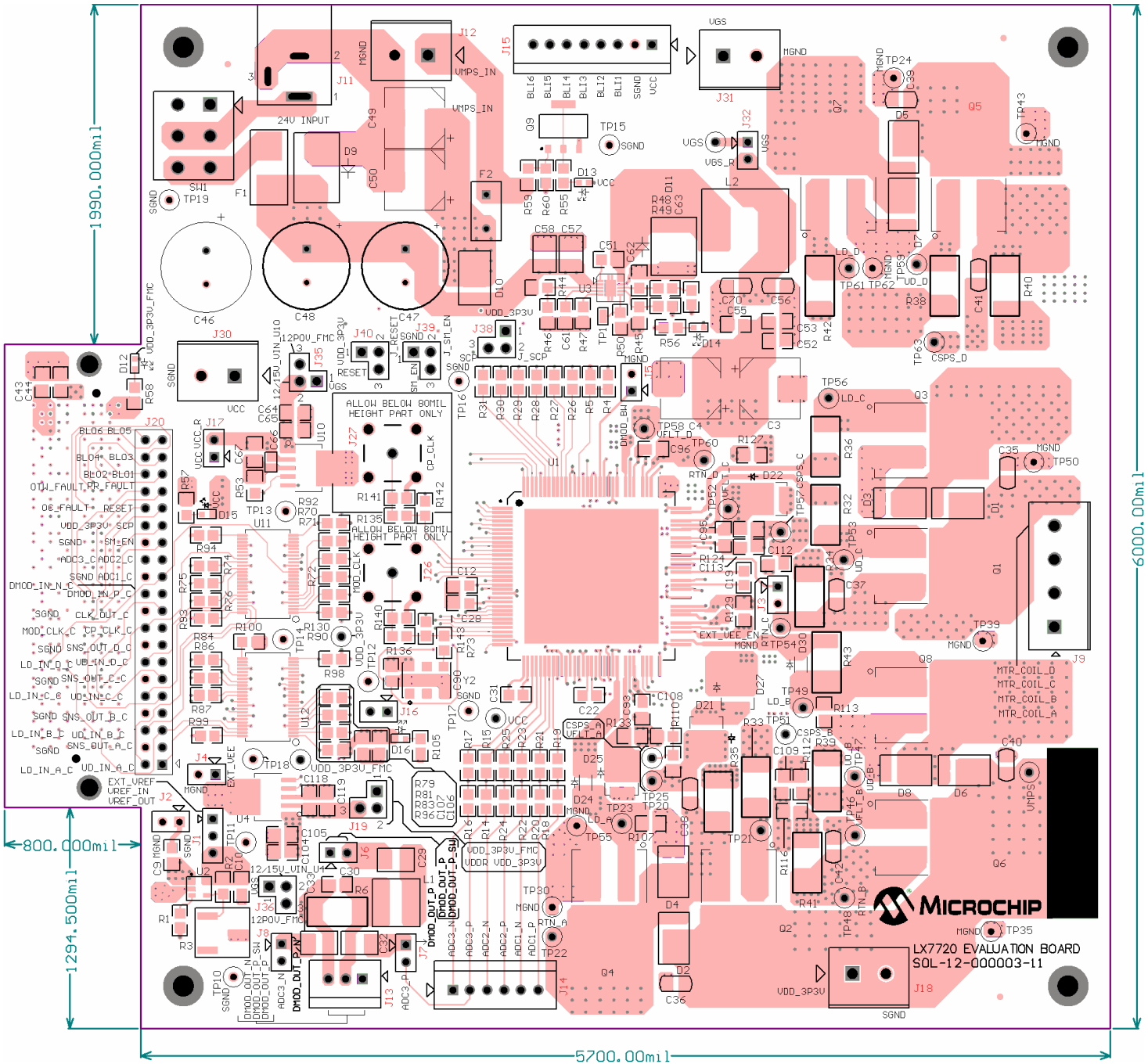


Figure 31. PCB Top copper layer 1 and component IDs

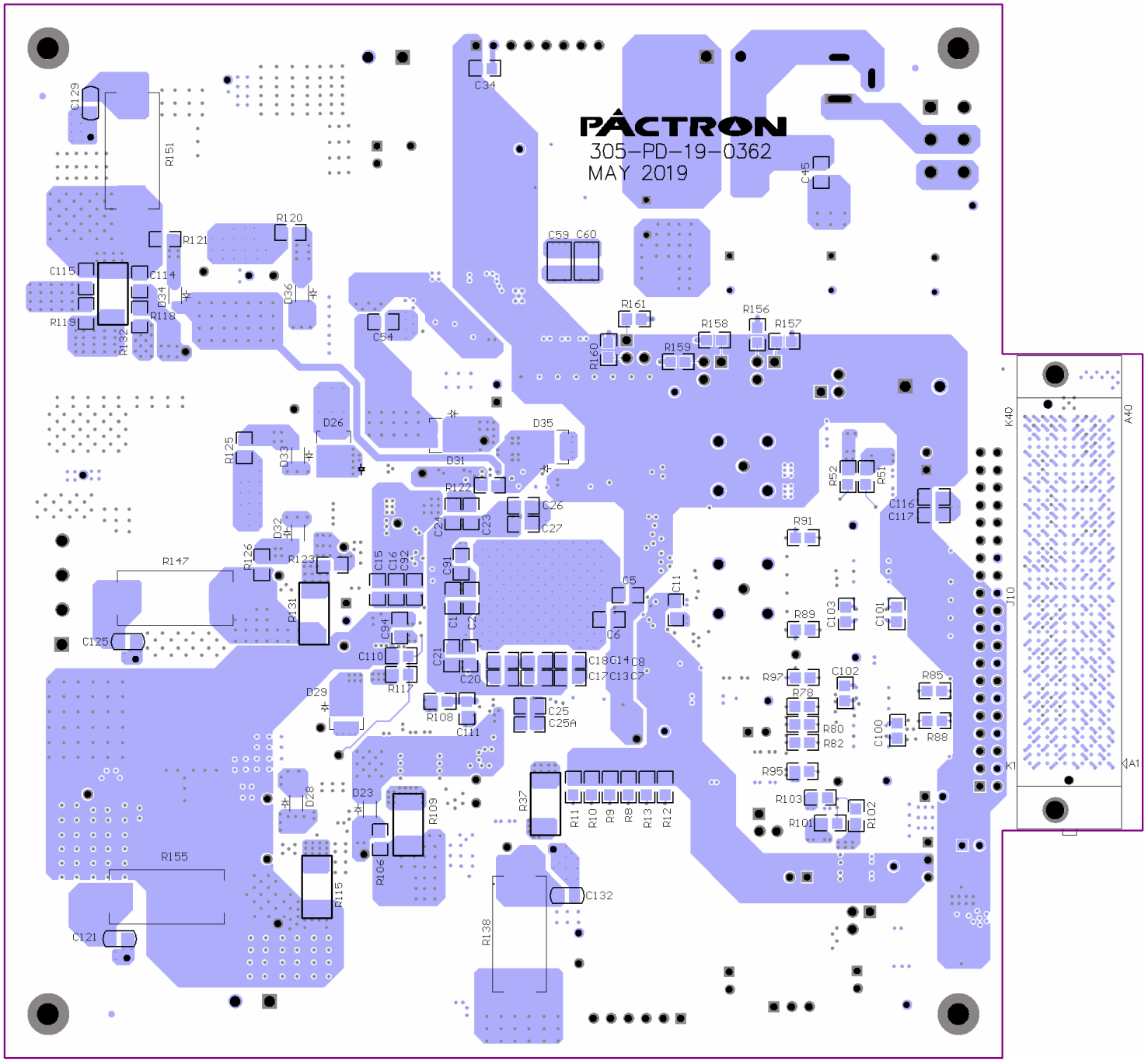


Figure 32. PCB Bottom copper layer and component IDs (bottom view)

7 PCB Parts List

Table 18. Bill of Materials

Designator	Value	Footprint	Part Number	Manufacturer	Description
C1, C6, C7, C13, C17, C20, C23, C25, C26, C28, C30, C31, C34, C51, C103	0.1uF/50V/0805	C0805	C0805C104M5RACTU	KEMET	CAP CER 0.1UF 50V X7R 0805
C2, C5, C8, C14, C15, C18, C21, C24, C25A, C27, C91, C92	10uF/50V/0805	C0805	C2012X5R1V106K125AC	TDK	CAP CER 10UF 35V X5R 0805
C3, C4	220uF/50V	UCM1H221MNL1GS	UCM1H221MNL1GS	Nichicon	CAP ALUM 220UF 20% 50V SMD
C9, C10, C22	1uF/50V/0805	C0805	CL21B105KBFNNNG	Samsung	CAP CER 1UF 50V X7R 0805
C11	0.1uF/50V/0805	C0805	CL21B104KBCSFNC	Samsung	CAP CER 0.1UF 50V X7R 0805
C12	1uF/50V/0805	C0805	CL21B105KBFNNNG	Samsung	CAP CER 1UF 50V X7R 0805
C16	0.1uF/50V/0805	C0805	GRM21BR71H104KA01L	Murata	CAP CER 0.1UF 50V X7R 0805
C19	3.3uF/50V/0805	C0805	C2012X5R1H335K125AB	TDK	CAP CER 3.3UF 50V X5R 0805
C29, C32, C33	10uF/50V/1210	C1210	CL32B106KBJNNWE	Samsung	CAP CER 10UF 50V X7R 1210
C35, C36, C39, C40	0.1uF/250V/1206	C1206	GRM31CR72E104KW03L	Murata	CAP CER 0.1UF 250V X7R 1206
C37, C38, C41, C42	1uF/50V/1206	C1206	CL31B105KBHNNNE	Samsung	CAP CER 1UF 50V X7R 1206
C43, C44, C55	10uF/25V/0805	C0805	CL21A106KAYNNNE	Samsung	CAP CER 10UF 25V 10% X5R 0805
C45, C61	0.01uF/100V/0805	C0805	C0805C103K1RACTU	Kemet	CAP CER 10000PF 100V X7R 0805
C46	220uF/100V	UVY2A221MHD1TO	UVY2A221MHD1TO	Nichicon	CAP ALUM 220UF 20% 100V RADIAL
C47, C48	330uF/63V	EEU-FR1J331B	EEU-FR1J331B	Panasonic	CAP ALUM 330UF 63V 20% RADIAL
C49, C50	22uF/100V	UUX2A220MNL6GS	UUX2A220MNL6GS	Nichicon	CAP ALUM 22UF 20% 100V SMD
C52, C65, C66, C90, C116	0.1uF/25V/0805	C0805	CC0805KRX7R8BB104	Yageo	CAP CER 0.1UF 25V X7R 0805
C53, C64, C104	1uF/25V/0805	C0805	CL21B105KAFNNNE	Samsung	CAP CER 1UF 25V X7R 0805
C54, C67, C117	4.7uF/25V/0805	C0805	CL21B475KAFNNNE	Samsung	CAP CER 4.7UF 25V X7R 0805
C56, C70	33uF/25V/1206	C1206	C3216X5R1E336M160AC	TDK	CAP CER 33UF 25V X5R 1206
C57, C58, C59, C60	2.2uF/100V/1210	C1210	C3225X7R2A225K230AB	TDK	CAP CER 2.2UF 100V 10% X7R 1210
C62	5.6pF/50V/0805	C0805	C0805C569D5GACTU	KEMET	CAP CER 5.6PF 50V C0G/NP0 0805
C63	2700pF/50V/0805	C0805	CL21B272KBANNNC	Samsung	CAP CER 2700PF 50V X7R 0805
C93, C94, C95, C96, C109, C111, C112, C115	1uF/50V/0805/DNL	C0805	CL21B105KBFNNNE	Samsung	CAP CER 1UF 50V X7R 0805
C100, C101	10uF/50V/0805	C0805	CC0805KKX5R9BB106	Yageo	CAP CER 10UF 50V X5R 0805
C102	0.1uF/50V/0805	C0805	CL21B104KBCSFNC	Samsung	CAP CER 0.1UF 50V X7R 0805
C105, C106, C118	0.1uF/25V/0805	C0805	C0805C104M5RACTU	KEMET	CAP CER 0.1UF 50V X7R 0805
C107, C119	4.7uF/10V/0805	C0805	CL21B475KPFNNNE	Samsung	CAP CER 4.7UF 10V X7R 0805
C108, C110, C113, C114	1uF/50V/0805	C0805	CL21B105KBFNNNE	Samsung	CAP CER 1UF 50V X7R 0805
C121, C125, C129, C132	2.2nF/100V	C1206	LDEEA1220JA0N00	KEMET	CAP FILM 2200PF 5% 100VDC 1206
D1, D2, D3, D4, D5, D6, D7, D8	PDS4200H-13	POWERDI5_PDS4200H	PDS4200H-13	Diodes	DIODE SCHOTTKY 200V 4A POWERDI5
D9	SMCJ51A	DO-214AB_SMCJ	SMCJ51A	Fairchild	TVS DIODE 51VWM 82.4VC SMC
D10	CDBZ310200H-HF	TO277_CDBZ310200H	CDBZ310200H-HF	Comchip	DIODE SCHOTTKY 200V 10A TO277
D11	STPS5L60S	DO-214AB_STPS5	STPS5L60S	STM	DIODE SCHOTTKY 60V 5A SMC
D12, D14, D15, D16	LTST-C190GKT	LED0603	LTST-C190GKT	LITEON	LED GREEN CLEAR 0603 SMD
D13	LTST-C190EKT	LED0603	LTST-C190EKT	Lite-On	LED RED CLEAR 0603 SMD
D21, D22, D27, D31	STPS5H100SF	TO-277_STPS5H	STPS5H100SF	STM	100V POWER SCHOTTKY RECTIFIER
D23, D24, D28, D30, D32, D33, D34, D36	1N4148WS	SOD323F_1N4148	1N4148WS	ON	DIODE GEN PURP 75V 150MA SOD323F
D25, D26, D29, D35	STPS5H100SF	TO-277_STPS5H	STPS5H100SF	STM	100V POWER SCHOTTKY RECTIFIER
F1	8A/ Fast	FUSE_SMD_HLDR_8A_0154008	0154008.DR	Littelfuse	FUSE BRD MNT 8A 125VAC/VDC 2SMD
F2	FUSE_HLD_THT	FUSE_THT_HLDX2_5620	56200001009	Littelfuse	FUSE HOLDER RADIAL 250V 6.3A PCB
FUSE(6.3AMP 350VAC/140VDC)	For F2		0698Q6300-01	Bel Fuse	FUSE 6.3A 350V RADIAL -THT
J1	HDR_3_100MIL	HDR_3_100MIL_THT	TSW-103-08-G-S	Samtec	CONN HEADER 3POS .100 SNGL GOLD"
J2, J3, J4, J5, J6, J7, J8, J16, J17, J32	HDR_2_100MIL	HDR_2_100MIL_T	TSW-102-08-G-S	Samtec	CONN HEADER 2POS .100 SNGL GOLD"
J9	OSTOQ047150	OSTOQ047150	OSTOQ047150	On Shore	TERM BLOCK HDR 4POS VERT 5MM

Designator	Value	Footprint	Part Number	Manufacturer	Description
J10	FMC_HPC_MALE_ASP-134488-01	FMC_HPC_MALE_ASP-134488-01	ASP-134488-01	Samtec	CONN SNGL-END ARRAY MALE 400POS
J11	DC JACK	PJ-202AH_JACK	PJ-202AH	CUI Inc.	CONN PWR JACK 2X5.5MM KINKED PIN
J12, J18, J30, J31	OSTOQ027150	OSTOQ027150	OSTOQ027150	On Shore	TERM BLOCK HDR 2POS VERT 5MM
J13	HDR_1X3_100MIL	HDR_1X3_SHRD_100MIL_THT	705430002	Molex	3 Positions Header, Shrouded Connector 0.100 (2.54mm) Through Hole Gold"
J14	HDR_1X6_100MIL	HDR_1X6_SHRD_100MIL_THT	705430005	Molex	6 Positions Header, Shrouded Connector 0.100 (2.54mm) Through Hole Gold"
J15	HDR_1X8_100MIL	HDR_1X8_SHRD_100MIL_THT	705430007	Molex	8 Positions Header, Shrouded Connector 0.100 (2.54mm) Through Hole Gold"
J19, J35, J36, J38, J39, J40	HDR_3_100MIL	HDR_3_100MIL_L	Regular 100MIL breakaway header		Break the header and install in 'L' shape
J20	HDR_THT_2X20	HDR_THT_2X20	TSW-120-15-T-D	Samtec	CONN HEADER VERT 40POS 2.54MM
J26, J27	142-0701-211	142-0701-211	142-0701-211	Cinch	CONN SMA JACK STR 50 OHM PCB
L1	1000uH/0.24A	6X6MM_LPS6225	LPS6225-105MRB	Coilcraft	Fixed Inductors LPS6225 Low Profile 1000uH 0.24A 20%SMD
L2	33uH/2.7A	12P3x12P3MM_MSS1260	MSS1260-333MLB	Coilcraft	Fixed Inductors MSS1260 SMT Power 33 uH 20 % 2.7 A
Q1, Q2, Q3, Q4, Q5, Q6, Q7, Q8	IRFS31N20DPBF or IRFR3410	D2PAK_DPAK_DUAL_FOOTPRINT	IRFS31N20DPBF or IRFR3410TRLPBF	Infineon	MOSFET N-CH 200V 31A D2PAK / MOSFET N-CH 100V 31A DPAK
Q9	STN3NF06	SOT-223_STN3NF06	STN3NF06	STM	MOSFET N-CH 60V 4A SOT-223
R1	0R/0805	R0805	RC0805JR-070RL	Yageo	RES 0 OHM JUMPER 1/8W 0805
R2	150K/1%/0805	R0805	CRCW0805150KFKEA	Vishay	RES SMD 150K OHM 1% 1/8W 0805
R3	50K_15Turns (Set to 34.09KΩ)	6p85mmx5mm_POT_50K	TS63Y503KR10	Vishay	TRIMMER 50K OHM 0.25W SMD
R4, R5, R8, R9, R10, R11, R12, R13, R14, R16, R18, R20, R22, R24, R49	10K/1%/0805	R0805	Y162910K0000F9R	Vishay	RES SMD 10K OHM 1% 1/10W 0805
R6	100R/2W/2512	R2512	RHC2512FT100R	Stackpole	RES SMD 100 OHM 1% 2W 2512
R15, R17, R19, R21, R23, R25, R26, R27, R28, R29, R30, R31, R56	1K/1%/0805	R0805	ERA-6AEB102V	Panasonic	RES SMD 1K OHM 0.1% 1/8W 0805
R32, R33, R36, R37, R38, R39, R42, R43	20R/1W/2512	R2512	RMCF2512FT20R0	Stackpole	RES 20 OHM 1% 1W 2512
R34, R35, R40, R41	0.04R/2W/2512/DNL	R2512	CSRN2512FK40L0	Stackpole	RES SMD 0.04 OHM 1% 2W 2512
R44	332K/1%/0805	R0805	RC0805FR-07332KL	Yageo	RES SMD 332K OHM 1% 1/8W 0805
R45	178K/1%/0805	R0805	ERA-6AEB1783V	Panasonic	RES SMD 178K OHM 0.1% 1/8W 0805
R46	56.2K/1%/0805	R0805	RC0805FR-0756K2L	Yageo	RES SMD 56.2K OHM 1% 1/8W 0805
R47	165K/1%/0805	R0805	RC0805FR-07165KL	Yageo	RES SMD 165K OHM 1% 1/8W 0805
R48	76.8K/1%/0805	R0805	RC0805FR-0776K8L	Yageo	RES SMD 76.8K OHM 1% 1/8W 0805
R50	100K/0805	R0805	RC0805FR-07100KL	Yageo	RES SMD 100K OHM 1% 1/8W 0805
R51	37.4k/1%/0805	R0805	RMCF0805FT37K4	Stackpole	RES 37.4K OHM 1% 1/8W 0805
R52, R102, R108, R116, R119, R122, R123, R127, R129, R133	0/0805	R0805	RMCF0805ZT0R00	Stackpole	RES 0 OHM JUMPER 1/8W 0805
R53, R103	13k/1%/0805	R0805	RG2012P-133-B-T5	Susumu	RES SMD 13K OHM 0.1% 1/8W 0805
R55, R57	300R/0805	R0805	RC0805FR-07300RL	Yageo	RES SMD 300 OHM 1% 1/8W 0805
R58	130R/0805	R0805	RC0805FR-07130RL	Yageo	RES SMD 130 OHM 1% 1/8W 0805
R59, R156, R159, R160	100K/0805	R0805	ERA-6AEB104V	Panasonic	RES SMD 100K OHM 0.1% 1/8W 0805
R60	2.7K/0805	R0805	ERA-6AEB272V	Panasonic	RES SMD 2.7K OHM 0.1% 1/8W 0805
R70, R71, R72, R74, R75, R76, R78, R79, R80, R81, R82, R83, R84, R85, R86, R87, R88, R130, R142, R143	33R	R0805	CRCW080533R0FKEAC	Vishay	RES 33 OHM 1% 1/8W 0805
R73	0R/0805/DNL	R0805	CRCW08050000Z0EBC	Vishay	RES 0 OHM JUMPER 1/8W 0805
R89, R91, R95, R97	1K/1%/0805/DNL	R0805	CRCW08051K00FKEA	Vishay	RES SMD 1K OHM 1% 1/8W 0805
R90, R92, R93, R94, R96, R98, R99, R100	1K/1%/0805	R0805	CRCW08051K00FKEA	Vishay	RES SMD 1K OHM 1% 1/8W 0805

Designator	Value	Footprint	Part Number	Manufacturer	Description
R101	20k/1%/0805	R0805	RG2012P-203-B-T5	Susumu	RES SMD 20K OHM 0.1% 1/8W 0805
R105	150R/0805	R0805	RNCP0805FTD150R	Stackpole	RES 150 OHM 1% 1/4W 0805
R106, R107, R112, R113, R120, R121, R125, R126	10K/1%/0805	R0805	RC0805FR-0710KL	Yageo	RES SMD 10K OHM 1% 1/8W 0805
R109, R115, R131, R132	0.25R/2W/2512	R2512	RHC2512FTR250	Stackpole	RES 0.25 OHM 1% 2W 2512
R110, R117, R118, R124	10/0805	R0805	RNCP0805FTD10R0	Stackpole	RES 10 OHM 1% 1/4W 0805
R135, R136	33R / DNL	R0805	CRCW080533R0FKEAC	Vishay	RES 33 OHM 1% 1/8W 0805
R138, R147, R151, R155	50/ 3W	R6227	SM6227FT50R0	Stackpole	RES 50 OHM 1% 3W 6227
R140, R141	49.9/1%/0805	R0805	RC0805FR-0749R9L	Yageo	RES SMD 49.9 OHM 1% 1/8W 0805
R157, R158, R161	4.7K/0805	R0805	RC0805JR-074K7L	Yageo	RES SMD 4.7K OHM 5% 1/8W 0805
SW1	SW_DPDT	SW_DPDT_1201	1201M2S3CQE2	C&K	SWITCH SLIDE MINI DPDT PC 120V
TP1	TPAD	TP_0603	1625854-3	TE	0603 PROBE PAD
TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19	TEST_POINT	TP_THT	5001	Keystone	PC TEST POINT MINIATURE BLACK
TP20, TP21, TP22, TP23, TP24, TP25, TP30, TP35, TP39, TP43, TP46, TP47, TP48, TP49, TP50, TP51, TP52, TP53, TP54, TP55, TP56, TP57, TP58, TP59, TP60, TP61, TP62, TP63, VCC, VDD_3P3V, VDD_3P3V_FMC, VGS, VMPS	TEST_POINT	TP_TH	5000	Keystone	PC TEST POINT MINIATURE RED
U1	LX7720	LX7720_CQFP132L	LX7720-ES	Microsemi	IC
U2	ADP123AUJZ-R7	TSOT23-5_ADP123	ADP123AUJZ-R7	ADI	IC REG LIN POS ADJ 300MA TSOT5
U3	TPS54160ADRCR	10SON_TPS54160A	TPS54160ADRCR	TI	IC REG BUCK ADJ 1.5A 10VSON
U4, U10	REG103GA-A	SOT223_ REG103GA	REG103GA-A	TI	IC REG LIN POS ADJ 500MA SOT223
U11, U12	SN74LVTH16245A	SN74LVT_48TSSOP	SN74LVTH16245ADGGR	TI	IC TXRX NON-INVERT 3.6V 48TSSOP
Y2	ASVMPC-27.000MHZ-LR-T	ASVMPC-27_000MHZ-LR-T	ASVMPC-27.000MHZ-LR-T	Abracon	OSC MEMS 27.000MHZ CMOS SMD

These components are not fitted

8 Change Log

Date	Issue	Part Type
2018-10-21	1	Initial release
2020-3-12	2	Update to revised EVB version SOL-12-000003-11
2020-6-4	2.1	Added reference to SAMV71Q21RT MCU, and separated hotlinks for product pages and EV board pages. Added SAMRH71F20-EK flexi connector information. Added FMC connectivity information to the PolarFire FPGA Evaluation Kit. Corrected reference to 3.3V to be 5V in Table 4. Corrected 'External' to 'Internal' on last row Table 8

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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