Microsemi Corporation: PCN18009

July 13, 2018

Product/Process Change Notification No: PCN18009

Change Classification: Major

Subject: RTG4 Family Important Changes

Summary: This document describes six Product Change Notifications (PCN) and two Customer Advisory Notices (CAN), and one Customer Notification (CN) for the RTG4 product family. A summary of the notifications can be found in the following table.

Notification	Description
PCN18009.1	RTG4 LSRAM ECC Errors
PCN18009.2	RTG4 SERDES REFCLK LVPECL Jitter
PCN18009.3	RTG4 MSIO LVPECL/LVDS33 Input Buffer Jitter on Fabric Clock
CAN18009.4	RTG4 Fabric DDR (FDDR) Controller Documentation
CAN18009.5	Synopsys Synplify Safe FSM Setting Change
PCN18009.6	RTG4 Timing Changes
PCN18009.7	RTG4 PLL in Internal Feedback Mode (TMR Mode)
CN18009.8	RTG4 CCC Simulation False Failures
PCN18009.9	Incorrect CoreFIFO Empty Flag Timing in Specific RTG4 Configuration

PCN18009.1 RTG4 LSRAM ECC Errors

Description of Change

In certain circumstances, RTG4 LSRAM can experience data corruption and ECC flag false positive indications.

When RTG4 LSRAM blocks are configured in non-pipelined ECC mode, without SET mitigation enabled, a timing issue in the LSRAM ECC circuits can generate incorrect ECC code words and in turn allow read-back of falsely corrected data and flag outputs. The following SRAM modes are **not** affected:

- LSRAM without ECC enabled
- LSRAM with pipelined ECC mode
- LSRAM with non-pipelined ECC mode **and** SET mitigation enabled
- uSRAM in any use mode

Microsemi will remove support for LSRAM non-pipelined ECC mode without SET mitigation from documentation and Libero software starting with Libero SoC v11.9 (available in August 2018). In addition, Microsemi will update the RTG4 LSRAM documentation explaining that ECC flag outputs are invalid whenever the RAM is not in an active read data out cycle or whenever the BLK select signal is de-asserted. Microsemi will also introduce features in the Libero SoC v11.9 LSRAM configurator to generate logic that gates-off ECC flags for inactive LSRAM blocks and to ensure that simulation shows ECC flags as unknown when not in valid data out clock cycle or when BLK is de-asserted.

Application Impact

This can lead to corruption of data and ECC flag outputs read from non-pipelined LSRAM blocks.

Action Required

Designers have two options to prevent this corruption of LSRAM data:

- Use CoreEDAC to perform ECC in the programmable logic fabric instead of using the built-in ECC in LSRAM blocks; or
- Turn on SET mitigation for LSRAM blocks using either ECC mode (pipelined or non-pipelined), recompile designs and repeat static timing analysis. Microsemi recommends using SET mitigation with ECC as the best practice for protection from radiation effects.
  - Can be applied at LSRAM instance level using NDC constraint (works today in Libero SoC v11.8 SP3):
    `set_mitigation –inst_name <instance_name> -mitigate <yes, or 1, or true>`
    - Documented in http://coredocs.s3.amazonaws.com/Libero/11_8_0/Tool/pdc_ug.pdf
    - Supports wildcard and hierarchical instance names; enables mitigation on all instance types capable of SET mitigation (SLE, MATH)
  - Can be applied globally at the project level, but will negatively impact entire design timing (works today in Libero SoC v11.8 SP3) Project menu -> Project Settings… -> Device Settings
  - Can be applied manually by statically connecting LSRAM input port DELEN to ‘1’ (requires Libero SoC v11.9, scheduled to be released August 2018)
  - Can be applied via inference during synthesis using Synplify Pro synthesis directive syn_ramstyle with value “lsram, ecc,set” (requires Libero SoC v11.9, scheduled to be released in August 2018)

Products Effected by this Change

See Appendix A.

PCN18009.2 RTG4 SERDES REFCLK LVPECL Jitter

Description of Change

Under specific circumstances, higher jitter has been observed on SERDES output data (TXD) when the SERDES REFCLK receiver is operated in 3.3 V LVPECL mode.

The triple-redundant input buffers used in the SERDES REFCLK MSIO inputs can generate more jitter than permitted by various serial protocols. This occurs when the RTG4 REFCLK receiver input differential voltage (V_{ID}) is lower than the input common mode voltage (V_{ICM}), combined with junction temperature lower than 25°C.

Table 1 • Worst-Case Jitter Values

	LVPECL[3]			**LVDS33[3]**			**LVDSV25, HCSL, LVCMOS25**
Tj range (C)	-55 °C to 125 °C	25°C to 125 °C	-55 °C to 125 °C	-55 °C to 125 °C	25 °C to 125 °C	-55 °C to 125 °C	-55 °C to 125 °C
Worst-case total transmit jitter (ps)	360	80	107	360	80	107	100
V_{ICM}[1]	0.6 V–1.8 V	0.6 V–1.8 V	0.6 V–1.8 V[2]	0.6 V–1.8 V	0.6 V–1.8 V	0.6 V–1.8 V[2]	See corresponding DC table.
V_{ID}[1]	0.6–2.4 V	0.6 V–2.4 V	0.6 V–2.4 V[2]	0.5 V–2.4 V	0.5 V–2.4 V	0.6 V–2.4 V[2]	See corresponding DC table.
Restriction	None	Restricted operating temp. range	V_{ID}>=V_{ICM} per note 2	None[4]	Restricted operating temp. range	V_{ID}>=V_{ICM} per note 2	See corresponding DC table.

Notes:

1. $V_{ICM} + (V_{ID}/2) < V_{DDI} + 0.4$ V and $V_{ICM} – (V_{ID}/2) >= –0.3$ V
2. $V_{ID} >= V_{ICM}$
3. For the lowest possible jitter on SERDES TX outputs running at 3.125 Gbps across the full mil-temp range, use LVDS25 differential inputs for the SERDES REFCLK receiver with SERDES_VDDI set to 2.5 V and design the interface to meet a minimum V_{ICM} of 600 mV.
4. If no measures are taken, such as limiting operating temperature range, or meeting $V_{ID} >= V_{ICM}$ relationship, then the SERDES will still start up at -55 °C to 25 °C range, but the maximum total transmit jitter could exceed the TX jitter limits of the serial protocol in use until T_j rises to >=25 °C.

Application Impact

If junction temperature is below 25 °C and V_{ID} is lower than V_{ICM}, the jitter observed on the SERDES TX data outputs may exceed acceptable levels for the system.

Action Required

If the FPGA junction temperature is 25 °C or higher when SERDES is required to operate, then no action is required.
If VID is equal to or greater than VICM when the SERDES is required to operate, then no action is required.
If the FPGA junction temperature is lower than 25 °C and VID is lower than VICM when the SERDES is required to operate, then designers should evaluate whether their serial protocol can operate with the elevated TX data jitter as described in the preceding table. If the jitter levels described in the preceding table are not acceptable, then the REFCLK connection on the board must be adjusted so that V_{ID} >= V_{ICM} at the RTG4 SERDES REFCLK receiver. Depending on the board configuration for the SERDES REFCLK connection, this can be accomplished by tuning an external termination resistor network, if one exists, at the RTG4 SERDES REFCLK differential input. If the connection to the RTG4 SERDES REFCLK receiver does not have any external termination, then a board change would be required to either add external termination, or change to another I/O standard for the SERDES REFCLK receiver.

Products Affected by this Change

See Appendix A.

PCN18009.3 RTG4 MSIO LVPECL/LVDS33 Input Buffer Jitter on Fabric Clock Inputs

Description of Change

Under specific circumstances, the RTG4 MSIO 3.3V LVPECL/LVDS33 input buffer can induce extra jitter on signals entering the FPGA fabric. The extra jitter can cause concern for critical signals such as clocks which directly drive fabric logic or which provide the reference clock to the fabric PLL. This issue is exacerbated in RTG4 due to the triple-redundant input buffers used in the MSIO input buffer. The extra input buffer jitter occurs when the LVPECL/LVDS33 input differential voltage (V_{ID}) is lower than the input common mode voltage (V_{ICM}), combined with junction temperature lower than 25 °C.

In the case of an input reference clock that drives a fabric PLL, the CCC output clock sourced from the PLL will have a max period jitter (peak-to-peak) that depends on the I/O standard, operating temperature range, and V_{ID} versus V_{ICM} relationship for differential inputs. This updated specification will be added to Revision 5 of the RTG4 Datasheet, as shown in the following table.

Table 2 • RTG4 FPGAs Fabric PLL Output Clock Jitter Specification

Ref Clock I/O Standard	Input Voltage Condition	Operating Temperature	Max Output Clock Jitter (peak-to-peak period jitter)	Unit
Single-ended and Voltage Referenced	N/A	-55°C ≤ T_j ≤ 125 °C	Max (80 ps, ± 1% x (1/f_{OUT_CCC}))	ps
LVDS25, HCSL, RSDS, B-LVDS, M-LVDS, Mini-LVDS	V_{ID} and V_{ICM} per the corresponding DC specification table.	-55 °C ≤ T_j ≤ 125 °C	Max (80 ps, ± 1% x (1/f_{OUT_CCC}))	ps
Differential 3.3V MSIO input: LVPECL, LVDS33	V_{ID} >= V_{ICM}	-55 °C ≤ T_j ≤ 125 °C	Max (80 ps, ± 1% x (1/f_{OUT_CCC}))	ps
	V_{ID} and V_{ICM} per the corresponding DC specification table.	-55 °C ≤ T_j ≤ 25 °C	Max (140 ps, ± 1% x (1/f_{OUT_CCC}))	ps
		25 °C ≤ T_j ≤ 125 °C	Max (80 ps, ± 1% x (1/f_{OUT_CCC}))	ps

In the case of an external clock entering the RTG4 fabric via a 3.3V LVPECL/LVDS33 MSIO input buffer without passing through a PLL, the maximum added period jitter (peak-to-peak) will be added to the RTG4 Datasheet, as shown in the following table.

Table 3 • RTG4 FPGAs Max Input Buffer Jitter Added to Input Clocks Directly Driving Globals

Input Clock I/O Standard	Input Voltage Condition	Operating Temperature	Max Clock Jitter (peak-to-peak period jitter)	Unit
Single-ended and Voltage Referenced	N/A	-55 °C ≤ T_j ≤ 125 °C	Max (100 ps, ± 1% x (1/f_{OUT_CCC}))	ps
LVDS25, HCSL, RSDS, B-LVDS, M-LVDS, Mini-LVDS	V_{ID} and V_{ICM} per the corresponding DC specification table.	-55 °C ≤ T_j ≤ 125 °C	Max (100 ps, ± 1% x (1/f_{OUT_CCC}))	ps
Differential 3.3V MSIO input: LVPECL, LVDS33	V_{ID} >= V_{ICM}	-55 °C ≤ T_j ≤ 125 °C	Max (150 ps, ± 2% x (1/f_{OUT_CCC}))	ps
	V_{ID} and V_{ICM} per the corresponding DC specification table.	-55 °C ≤ T_j ≤ 25 °C	Max (300 ps, ± 4% x (1/f_{OUT_CCC}))	ps
		25 °C ≤ T_j ≤ 125 °C	Max (100 ps, ± 1% x (1/f_{OUT_CCC}))	ps

Application Impact

If the operating junction temperature is below 25 °C and V_{ID} is lower than V_{ICM}, extra jitter is observed on fabric input clocks which could cause timing issues in the design if the jitter was not properly accounted for during static timing analysis (STA).

Action Required

Designers should review the updated datasheet jitter specifications shown above to evaluate whether their design can meet the required timing performance with the added clock jitter. This clock jitter should be factored into STA using SmartTime. The clock jitter can be specified using clock source latency constraints. For example, to specify a clock jitter of +/- 200 ps on a clock named "RTG4FCCC_0/GL0", use the constraints below and re-run static timing analysis.

```
set_clock_latency -source -early -0.2 { RTG4FCCC_0/GL0 }
set_clock_latency -source -late 0.2 { RTG4FCCC_0/GL0 }
```

For more information, see the RTG4 Timing Constraints User's Guide found at the link below:

https://www.microsemi.com/document-portal/doc_download/136454-rtg4-fpga-timing-constraints-enhanced-constraint-flow

Products Affected by this Change

See Appendix A.

CAN18009.4 RTG4 Fabric DDR (FDDR) Controller Documentation

Description of Change

The RTG4 FDDR Users Guide (UG0573) contains information indicating that dynamic write leveling and dynamic read training are available when the FDDR is used in DDR3 mode. This is incorrect. These features are not available in the RTG4 FDDR controller. UG0573 has been updated to explain how these DRAM training tasks are handled by the RTG4 FDDR controller. References to the support for dynamic write leveling and read training have been removed. Furthermore, the RTG4 board design and layout guidelines (AC439 revision 9) have been updated with DDR3 specific trace length-matching guidelines for all data byte lanes to ensure that the user board design meets DDR3 timing specifications at worst-case operating conditions.

Application Impact

Depending on the board layout, the DDR3 tDQSS limit on skew between DQS and CK during writes could be violated at worst-case operating conditions. Note that the RTG4 FDDR DDR3 max clock frequency is 333MHz, which is a relatively large clock period compared to the DDR3 operating spectrum. This means that a DDR3-compliant board layout can be achieved without dynamic write leveling for such low frequency DDR3 operation. Read-gate training and read data-eye leveling are handled by automatically generated static delay values used to initialize the FDDR controller (via CoreABC) combined with board layouts which meet any revision of the RTG4 board design and layout guidelines (AC439 and AC453).

Action Required

Designers planning to use the RTG4 FDDR with DDR3 memories must ensure that the RTG4 DDR3 board layout and trace length-matching guidelines, found in application note AC439, revision 9 have been followed. If the board layout meets the updated length-matching guidelines for the DDR3 data byte lanes, then no further action is required.

If the updated layout guidelines are not met, designers must calculate the skew between DQS and CK at each DDR3 device during a write (tDQSS) to determine if the DDR3 specification is met at worst-case conditions. As an example, designers can refer to the AC439 addendum showing a similar analysis of the RTG4 development kit. If the board meets tDQSS limits at each memory device, then no further action is required.

If the board does not meet tDQSS at each memory device, then manual tuning can be applied to the RTG4 FDDR controller configuration registers. Guidance can be found in the addendum to AC439 and in the DRAM training section of the RTG4 FDDR Users Guide UG0573. The FDDR controller supports static delay values for the write DQS output signal, which allows user control of the DQS to CK skew at each DDR3 memory device for circuit board layouts that do not comply to the guidelines in AC439 revision 9.

Products Affected by this Change

See Appendix A.

CAN18009.5 Synopsys Synplify Safe FSM Setting Change

Description of Change

Microsemi recommends that you avoid the use of the "safe" FSM attribute for RTG4 FPGAs.
RTG4 FPGAs have triple-redundant fabric flip-flops, which combined with optional built-in SET mitigation filters, provide ample mitigation of single event upsets. Using the “safe” FSM attribute will consume more fabric resources and will cause the generation of additional asynchronous reset networks, which can contribute to routing congestion, with negative impact on design performance and utilization.
Starting with Synplify Pro ME L2016.09MSP1-5, Synplify will generate an error message (error message DE108) by default if the “safe” FSM attribute is used for an RTG4 design. This error message may be downgraded to a warning if the user wishes to continue with the added “safe” FSM recovery logic.

Application Impact

Synplify Pro ME L2016.09MSP1-5 and later releases will generate error message DE108 if the “safe” FSM attribute is used.

Action Required

Designers who absolutely require safe FSM encoding may downgrade the error message to a warning to continue compiling the design with the safe FSM implementation included. To downgrade the error to a warning, identify the error in the report log, right click ‘DE108’ and select ‘Downgrade to Warning:DE108’. The report log is stored in synthesis /<design_name>.pfl. It is also possible to downgrade the warning if using a scripted design flow, using the following Tcl script:

```
message_override -warning DE108
```

Products Affected by this Change

See Appendix A.

PCN18009.6 RTG4 Timing Changes

Description of Change

Silicon characterization has highlighted a need for an adjustment to the timing models for certain signal paths connecting programmable gates to the EPCS, SERDES, and FDDR blocks. Additionally, signals derived from programming gates connecting to row global buffers (RGB) via local routing tracks are subject to a timing adjustment. Finally, the row global reset macro (RG RESET) that connects a D-type flip-flop output to an asynchronous reset network is also subject to a timing change.

Application Impact

Timing faults may occur in a very specific set of circumstances (corner cases) in which local routing tracks are used to feed clock signals to RGBs, or where a flip-flop in the logic fabric feeds directly to a data input in the SERDES. These timing faults are observable as functional failures only in specific combinations of temperature and voltage. If functional testing of flight model hardware successfully exercises the hardware at or beyond the extremes of temperature and voltage that the system will be exposed to during operation, then the timing issues should not occur in operation. Production testing at the extremes of the operating range is a best practice recommended by Microsemi.

Action Required

Microsemi will introduce updated timing models with the Libero v11.9 release, scheduled for August 2018. Customers are advised to re-run timing using this release to evaluate whether timing faults exist in their designs. Contact Microsemi if timing violations identified by re-running timing using Libero v11.9 cannot be resolved by re-running the tool flow.

Products Affected by this Change

See Appendix A.

PCN18009.7 RTG4 PLL in Internal Feedback Mode (TMR Mode)

Description of Change

A triple module redundant (TMR) PLL is used when the PLL Internal feedback mode is selected, while a single, non-TMR PLL is used when CCC Internal or External feedback modes are selected in the Libero CCC configurator software. RTG4 TMR PLL includes three sub-PLLs with a voted lock to help mitigate single event effects in radiation environments. Preliminary single event effect radiation testing has demonstrated that the RTG4 PLL can experience loss of lock in several ways, and can also experience loss of output. The results are summarized in the following table and are described in a separate radiation test report available from Microsemi.

When the PLL is configured for single, non-TMR operation, it can experience a disturbance during which lock is temporarily lost and the output clock changes phase with respect to the input clock. This mode self recovers after a brief time. A second effect, in which lock is lost and the output clock stops, is also observed. This mode occurs much less often than the first, and requires an asynchronous reset to the PLL to recover.

When the PLL is configured for triple redundant configuration via the selection of PLL Internal feedback mode, it can experience a loss of lock that will not self-recover and requires assertion of the PLL_ARSTN_N reset input to regain lock. During this time, the clock output from the triple redundant PLL will continue to run, however, the quality of the clock (frequency stability, jitter) has not been determined.

Table 4 • RT4 PLL Radiation Single Event Effects

	Loss of Lock, Self-Recoverable Upset Rate, GEO Solar Min	Loss of Lock, Reset-Recoverable Upset Rate, GEO Solar Min	Loss of Output, Reset-Recoverable Upset Rate, GEO Solar Min
CCC Internal or External Feedback modes (Single PLL), External Clock (20 MHz)	8.28E-05 upsets/PLL/day	Not applicable, loss of lock always recovers for single PLL	5.71E-07 upsets/PLL/day
PLL Internal Feedback (TMR PLL), External Clock (20 MHz)	Not applicable, loss of lock requires reset	1.88E-05 upsets/PLL/day	Not observed

Application Impact

Loss of lock of the PLL when running in PLL Internal Feedback (TMR) mode requires a reset signal to be applied to the PLL. During the time that lock is lost, the quality of the clock output from the PLL is not guaranteed.

Action Required

Designers have two options if they are using the PLL features in RTG4:

- Use the single PLL in CCC Internal or External feedback Mode. This will actually increase the probability of loss of lock, however, in single PLL mode most instances of loss of lock will self-recover. The rate of occurrence of single event effects requiring the PLL to be reset is significantly lower for the single PLL versus the triple redundant PLL.
- Use the triple-redundant PLL via PLL Internal feedback mode with a Microsemi-generated reset circuit. Microsemi will introduce a circuit that will monitor the PLL lock signal when the PLL is in PLL Internal feedback mode. This circuit will automatically issue a reset command to the PLL if loss of lock is detected. The circuit will be introduced in Microsemi Libero SoC v11.9 development software, which is expected to be released in August 2018. Selection of a clock source for the monitor circuit will be described in a future edition of the RTG4 Clocking Users Guide.

Products Affected by this Change

See Appendix A.

CN18009.8 RTG4 CCC Simulation False Failures

Description of Change

The RTG4 simulation library model will be updated in Libero SoC v11.9 software to enhance the PLL modelling equation in cases where specific CCC configurations, coupled with cascaded PLLs, and simulator rounding effects can lead to clock distortion during simulation of the FDDR memory controller. Digital simulators will round to the nearest picosecond, and for example, this means that clock frequencies of 300 MHz will have their periods truncated to 3.333 ns. Cascaded PLLs can cause the rounding effect on the clock period to accumulate. One example of this situation occurs when a fabric CCC provides a base clock for the FDDR which in-turn generates the DDR clock for the memory interface. The simulation model tries to compensate for this effect using an equation to model the clock period and will periodically add extra time to stabilize the clock period and edge alignment of the output clock. Prior to Libero SoC v11.9, the simulation model equation didn't correctly account for the contribution of one of the PLL output dividers which allowed the FDDR PLL clock to have a distorted clock period and duty cycle.

Application Impact

This issue manifests as a simulation issue only. The distorted clock period and duty cycle on the FDDR PLL clock can cause the FDDR PLL to lose lock and result in false simulation failures when simulating the DDR memory interface using a memory device simulation model. The RTG4 FPGA silicon does not show this behavior.

Action Required

Re-run simulations using the updated simulation library in Libero SoC v11.9.

Products Affected by this Change

See Appendix A.

PCN18009.9 Incorrect CoreFIFO Empty Flag Timing in Specific RTG4 Configuration

Description of Change

CoreFIFO will be modified to account for the actual LSRAM timing when using pipelined ECC mode in a single-clock configuration by waiting one extra clock cycle during writes before de-asserting the Empty Flag. In single-clock (synchronous) mode, when the LSRAMs are enabled to use pipelined-ECC mode, CoreFIFO does not account for the extra clock cycle required for the LSRAM ECC encoder to process the write data, prior to the actual memory array being written with the encoded data. This allows the Empty Flag to de-assert too early, which could cause user logic to issue a FIFO read too soon.

Application Impact

When using CoreFIFO on RTG4, the configuration described above utilizes incorrect Empty Flag timing which could result in read data errors due to reads being issued before the expected data is actually written into the LSRAM. The resulting write and read sequence can reach a point where the read is occurring on an address in LSRAM where the expected data has not yet been completely written, resulting in read data errors/ECC flag assertion on the LSRAM blocks.

Action Required

Update RTG4 designs using CoreFIFO to replace the instance version with the updated release of CoreFIFO, targeted for the end of July 2018.

Products Affected by this Change

See Appendix A.

Contact Information

If you have further questions about this subject, contact Microsemi's Technical Support at soc_tech@microsemi.com .

Regards,
Microsemi Corporation

Any projected dates in this PCN are based on the most current product information at the time this PCN is being issued, but they may change due to unforeseen circumstances. For the latest schedule and any other information, please contact your local Microsemi Sales Office, the factory contact shown above, or your local distributor.

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Appendix A

Microsemi Part Number	DLA SMD Number
RT4G150-CB1657PROTO	
RT4G150-CG1657B	5962-1620801QXF
RT4G150-CG1657E	5962-1620805QXF
RT4G150-CG1657EV	
RT4G150-CG1657PROTO	
RT4G150-CQ352B	
RT4G150-CQ352E	
RT4G150-CQ352EV	
RT4G150-CQ352PROTO	
RT4G150-LG1657B	5962-1620803QZC
RT4G150-LG1657E	5962-1620807QZC
RT4G150-LG1657EV	
RT4G150-LG1657PROTO	
RT4G150-1CB1657PROTO	
RT4G150-1CG1657B	5962-1620802QXF
RT4G150-1CG1657E	5962-1620806QXF
RT4G150-1CG1657EV	
RT4G150-1CG1657PROTO	
RT4G150-1CQ352B	
RT4G150-1CQ352E	
RT4G150-1CQ352EV	
RT4G150-1CQ352PROTO	
RT4G150-1LG1657B	5962-1620804QZC
RT4G150-1LG1657E	5962-1620808QZC
RT4G150-1LG1657EV	
RT4G150-1LG1657PROTO	

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