Total Ionizing Dose Test Report

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Nadia Rezzak, J.J. Wang, Alex Cai, Stephen Varela, Harvey Chen, Kevin Chou, Michael Traas

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I. SUMMARY TABLE

Parameter	Tolerance
1. Gross Functionality	Passed 125 krad(SiO_2)
2. Power Supply Current	Passed 125 krad(SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 125 krad(SiO_2)
4. Output Drive (VOL/VOH)	Passed 125 krad(SiO_2)
5. Propagation Delay	Passed 125 krad(SiO_2) for 10% degradation criterion
6. Transition Time	Passed 125 krad(SiO_2)

II. TOTAL IONIZING DOSE (TID) TESTING

This testing is designed on the basis of an extensive database of TID testing for Radiation-Tolerant FPGAs including flash-based FPGAs. Microsemi TID reports can be found at http://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/military-aerospace-radiation-reliability-data#tid-reports

Electrical parameters are measured pre-irradiation and post-irradiation using the burn in design and the ATE test program. The report summarizes sample pins. Two factors make sampling appropriate: first, the tolerance is determined by current and propagation delays which are global parameters; second the total dose effect is uniformly distributed across the chip.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation each input and most of the output is grounded.

Table. 1. DUT and Irradiation Parameters

Part Number	RT4G150
Package	LG1657
Foundry	United Microelectronics Corp.
Technology	65 nm
DUT Design	Burn in design with inverter string
Die Lot Number	KRKTL
Quantity Tested	3
Serial Number	6864, 6874, 6877
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate	5 krad (SiO_2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias	Static at 1.2V/2.5V/3.3V/3.3V
IO Configuration	Single ended Differential Pair

B. Test Method

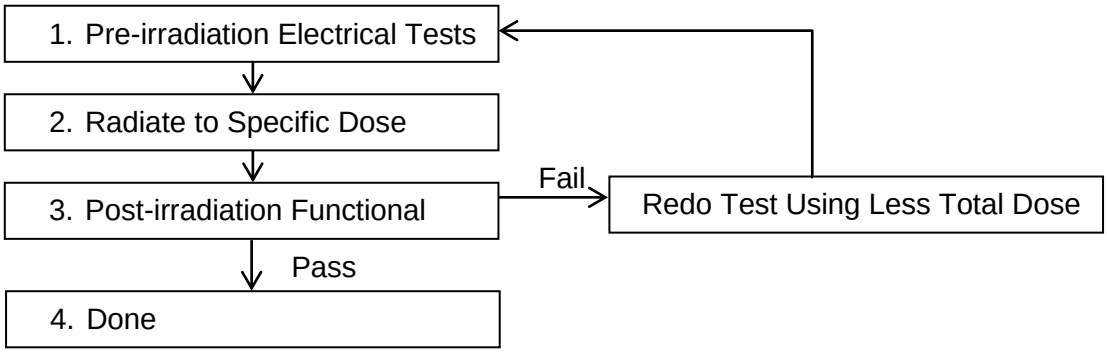

Fig. 1. Parametric test flow chart

The test method generally follows the guidelines in the military standard TM1019. Figure 1 shows the flow chart describing the steps for the functional and parametric tests.

C. Design and Parametric Measurements

RTG4 FPGA devices have different types of I/Os, such as MSIO and MSIOD, double data rate I/Os (DDRIO), and dedicated I/Os based on functional usage. For more information on I/O naming conventions and I/O description, refer to the RTG4 FPGA Pin Description. All I/Os are tested pre and post-irradiation.

Fabric functionality coverage performed by the burn in design is summarized in table 2 below. In addition to the fabric coverage the supplemental test of propagation delay is also used to determine DUT functionality. These tests are performed pre and post-irradiation and recorded as a pass/fail.

Refer to appendix A for a graphical representation of fabric functional coverage blocks used to perform the functional tests.

Table. 2. Fabric Functional Coverage

Block	**Coverage**
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	Maximum output toggle rate(checker board) compared to reference
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 uRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
I/O Block	I/O utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

The core power supply current IDD, the I/Os power supply currents (IDDI_2.5/IDDI_3.3) and the charge pump/PLL power supply current (IPP_PLL) are also monitored during irradiation in real time.

The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential inputs, and is reported as a pass or fail, as part of the ATE test program. The output-drive voltage (VOL/VOH) is also measured on all pins on the MSIO MSIOD and DDRIO. This report contains the output-drive voltage measurements on selected IO pins used in the burn in design are reported at the LVTTL and LVCMOS 2.5V standard at different sourcing and sinking currents.

A 2000 stage inverter string is used to measure the propagation delay. The propagation delay is defined as the time delay from the triggering edge at the Clock input to the switching edge at the output. The propagation delay is monitored real time during irradiation and the time difference between positive switching edges of the clock and output are reported. Additionally, the transition characteristics (rise and fall) at the output of the inverter chain are measured pre and post-irradiation. Oscilloscope screen captures are shown in section III. F.

III. TEST RESULTS

A. Functionality

Every DUT passed the pre-irradiation and post-irradiation functional tests mentioned in section II.C.

B. Power Supply Current

The core power supply current (IDD) is 1.2 V, the I/O bank power supply currents (IDDI) are 2.5 V (IDDI_2.5) and 3.3 V (IDDI_3.3). The charge pump and PLL power supply current (IPP_PLL) is 3.3 V. Figures 2-13 illustrate the plot of in-flux standby IDD, IDDI_2.5, IDDI_3.3 and IPP_PLL versus total dose for every DUT. Tables 3-6 summarize the pre-irradiation and post-irradiation total current (static & dynamic) IDD, IDDI_2.5 , IDDI_3.3 and IPP_PLL. In each case the current measured pre and post irradiation is minimal.

Table. 3. Pre-irradiation and Post-irradiation I_{DD}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
6864	125 krad	0.471	0.496	5.40
6874	125 krad	0.470	0.499	6.24
6877	125 krad	0.457	0.485	6.23

Table. 4. Pre-irradiation and Post-irradiation $I_{DDI\_2.5}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
6864	125 krad	0.0130	0.0157	20.38
6874	125 krad	0.0112	0.0138	22.39
6877	125 krad	0.0115	0.0141	22.96

Table. 5. Pre-irradiation and Post-irradiation $I_{DDI\_3.3}$

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
6864	125 krad	0.0331	0.0458	22.32
6874	125 krad	0.0402	0.0451	10.40
6877	125 krad	0.0409	0.0415	9.47

Table. 6. Pre-irradiation and Post-irradiation I_{PP_PLL}

DUT	Total Dose	Pre-irradiation (A)	Post-irradiation (A)	Increase (%)
6864	125 krad	0.0161	0.0173	2.25
6874	125 krad	0.0158	0.0179	1.00
6877	125 krad	0.0159	0.0164	1.19

The following figures (2-13) show the in-beam monitoring of the currents mentioned above as a function of TID for the available DUTs.

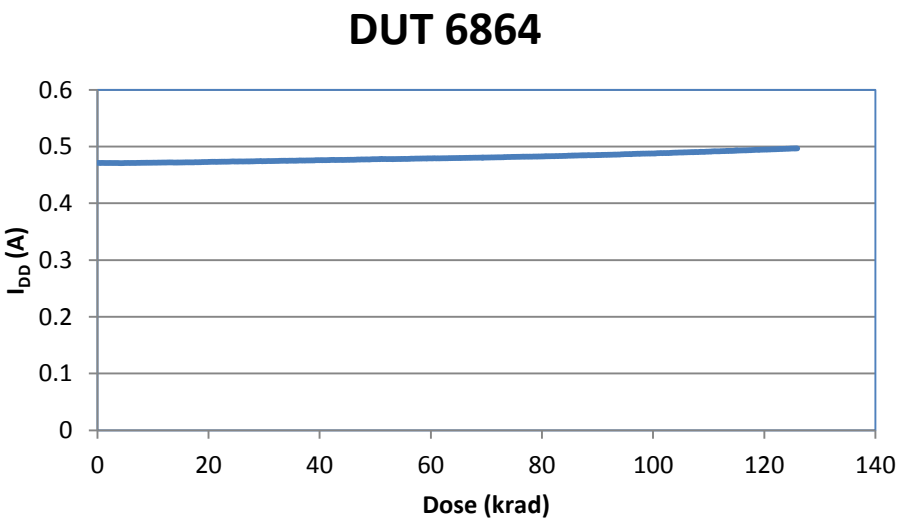

Fig. 2. DUT 6864 core power supply current (I_{DD}) versus TID

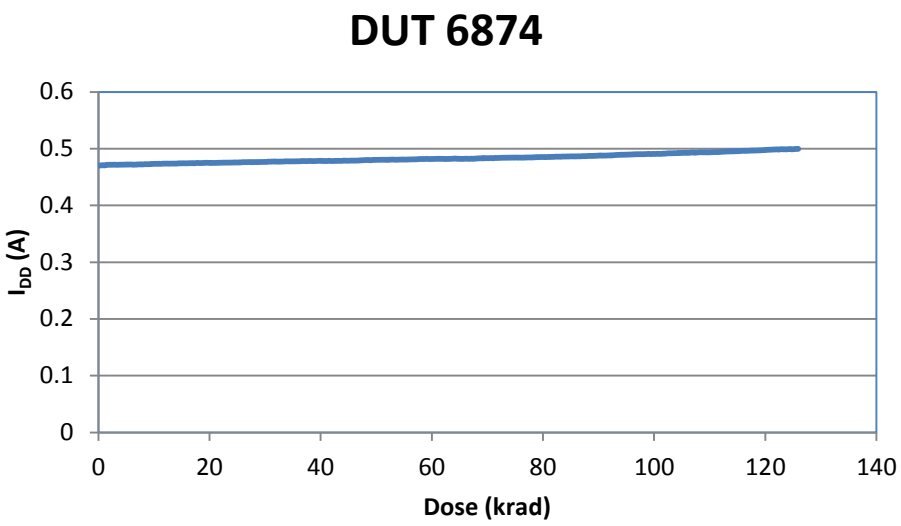

Fig. 3. DUT 6874 core power supply current (I_{DD}) versus TID

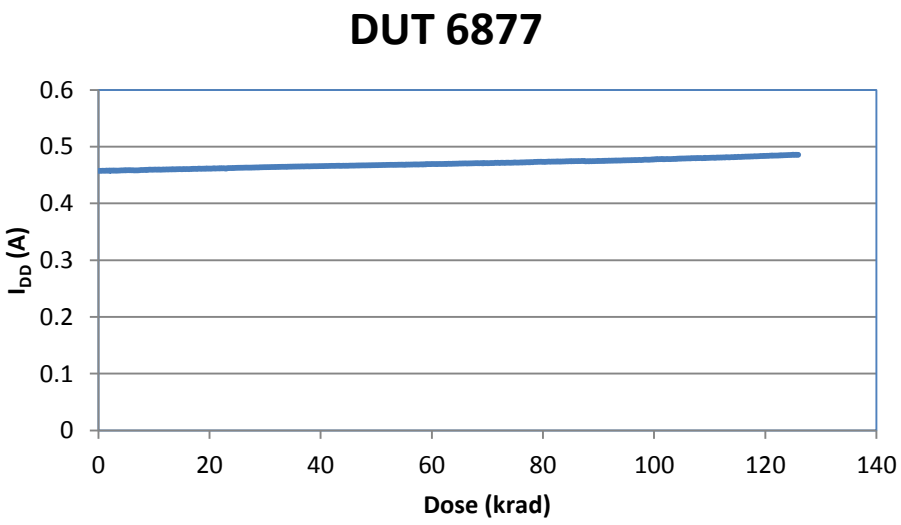

Fig. 4. DUT 6877 core power supply current (I_{DD}) versus TID

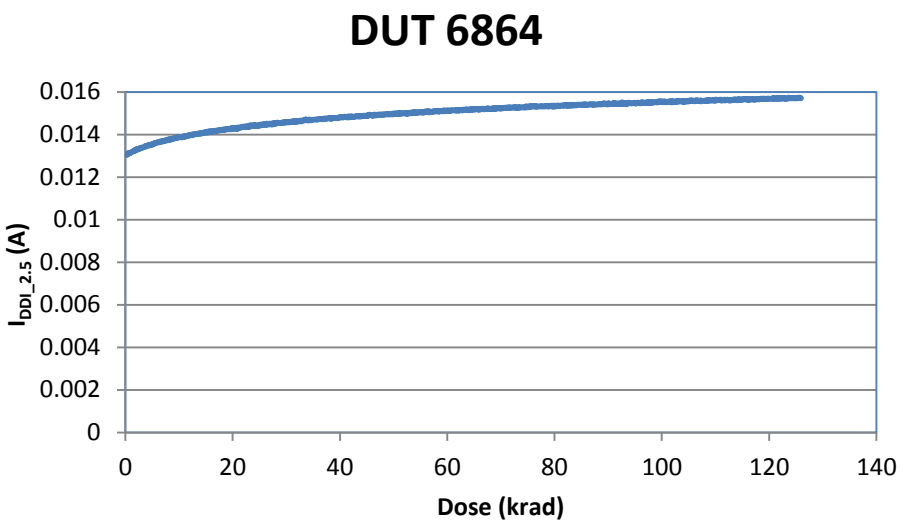

Fig. 5. DUT 6864 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

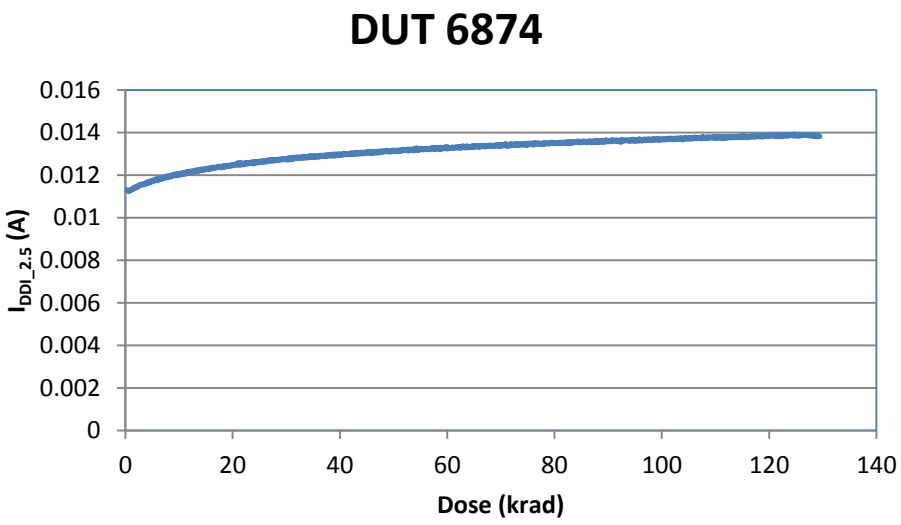

Fig. 6. DUT 6874 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

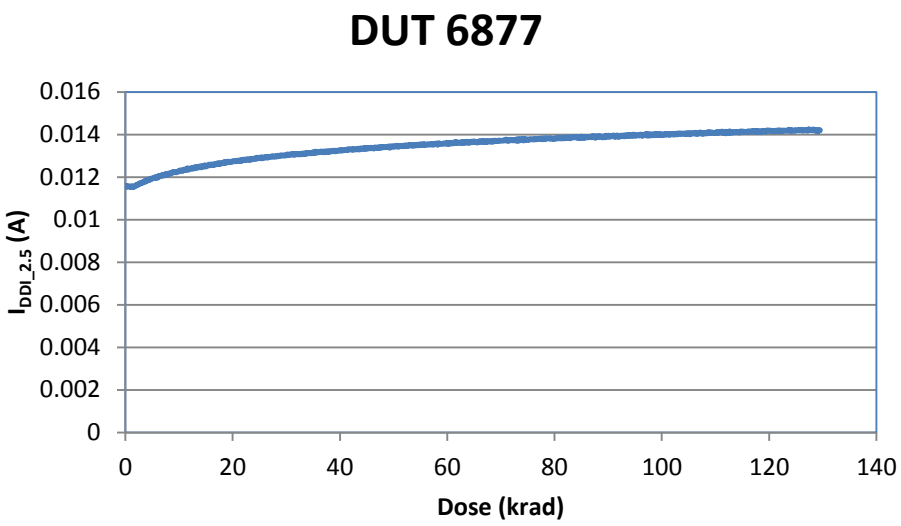

Fig. 7. DUT 6877 I/O bank 2.5V power supply current ($I_{DDI\_2.5}$) versus TID

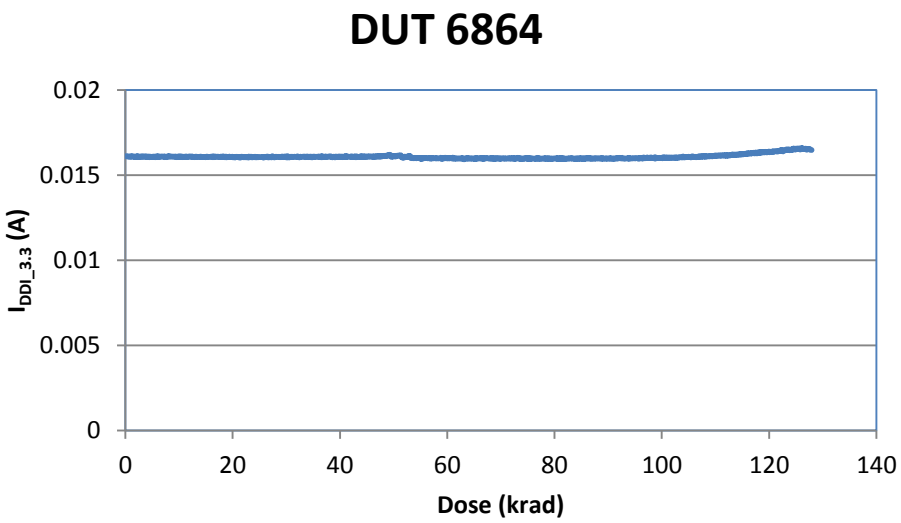

Fig. 8. DUT 6864 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

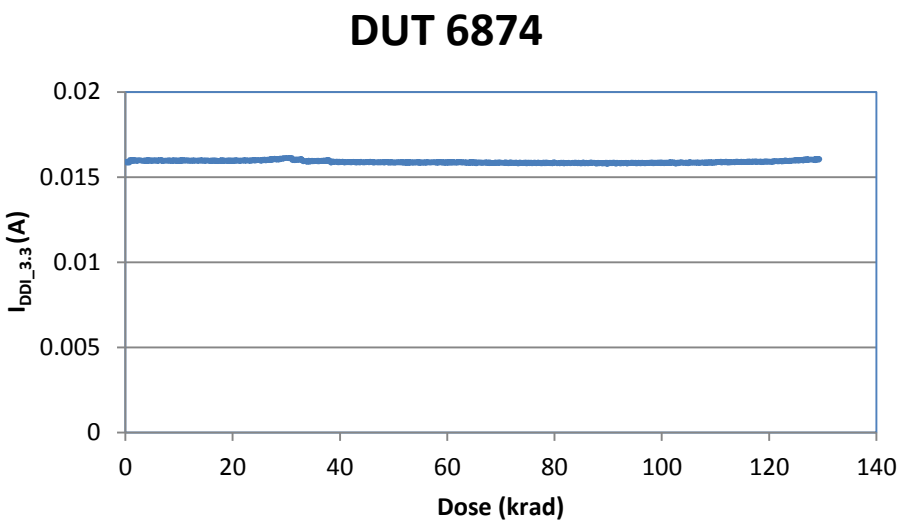

Fig. 9. DUT 6874 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

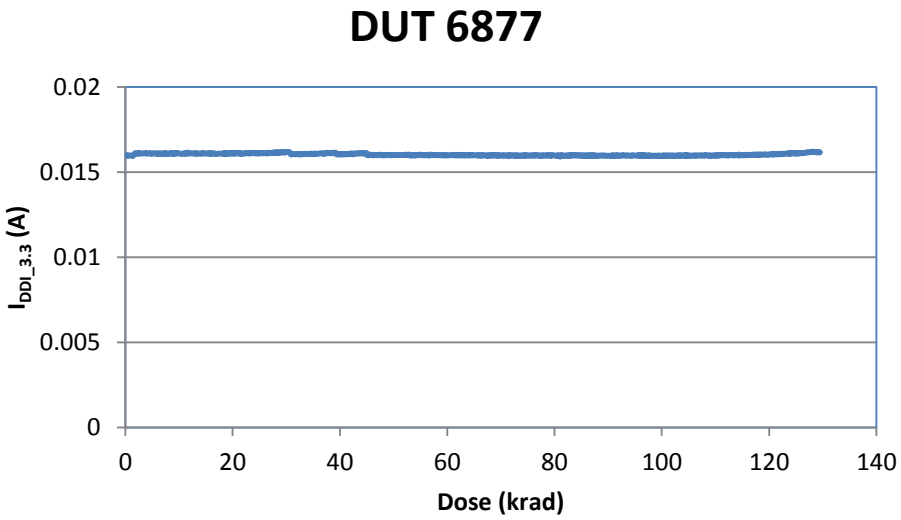

Fig. 10. DUT 6877 I/O bank 3.3V power supply current ($I_{DDI\_3.3}$) versus TID

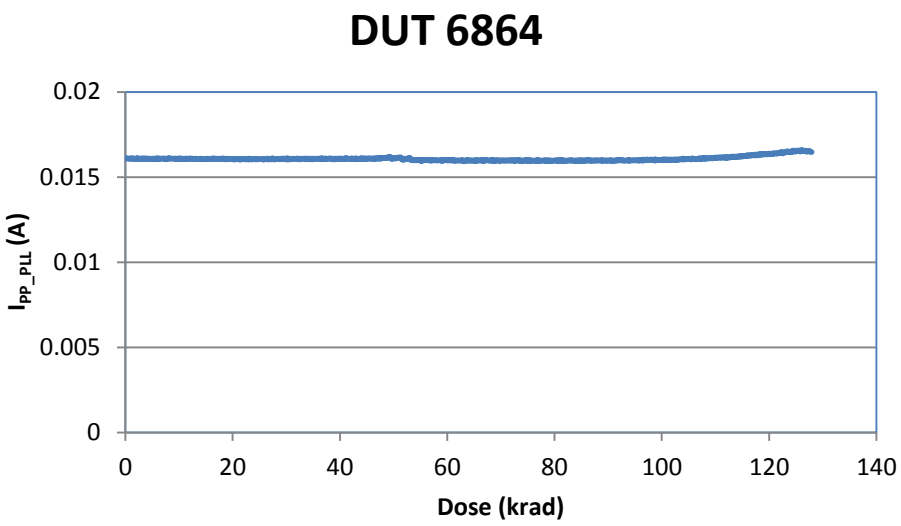

Fig. 11. DUT 6864 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

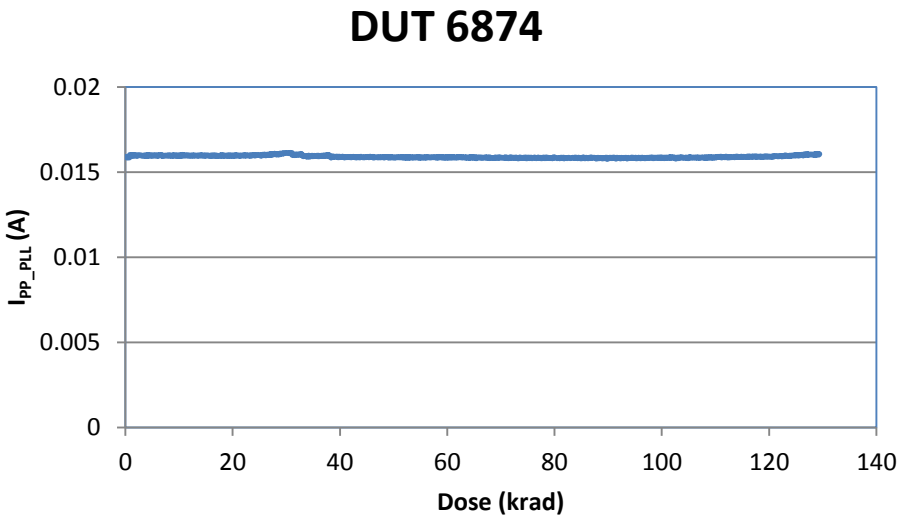

Fig. 12. DUT 6874 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

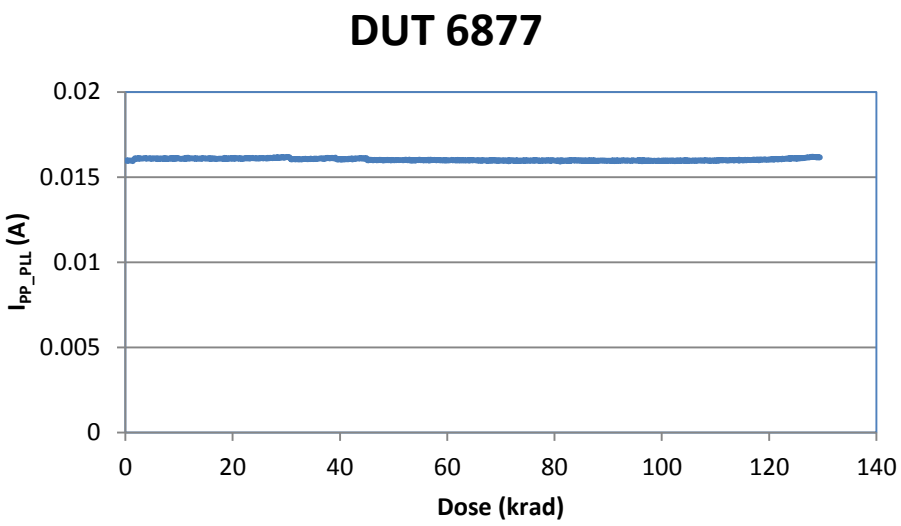

Fig. 13. DUT 6877 charge pump and PLL power supply current (I_{PP_PLL}) versus TID

C. Single-Ended Input Logic Threshold (VIL/VIH)

The input switching threshold, or trip point, is defined as the applied input voltage at which the output of the design starts to switch. VIH is the input trip point when the input is going high to low and VIL is the input trip point when the input is going low to high. The input logic threshold (VIL/VIH) is measured on all single-ended inputs as well as all differential input and recorded as pass or fail. All I/Os are tested at their respective I/O standards and are compliant to the JEDEC specs. Refer to http://www.microsemi.com/document-portal/doc_view/135193-ds0131-rtg4-fpga-datasheet for more information.

The 3 DUTs tested passed with respect to the testing specification pre and post-irradiation. This pass/fail is determined as part of the ATE test program used to perform pre and post-irradiation electrical parametric measurements.

Table. 7. VIH Summary

DUT	Pre-irradiation	Post-irradiation
6864	Passed	Passed
6874	Passed	Passed
6877	Passed	Passed

Table. 8. VIL Summary

DUT	Pre-irradiation	Post-irradiation
6864	Passed	Passed
6874	Passed	Passed
6877	Passed	Passed

D. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-irradiation output-drive voltages (VOL/VOH) are performed on all available IOs. The measurements performed pre and post irradiation are within the specification limits; in each case, the radiation-induced degradation is within 10%. For the purpose of this report, the measurements presented below in tables 9 through 20 are sampled on several pins used in the burn in design.

Table. 9. LVCMOS 25 VOH – DUT 6864

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.1324	2.1271	2.2014	2.1934	2.1719	2.1603	2.1526	2.1375	2.119	2.0966	2.1048	2.0791
EPCSRST_N_0	B31	2.1334	2.1271	2.2019	2.1923	2.1725	2.1586	2.1532	2.1352	2.1193	2.0929	2.1052	2.0746
EPCSRST_N_1	B32	2.1344	2.1302	2.2036	2.1981	2.1753	2.1675	2.1554	2.1453	2.1241	2.1094	2.1108	2.0938
EPCSRST_N_2	B34	2.1326	2.1304	2.2017	2.1996	2.1729	2.1701	2.1525	2.1491	2.1204	2.1156	2.1067	2.1015
EPCSRST_N_3	B35	2.1337	2.1323	2.2037	2.2021	2.1755	2.174	2.1559	2.1541	2.1252	2.1235	2.1124	2.1104
EPCSRST_N_4	B36	2.131	2.1281	2.1989	2.1953	2.1688	2.1642	2.1471	2.1405	2.1118	2.1029	2.0967	2.0865
EPCSRST_N_5	B37	2.1331	2.1311	2.2033	2.2016	2.1751	2.1732	2.1552	2.153	2.1243	2.1214	2.1115	2.1083
MONITOR	K23	2.1337	2.1297	2.2026	2.1979	2.1744	2.1678	2.1547	2.1462	2.1237	2.1117	2.1107	2.097
PLL_MON	L20	2.13	2.1316	2.1978	2.203	2.1668	2.1756	2.1455	2.1574	2.1091	2.1284	2.0929	2.1164
TOGGLE_MON	L22	2.1326	2.1306	2.2032	2.2019	2.1758	2.1741	2.156	2.1538	2.1265	2.1239	2.1143	2.1116

Table. 10. LVCMOS 25 VOH – DUT 6874

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.1337	2.129	2.2019	2.1943	2.1726	2.1614	2.1533	2.1382	2.1191	2.0976	2.1049	2.0796
EPCSRST_N_0	B31	2.1348	2.1294	2.2027	2.1936	2.1732	2.1603	2.1537	2.1364	2.1198	2.0945	2.1057	2.0762
EPCSRST_N_1	B32	2.1354	2.1323	2.2042	2.1994	2.176	2.1689	2.1561	2.1466	2.1247	2.1111	2.1113	2.0956
EPCSRST_N_2	B34	2.1343	2.1326	2.2029	2.201	2.1742	2.1712	2.1536	2.1502	2.1212	2.1165	2.1075	2.1019
EPCSRST_N_3	B35	2.1355	2.1346	2.2047	2.2039	2.1768	2.1759	2.1572	2.1557	2.1262	2.1252	2.1134	2.1121
EPCSRST_N_4	B36	2.1337	2.1312	2.2007	2.1973	2.1714	2.1659	2.1497	2.1426	2.1155	2.1049	2.101	2.089
EPCSRST_N_5	B37	2.1354	2.1343	2.2041	2.2035	2.1761	2.175	2.1563	2.1551	2.1254	2.1237	2.1123	2.1105
MONITOR	K23	2.1347	2.1316	2.2036	2.1993	2.176	2.1694	2.1568	2.148	2.1263	2.1136	2.1136	2.0988
PLL_MON	L20	2.135	2.1336	2.2053	2.2047	2.1785	2.1775	2.1603	2.1594	2.1316	2.1308	2.1204	2.1191
TOGGLE_MON	L22	2.1338	2.1329	2.2042	2.2033	2.1768	2.1761	2.1575	2.1562	2.128	2.1267	2.1161	2.1148

Table. 11. LVCMOS 25 VOH – DUT 6877

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.133	2.1278	2.2013	2.1936	2.1721	2.1608	2.1526	2.1376	2.1188	2.0971	2.1042	2.0794
EPCSRST_N_0	B31	2.1337	2.1279	2.2021	2.1926	2.1728	2.1595	2.1534	2.1358	2.1195	2.0937	2.1054	2.0755
EPCSRST_N_1	B32	2.1346	2.131	2.2036	2.1983	2.1755	2.1679	2.1555	2.1456	2.124	2.1096	2.1107	2.0943
EPCSRST_N_2	B34	2.1324	2.1306	2.2019	2.2001	2.1731	2.1707	2.1527	2.1492	2.1202	2.1159	2.1068	2.1018
EPCSRST_N_3	B35	2.1337	2.1323	2.2038	2.2027	2.1756	2.1745	2.1561	2.1545	2.1253	2.1235	2.1122	2.1105
EPCSRST_N_4	B36	2.1317	2.1287	2.1995	2.1959	2.1694	2.1643	2.1478	2.141	2.113	2.1031	2.0981	2.0866
EPCSRST_N_5	B37	2.1335	2.1323	2.2033	2.2021	2.1752	2.1737	2.1553	2.1533	2.1243	2.122	2.1114	2.1086
MONITOR	K23	2.1343	2.1306	2.2033	2.1983	2.1756	2.1685	2.1564	2.1473	2.1259	2.1127	2.113	2.098
PLL_MON	L20	2.1314	2.1323	2.2	2.2037	2.1707	2.1764	2.1503	2.1583	2.1165	2.1296	2.1029	2.1173
TOGGLE_MON	L22	2.1332	2.1314	2.2038	2.2025	2.1762	2.1748	2.1567	2.155	2.1273	2.1253	2.1155	2.1132

Table. 12. LVCMOS 25 VOL – DUT 6864

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	236.885	241.599	169.288	176.894	197.901	209.152	221.108	235.829	253.039	274.688	266.9435	291.9608
EPCSRST_N_0	B31	236.923	242.228	169.464	178.641	197.951	211.466	221.271	239.06	253.128	279.301	267.0692	297.5174
EPCSRST_N_1	B32	235.307	238.76	167.277	172.574	194.72	202.466	215.522	225.277	246.004	260.29	259.1351	275.6815
EPCSRST_N_2	B34	237.253	239.388	169.185	171.407	197.294	200.231	218.397	221.661	249.632	253.975	263.1524	268.1113
EPCSRST_N_3	B35	236.575	238.044	167.616	168.745	195.046	196.39	215.522	216.765	245.175	246.757	257.842	259.5871
EPCSRST_N_4	B36	239.513	242.501	172.374	175.926	201.976	206.86	224.611	230.637	258.846	267.345	273.8737	283.6282
EPCSRST_N_5	B37	237.153	239.074	167.879	169.31	195.36	197.08	215.924	217.857	246.016	248.389	258.884	261.5455
MONITOR	K23	235.535	238.55	167.291	171.513	194.684	200.778	215.593	223.245	245.65	256.607	258.2908	271.1329
PLL_MON	L20	238.021	235.532	172.188	166.041	201.755	192.854	220.975	212.905	248.669	240.774	276.3996	252.8294
TOGGLE_MON	L22	235.159	236.602	165.783	167.037	192.66	194.141	212.084	213.577	241.019	243.064	253.5041	255.587

Table. 13. LVCMOS 25 VOL – DUT 6874

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	234.471	238.092	167.956	174.983	196.543	207.091	219.838	233.767	251.946	272.902	265.963	290.3265
EPCSRST_N_0	B31	234.471	238.645	168.182	176.492	196.769	209.215	220.077	236.659	252.071	276.913	266.1012	295.0408
EPCSRST_N_1	B32	233.173	235.609	165.984	170.528	193.603	200.093	214.292	222.766	244.786	257.742	257.7793	273.1078
EPCSRST_N_2	B34	234.441	235.609	167.553	169.298	195.599	197.821	216.677	219.326	247.975	252.117	261.5957	266.3412
EPCSRST_N_3	B35	233.412	233.839	165.77	166.172	193.063	193.515	213.4	213.965	243.33	243.945	256.1347	256.7373
EPCSRST_N_4	B36	235.496	237.529	169.499	173.039	198.449	203.533	220.456	227.059	253.85	263.705	268.4126	279.8494
EPCSRST_N_5	B37	233.776	234.253	166.034	166.624	193.477	194.18	214.016	214.493	243.932	244.899	256.8503	258.0806
MONITOR	K23	232.896	234.969	164.991	169	192.133	197.963	212.653	220.003	241.968	253.177	254.5588	267.514
PLL_MON	L20	232.251	232.238	163.602	163.841	189.837	189.863	209.724	209.825	237.33	237.179	248.8445	248.8319
TOGGLE_MON	L22	232.386	232.888	164.001	164.327	190.564	191.016	209.737	209.888	238.459	238.773	250.593	251.007

Table. 14. LVCMOS 25 VOL – DUT 6877

		2mA		4mA		6mA		8mA		12mA		16mA	
Pin Name	Pin #	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	235.791	239.965	168.76	176.102	197.524	208.197	220.731	234.874	252.524	273.745	266.6544	291.1311
EPCSRST_N_0	B31	235.703	240.493	168.785	177.485	197.398	210.158	220.618	237.639	252.524	277.906	266.4407	295.9711
EPCSRST_N_1	B32	234.366	237.404	166.762	171.934	194.23	201.662	214.97	224.423	245.69	259.487	258.7459	274.8905
EPCSRST_N_2	B34	236.889	238.459	168.62	170.478	196.791	199.101	217.87	220.732	249.23	253.272	262.6879	267.3204
EPCSRST_N_3	B35	235.634	236.701	167.088	167.854	194.381	195.31	214.832	215.886	244.748	245.978	257.4026	258.8966
EPCSRST_N_4	B36	238.032	240.593	171.306	174.947	200.671	205.768	223.042	229.533	256.813	266.266	271.6767	282.5988
EPCSRST_N_5	B37	235.91	237.103	167.352	168.293	194.758	196.113	215.384	217.004	245.552	247.485	258.3568	260.5663
MONITOR	K23	233.914	236.64	165.883	170.281	192.912	199.308	213.482	221.637	242.898	254.798	255.3756	269.1224
PLL_MON	L20	235.117	233.823	169.209	164.797	197.254	191.308	220.296	211.434	247.06	238.851	266.3681	250.5541
TOGGLE_MON	L22	233.365	234.369	164.829	165.695	191.556	192.635	210.716	211.883	239.513	240.793	251.6219	252.9771

Table. 15. LVTTL VOH – DUT 6864

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.9198	2.9146	2.9099	2.9015	2.8904	2.8751	2.8708	2.8485	2.8524	2.8234
EPCSRST_N_0	B31	2.9202	2.9147	2.9103	2.9006	2.8907	2.8725	2.8711	2.8446	2.8527	2.818
EPCSRST_N_1	B32	2.9213	2.9178	2.9122	2.9066	2.8944	2.8846	2.8767	2.8625	2.8593	2.8404
EPCSRST_N_2	B34	2.9197	2.9179	2.9102	2.9078	2.8915	2.8882	2.8729	2.8685	2.8546	2.8492
EPCSRST_N_3	B35	2.9207	2.9194	2.912	2.9107	2.8948	2.8935	2.8779	2.8761	2.8612	2.8594
EPCSRST_N_4	B36	2.9179	2.9154	2.9073	2.9036	2.886	2.8796	2.8643	2.8559	2.8431	2.832
EPCSRST_N_5	B37	2.92	2.9186	2.9114	2.9098	2.8942	2.8919	2.8772	2.8744	2.8601	2.8568
MONITOR	K23	2.9208	2.9175	2.9116	2.9067	2.8938	2.8856	2.8763	2.8649	2.8595	2.8446
PLL_MON	L20	2.9176	2.9198	2.9073	2.9118	2.8844	2.8965	2.8624	2.8815	2.8411	2.8669
TOGGLE_MON	L22	2.92	2.9185	2.912	2.9105	2.8961	2.8942	2.88	2.8778	2.8641	2.8614

Table. 16. LVTTL VOH – DUT 6874

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.9209	2.9165	2.9112	2.9031	2.8913	2.8762	2.8712	2.8493	2.8525	2.8235
EPCSRST_N_0	B31	2.9219	2.9168	2.9117	2.9026	2.8916	2.8747	2.8718	2.8466	2.8533	2.8197
EPCSRST_N_1	B32	2.9225	2.9197	2.9133	2.9083	2.8955	2.8865	2.8777	2.8643	2.8602	2.8421
EPCSRST_N_2	B34	2.9215	2.9202	2.9116	2.9097	2.893	2.8898	2.8742	2.8695	2.8558	2.8498
EPCSRST_N_3	B35	2.9225	2.9219	2.9135	2.9129	2.8964	2.8959	2.8794	2.8784	2.8624	2.8615
EPCSRST_N_4	B36	2.9207	2.9184	2.9099	2.9062	2.8893	2.8823	2.8685	2.8584	2.8481	2.8346
EPCSRST_N_5	B37	2.9222	2.9216	2.9132	2.9125	2.8956	2.8947	2.8784	2.8769	2.8611	2.8594
MONITOR	K23	2.9223	2.9193	2.9133	2.9088	2.8962	2.8879	2.8795	2.8671	2.8632	2.8469
PLL_MON	L20	2.9225	2.9218	2.9152	2.9143	2.9	2.8994	2.8849	2.8844	2.8705	2.8699
TOGGLE_MON	L22	2.9213	2.9206	2.9135	2.9123	2.8977	2.8967	2.882	2.8809	2.8664	2.865

Table. 17. LVTTL VOH – DUT 6877

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	2.9203	2.9157	2.9102	2.9023	2.8904	2.8756	2.8707	2.8488	2.8521	2.8235
EPCSRST_N_0	B31	2.9206	2.9157	2.9108	2.9017	2.8911	2.8738	2.8714	2.8458	2.8529	2.819
EPCSRST_N_1	B32	2.9217	2.9185	2.9123	2.907	2.8947	2.8851	2.8769	2.8627	2.8593	2.8407
EPCSRST_N_2	B34	2.9194	2.9181	2.9101	2.9081	2.8917	2.8887	2.873	2.869	2.8548	2.8494
EPCSRST_N_3	B35	2.9209	2.9197	2.912	2.9112	2.8952	2.8939	2.8778	2.8765	2.861	2.8596
EPCSRST_N_4	B36	2.9186	2.9165	2.9081	2.9041	2.8868	2.8801	2.8658	2.8562	2.8448	2.8322
EPCSRST_N_5	B37	2.9206	2.9195	2.9117	2.9104	2.8945	2.8927	2.877	2.8749	2.8599	2.8575
MONITOR	K23	2.9218	2.9185	2.9127	2.9076	2.8958	2.8868	2.8787	2.8662	2.8627	2.8459
PLL_MON	L20	2.9195	2.9204	2.9097	2.9129	2.8894	2.8977	2.8702	2.8827	2.8504	2.8683
TOGGLE_MON	L22	2.9205	2.9195	2.9127	2.9112	2.8968	2.895	2.881	2.879	2.8656	2.8633

Table. 18. LVTTL VOL – DUT 6864

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	216.3351	220.7859	229.2175	237.1162	244.7014	259.3704	264.2914	285.6994	285.4865	314.0112
EPCSRST_N_0	B31	216.7739	221.6322	229.813	239.1535	244.8268	262.6929	264.2601	290.307	285.9139	320.3473
EPCSRST_N_1	B32	214.7116	217.8365	224.2424	229.086	240.5229	250.21	258.2409	272.2715	276.8615	295.4919
EPCSRST_N_2	B34	216.4303	217.9927	226.5548	228.4922	243.7728	246.9914	261.9594	266.3655	281.4061	286.7165
EPCSRST_N_3	B35	215.6803	216.9303	224.8361	225.8986	240.4604	241.8041	257.6472	259.0846	275.4053	277.0122
EPCSRST_N_4	B36	218.6802	221.3051	229.6172	233.1795	249.7413	255.8035	271.1153	279.4586	293.6715	304.3676
EPCSRST_N_5	B37	216.5553	217.8052	225.3049	226.7111	241.0229	243.2103	258.3346	260.5533	276.4096	279.1966
MONITOR	K23	215.1679	217.669	225.3287	228.9554	240.3043	248.3079	257.6872	268.7547	275.7696	290.019
PLL_MON	L20	216.7063	214.3626	229.7686	223.6124	249.8933	237.1435	272.8617	252.2995	299.4669	268.9954
TOGGLE_MON	L22	214.3025	215.5225	221.685	222.7486	237.5763	239.1404	253.4051	255.501	270.1675	272.2881

Table. 19. LVTTL VOL – DUT 6874

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	214.2664	217.7142	227.3995	234.3579	242.9462	257.2077	262.7869	283.9442	284.6065	312.8924
EPCSRST_N_0	B31	214.141	218.2784	227.901	235.8624	243.1969	259.7466	263.069	287.6741	284.8453	317.7575
EPCSRST_N_1	B32	212.6492	215.0241	222.3987	226.4611	238.773	247.5226	256.7409	269.7404	275.4053	292.7551
EPCSRST_N_2	B34	213.8679	214.8678	224.2112	225.5549	241.3041	244.2415	259.8658	264.0219	279.8745	285.097
EPCSRST_N_3	B35	212.7742	213.1179	222.2113	222.18	238.0543	238.5855	255.3972	255.8347	273.4217	274.0871
EPCSRST_N_4	B36	214.9303	217.0552	226.3361	229.3047	245.3352	251.9286	265.8343	275.5838	287.6079	300.5386
EPCSRST_N_5	B37	213.2742	213.7116	222.555	222.68	238.773	239.3042	256.1785	257.0222	274.4511	275.6187
MONITOR	K23	212.3853	214.7614	222.515	225.7352	236.8652	244.8063	253.7166	265.2219	271.2711	286.4252
PLL_MON	L20	211.6751	211.5189	221.1125	220.55	233.6435	233.8935	248.8308	248.6121	262.3581	264.8345
TOGGLE_MON	L22	211.7686	212.144	219.5578	219.3076	234.9486	235.324	250.4646	251.184	266.9929	267.4823

Table. 20. LVTTL VOL – DUT 6877

		2mA		4mA		6mA		12mA		16mA	
Pin Name	Pin#	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad	Pre-rad	Post-rad
TID_BUF_OUT	A33	215.3634	219.2814	228.4339	235.9878	244.0746	258.4928	263.5392	284.7591	285.2351	313.5084
EPCSRST_N_0	B31	215.2067	219.971	228.6219	237.3669	244.0119	261.0317	263.5705	288.7084	285.1848	318.7884
EPCSRST_N_1	B32	213.9616	216.7428	223.5862	228.4922	239.648	249.1475	257.3347	271.3965	276.4975	294.588
EPCSRST_N_2	B34	216.2428	217.3365	226.1173	227.336	242.8353	245.8977	261.4595	265.2405	280.9667	285.9884
EPCSRST_N_3	B35	214.8991	215.899	223.8987	224.3049	239.8667	240.7729	256.8347	257.9596	274.991	276.2841
EPCSRST_N_4	B36	217.2115	219.6489	228.4297	231.6171	248.0851	254.5223	269.0841	278.4275	291.2486	303.4763
EPCSRST_N_5	B37	215.1491	216.3053	224.3362	225.4299	240.2417	241.7416	257.8034	259.4283	275.9828	278.2551
MONITOR	K23	213.5108	215.9495	223.4529	227.2671	237.9282	246.182	254.7484	266.9727	272.1632	287.9833
PLL_MON	L20	214.2688	212.8626	226.2061	221.8625	243.7684	235.2373	263.3618	249.862	287.2356	266.4687
TOGGLE_MON	L22	212.6445	213.3327	220.7153	220.8404	236.1686	237.2009	251.7784	253.3738	268.0971	269.4899

E. Propagation Delay

Table 21 lists the pre-irradiation and post-irradiation propagation delay measurements. It shows that the change due to radiation on each DUT is not significant and every DUT passes the 10% degradation criterion.

Table. 21. Pre-irradiation and Post-irradiation Propagation Delay Change

DUT	Total Dose	Pre-irradiation (µs)	Post-irradiation (µs)	Change Degradation (%)
6864	125 krad	0.440	0.438	-0.464
6874	125 krad	0.429	0.424	-1.031
6877	125 krad	0.426	0.424	-0.628

F. Transition Time

The figures below show the pre-irradiation and post-annealing transitions edges. In each case the radiation induced transition degradation is not observable.

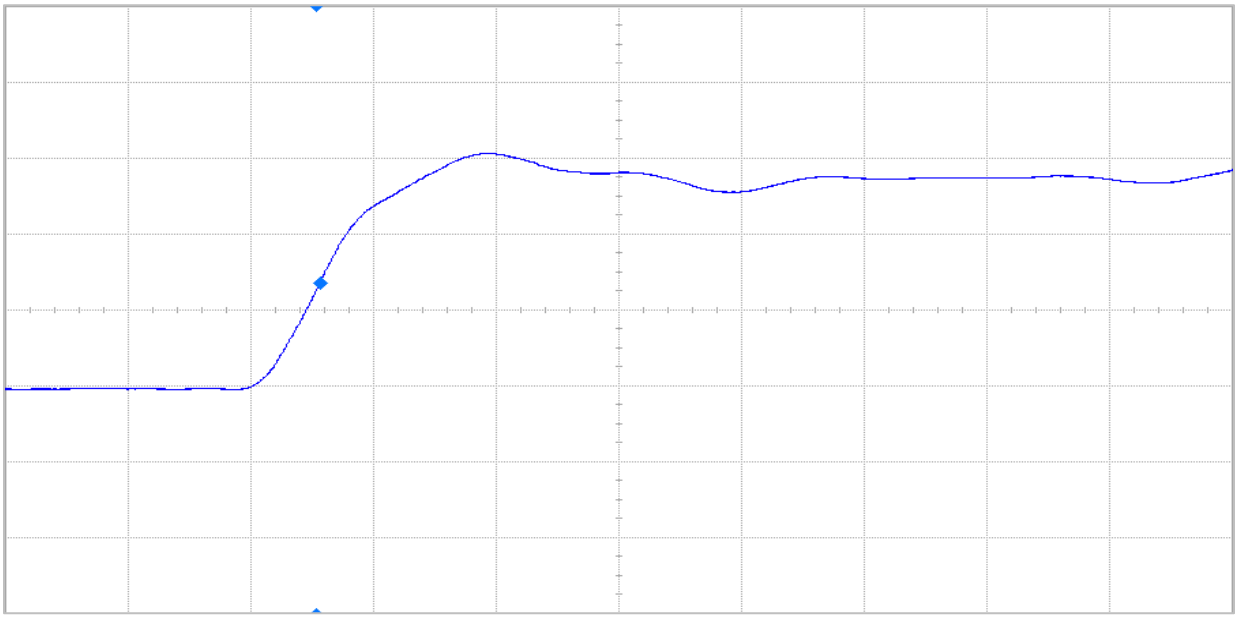

Fig. 14 (a). DUT 6864 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

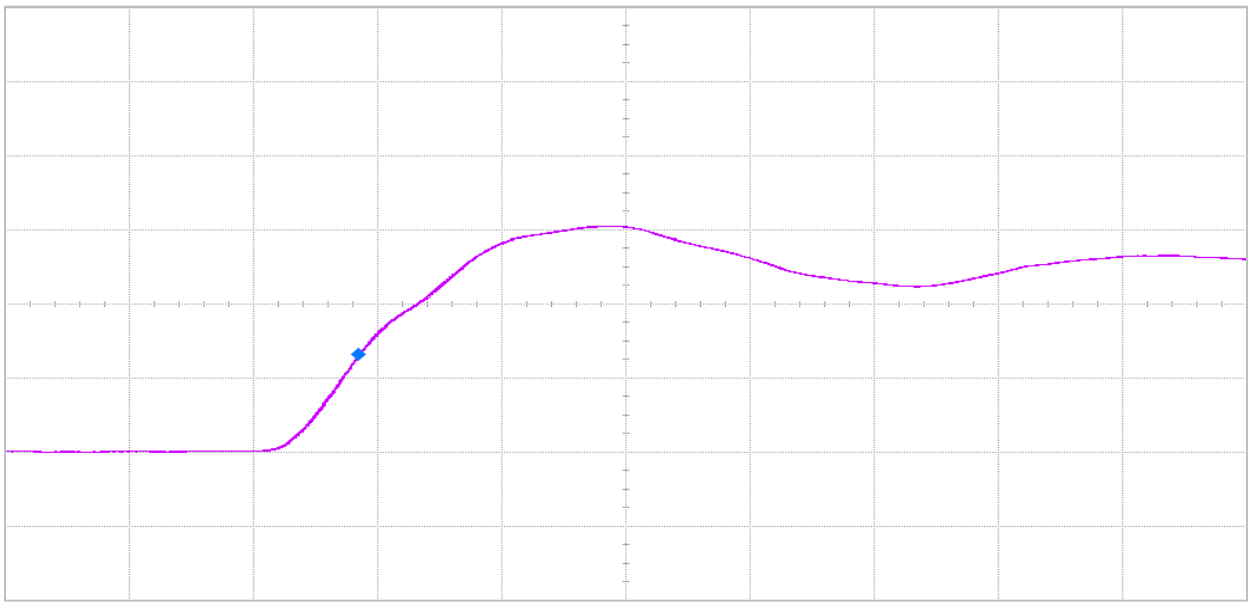

Fig. 14 (b). DUT 6864 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

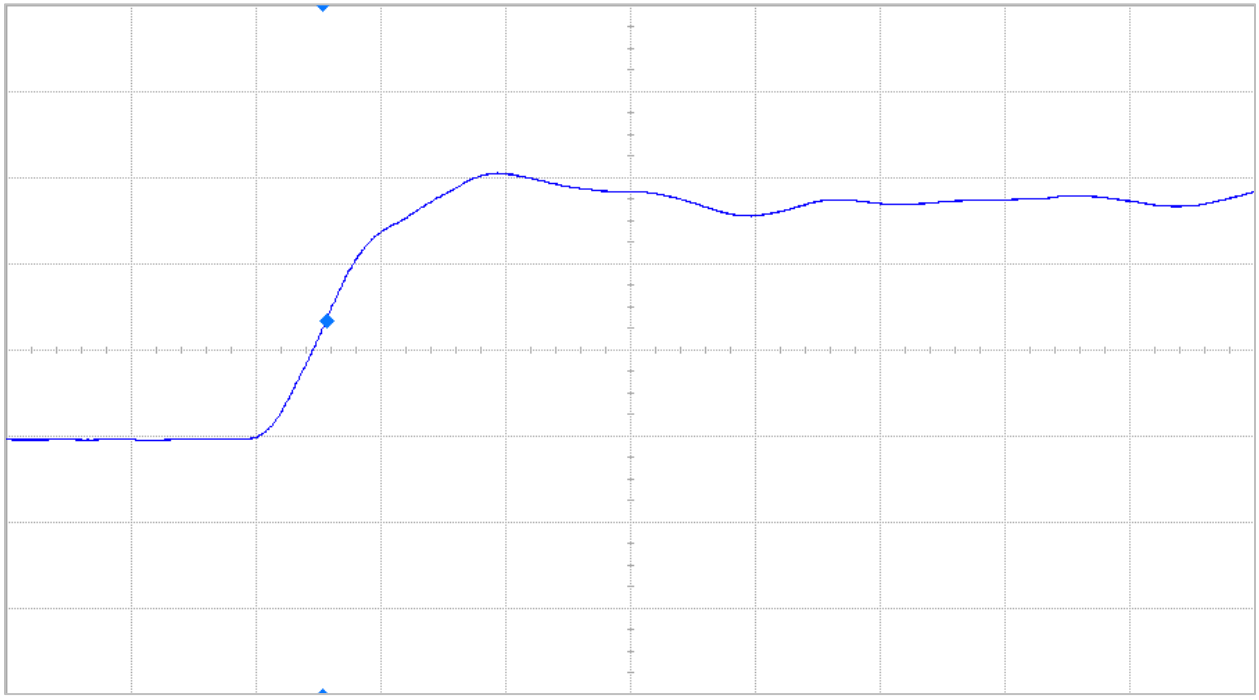

Fig. 15 (a). DUT 6874 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

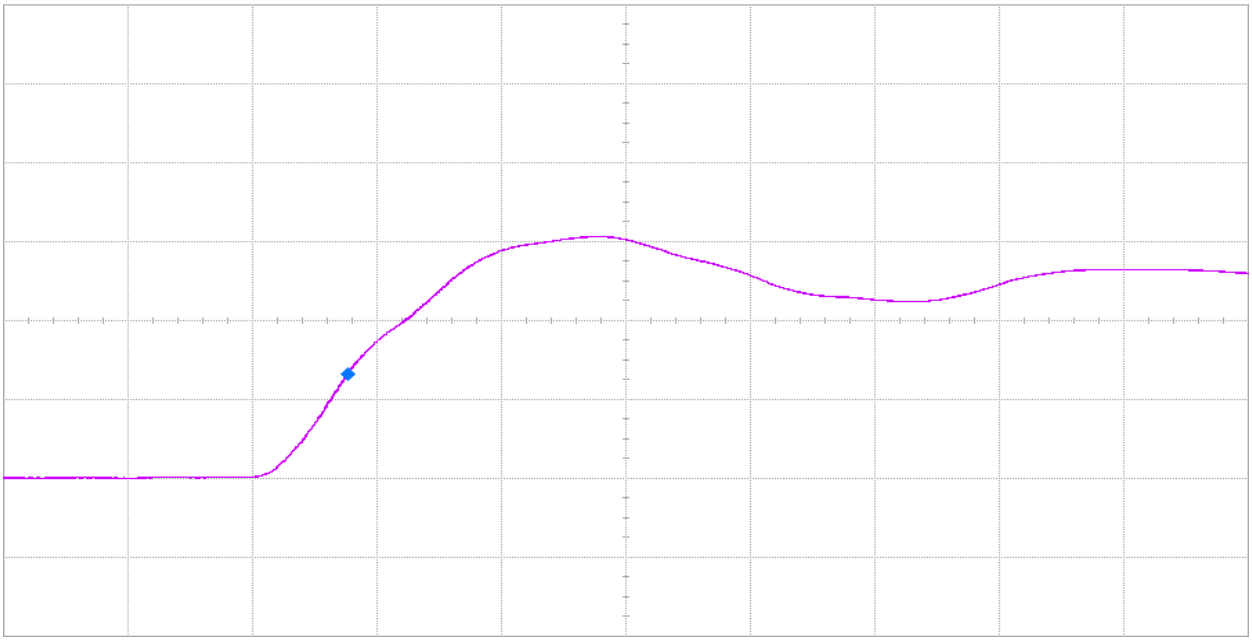

Fig. 15 (b). DUT 6874 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

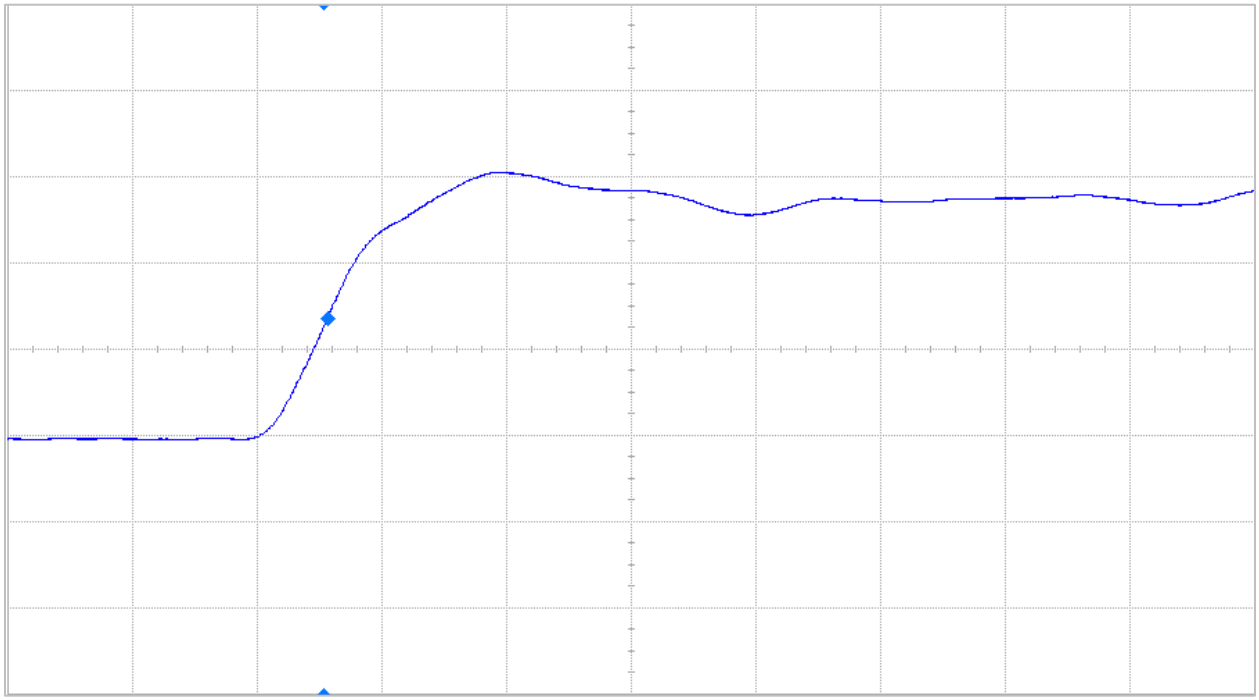

Fig. 16 (a). DUT 6877 pre-irradiation rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

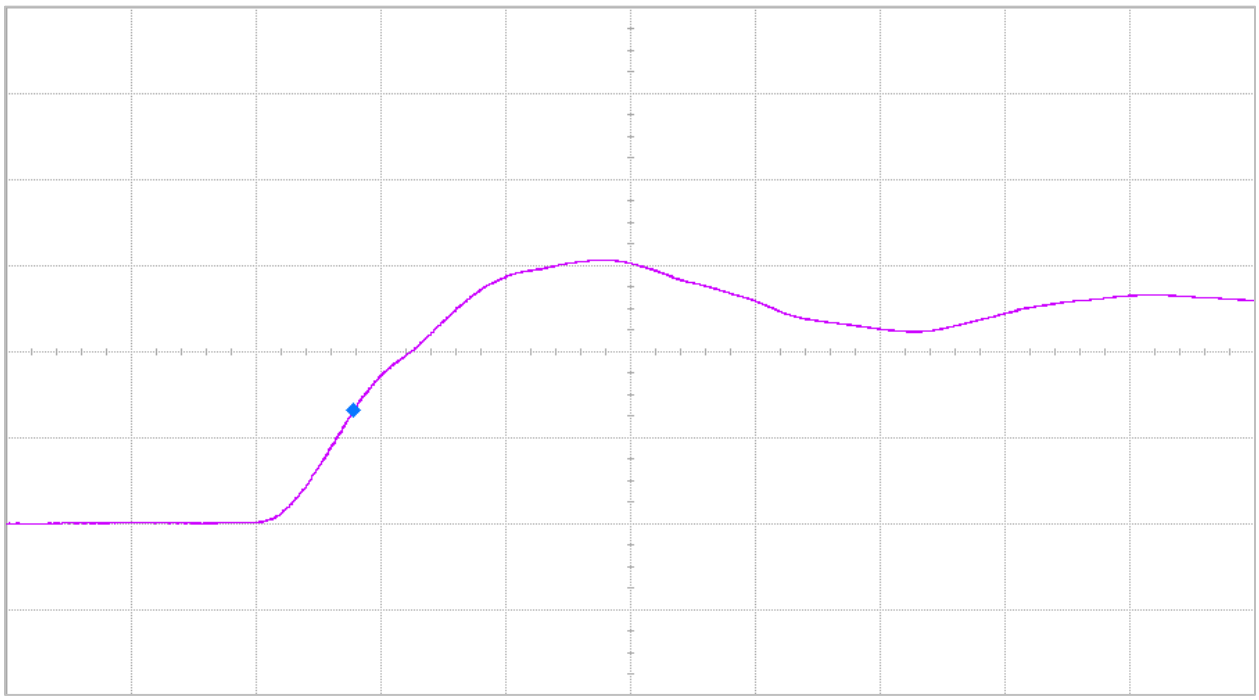

Fig. 16 (b). DUT 6877 post-annealing rising edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

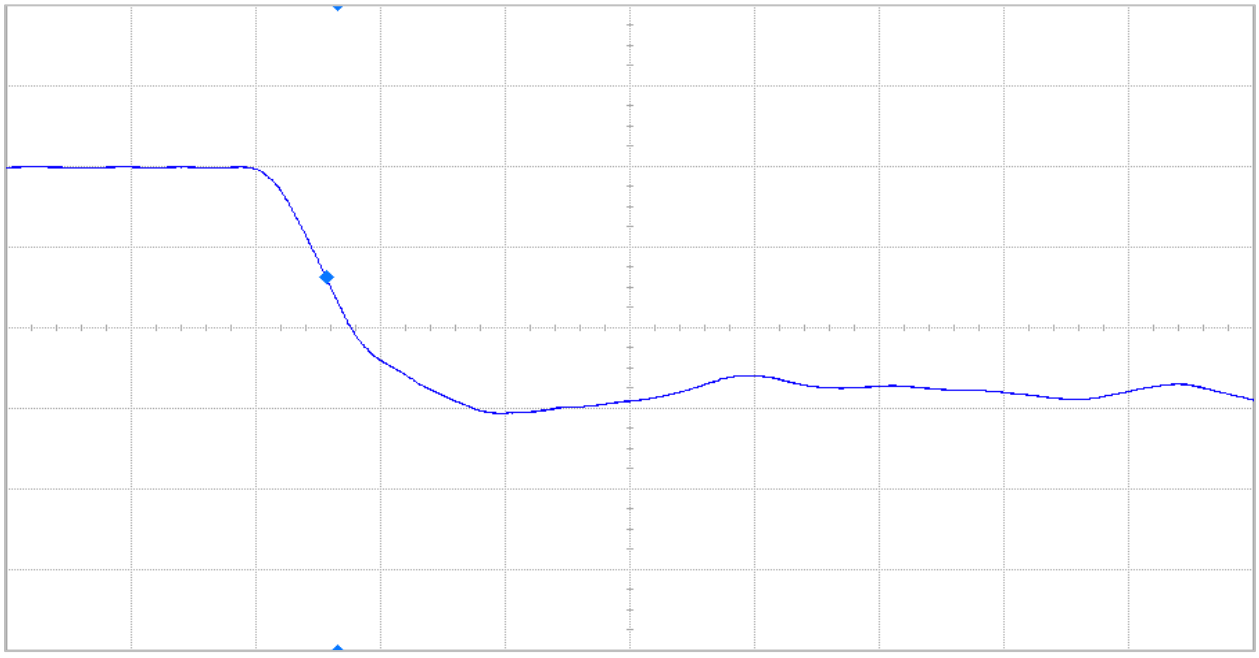

Fig. 17 (a). DUT 6864 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

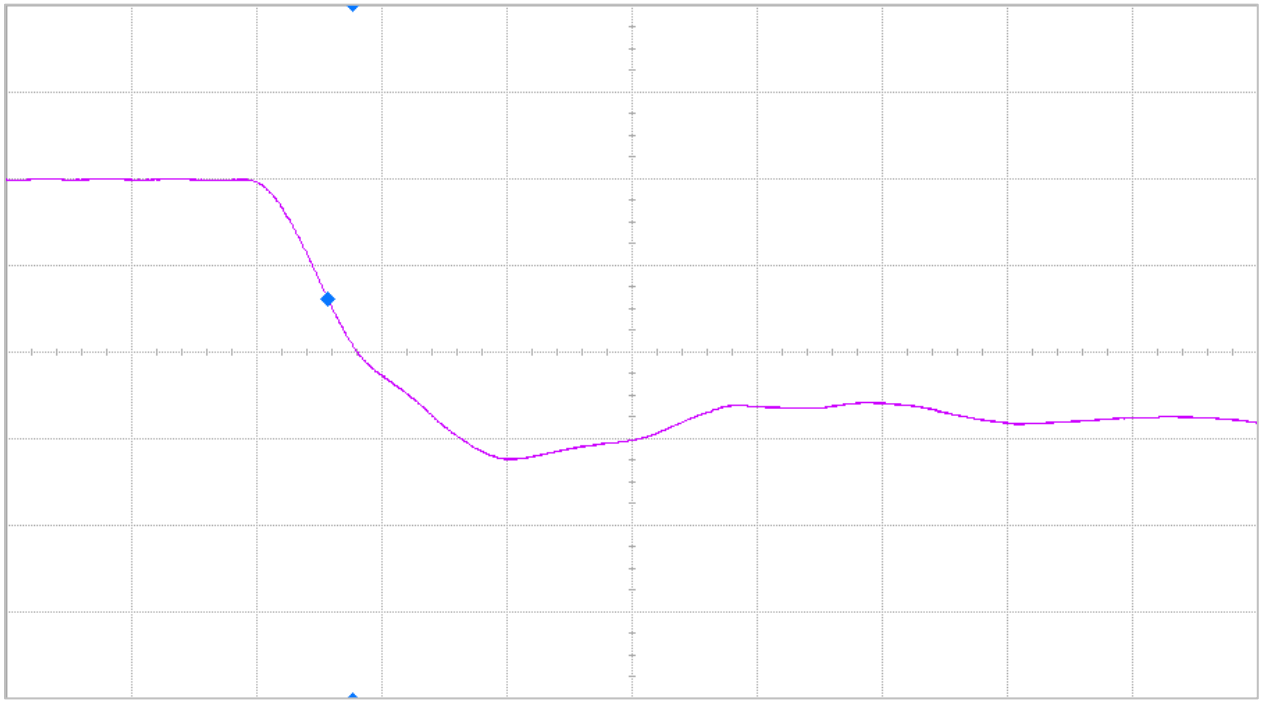

Fig. 17 (b). DUT 6864 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

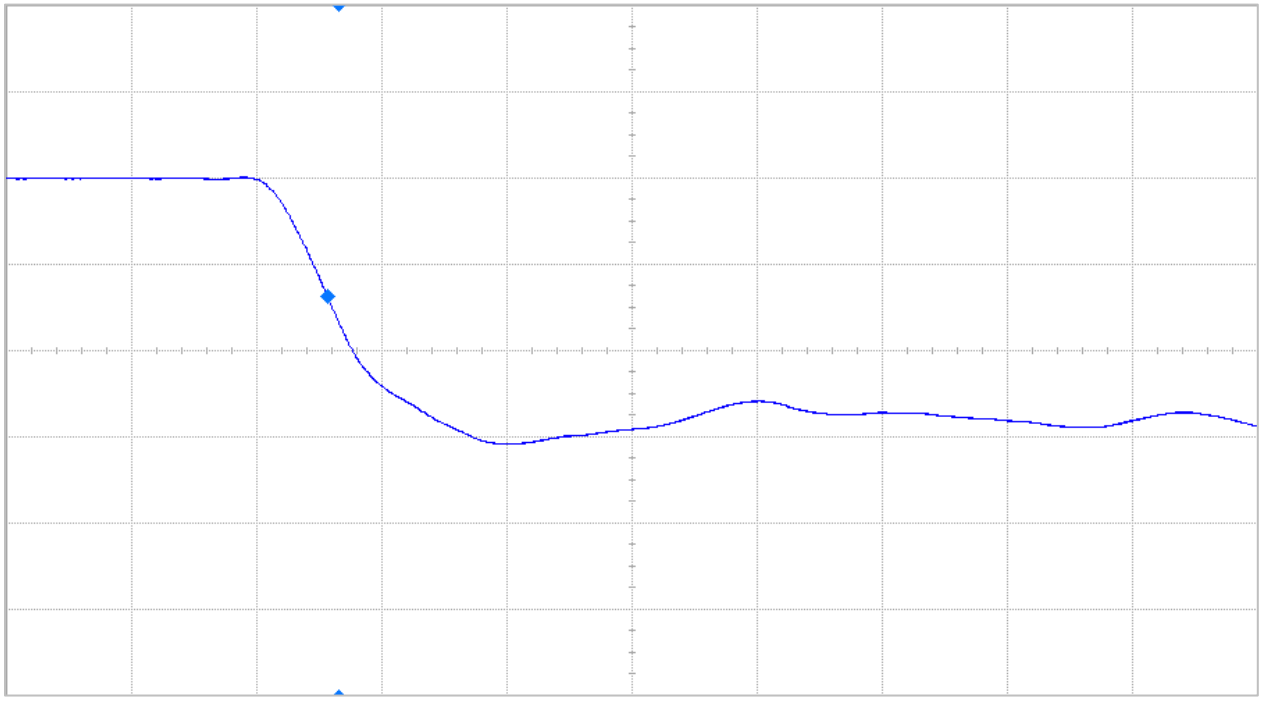

Fig. 18 (a). DUT 6874 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

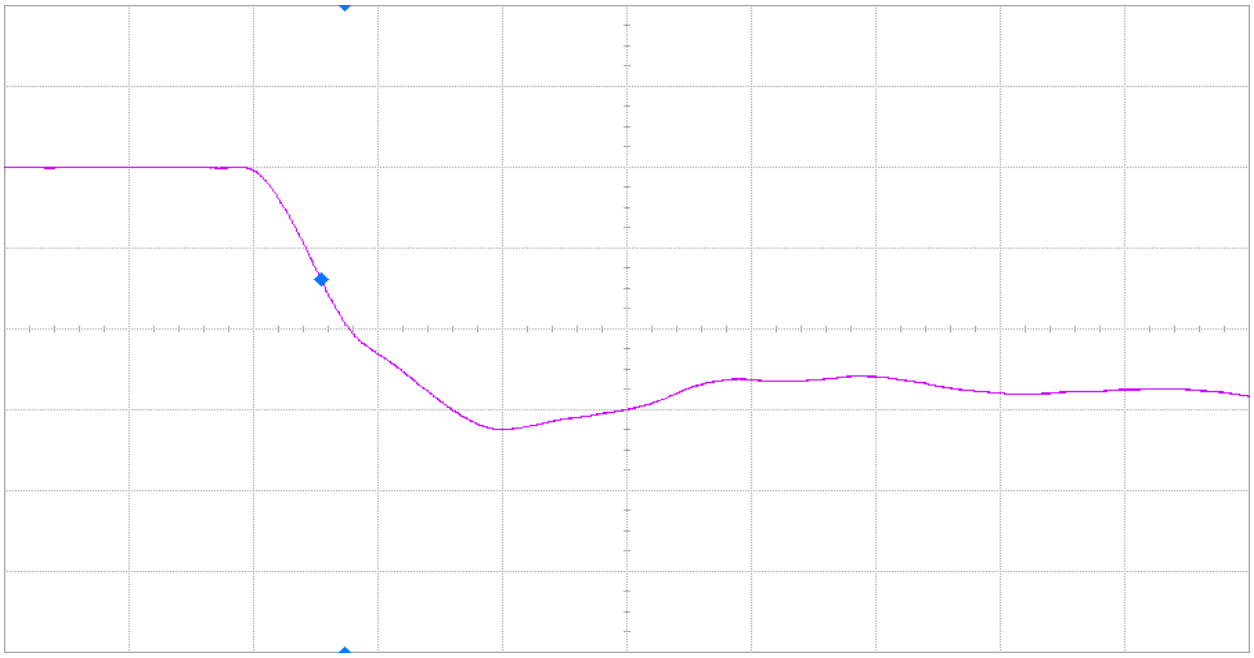

Fig. 18 (b). DUT 6874 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

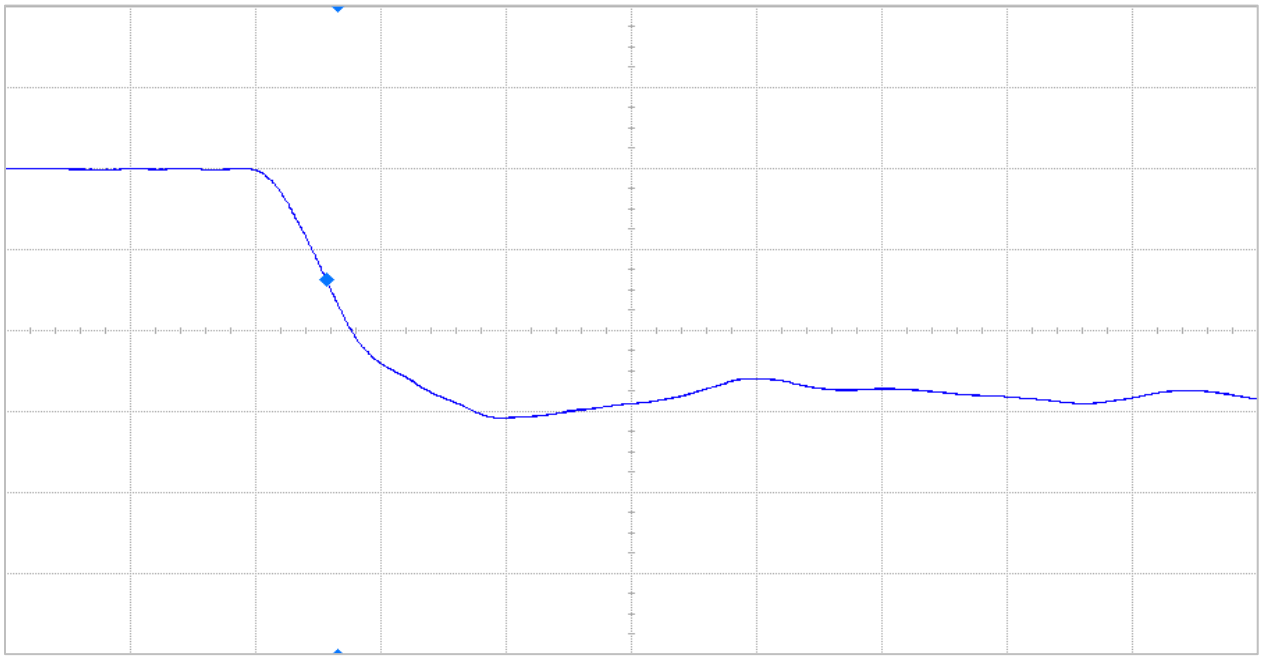

Fig. 19 (a). DUT 6877 pre-irradiation Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

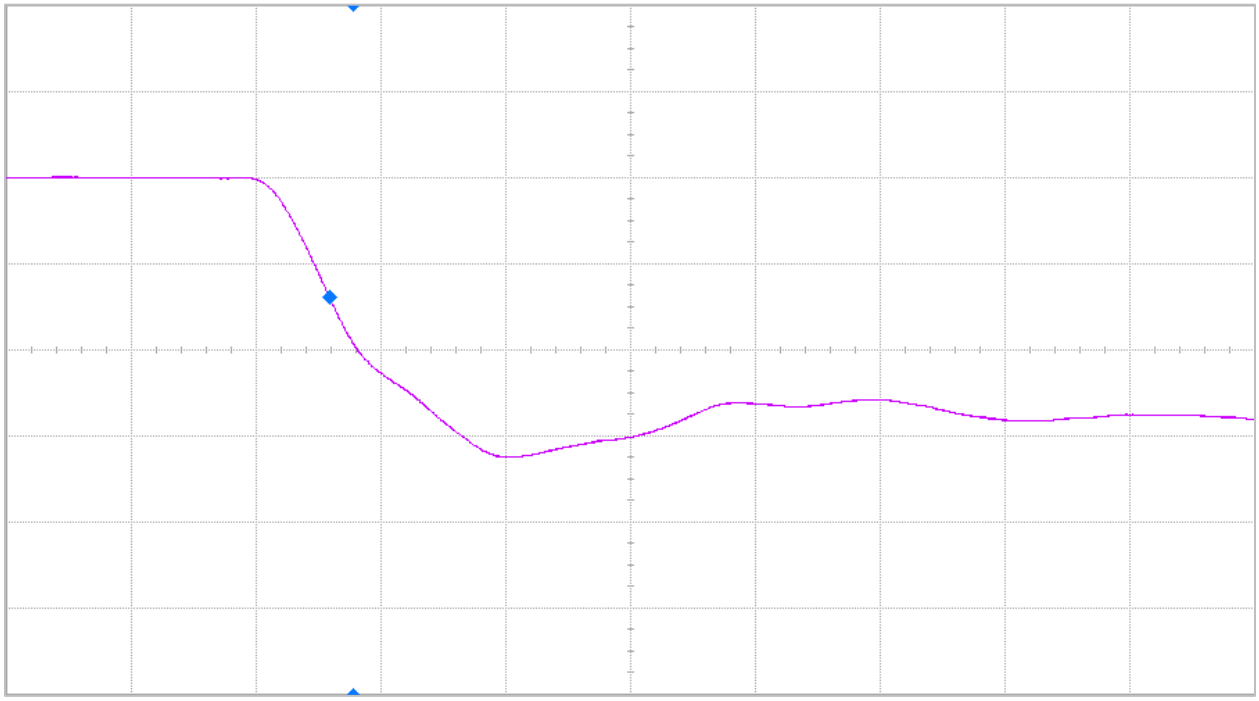

Fig. 19 (b). DUT 6877 post-annealing Falling edge, abscissa scale is 1V/div and ordinate scale is 2ns/div

Appendix A

Table. 22. High level block diagrams of blocks used to perform fabric functional coverage pre and post-irradiation

Block	**Coverage**
Combo Block	combinatorial macros available in the RTG4 library
Register Block	sequential macros available in the RTG4 library
UPROM	
Embedded SRAM Blocks	full toggle coverage on 209 fabric LSRAM & 210 uRAM blocks using dual port/ two port configurations (x18 width)
Shift Register Block	core utilization
IO Block	IO utilization
Math Block	full toggle coverage on 462 fabric math blocks with maximum width configuration

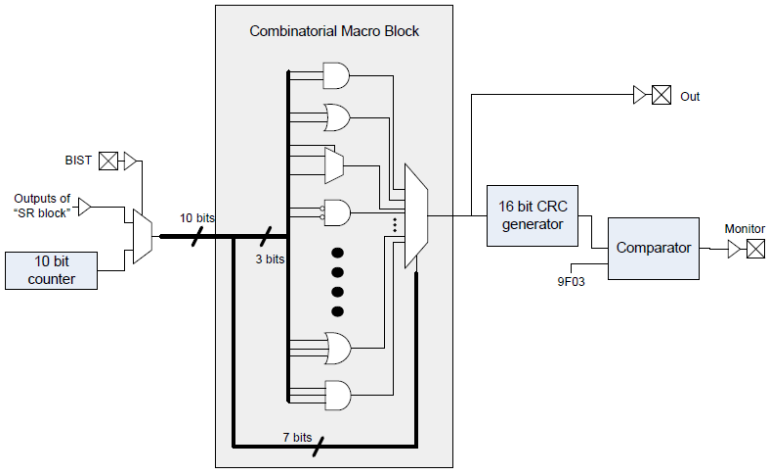

Fig. 20. Combo Block

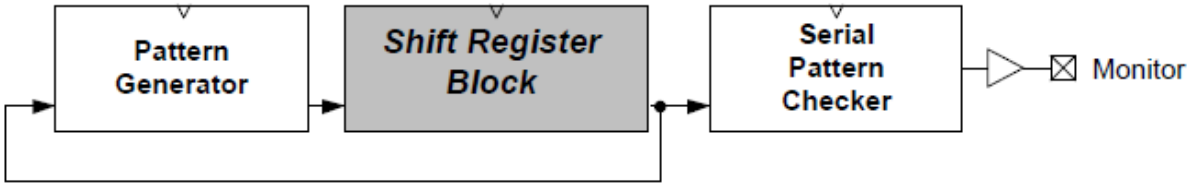

Fig. 21. Shift Register Block

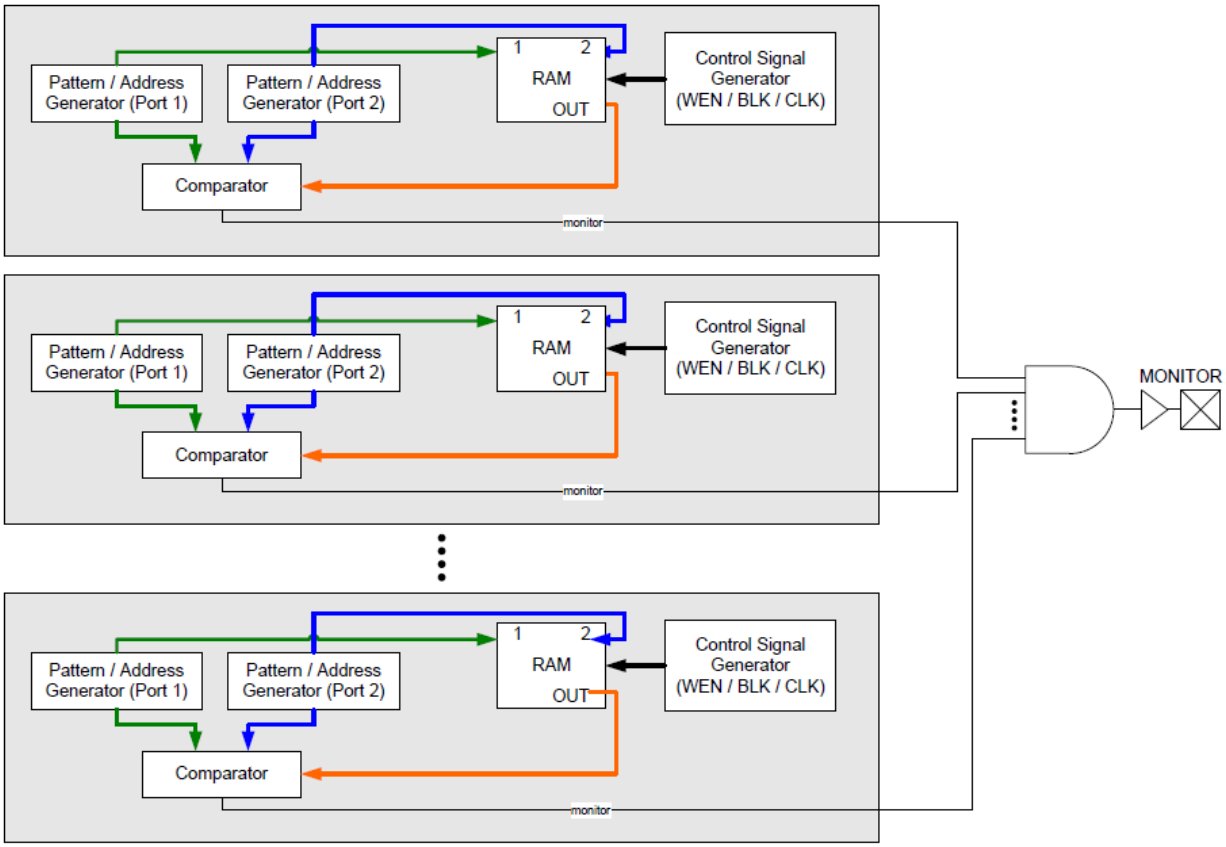

Fig. 22. Embedded Ram Blocks

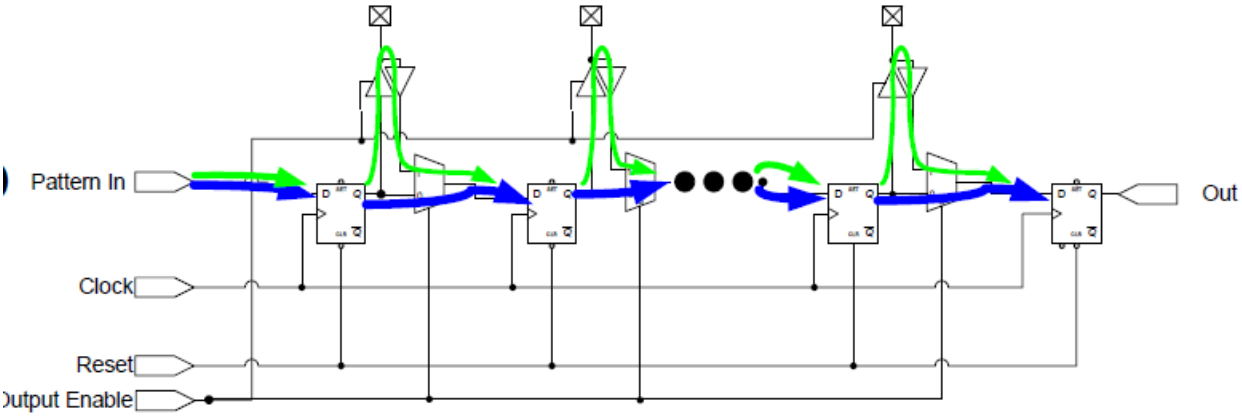

Fig. 23. IO Block

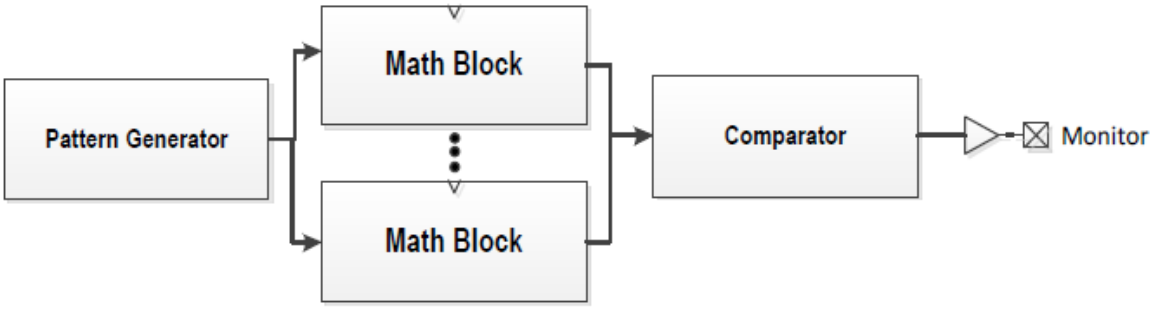

Fig. 24. Math Block