Total Ionizing Dose Test Report

No. 16T-RTAX2000D-CQ352B-D8QLF1

February 17, 2016

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I. Summary Table

Parameter	Tolerance
1. Gross Functionality	Passed 300 krad (SiO_2)
2. Power Supply Current (ICCA/ICCI)	Passed 200 krad (SiO_2)
3. Input Threshold (VTIL/VIH)	Passed 300 krad (SiO_2)
4. Output Drive (VOL/VOH)	Passed 300 krad (SiO_2)
5. Propagation Delay	Passed 300 krad (SiO_2)
6. Transition Characteristics	Passed 300 krad (SiO_2)

II. Total Ionizing Dose (TID) Testing

This testing is designed on the base of an extensive database (see TID data of antifuse-based FPGAs at http://www.klabs.org and http://www.microsemi.com/soc) accumulated from the TID testing of many generations of antifuse-based FPGAs.

A. Device-Under-Test (DUT) and Irradiation Parameters

Table 1 lists the DUT and irradiation parameters. During irradiation, each input and most of the output is grounded through a 1 MΩ resistor; during annealing, each input or output is tied to the ground or VCCI with a 2.7 kΩ resistor. Appendix A contains the schematics of the irradiation-bias circuit.

Table 1 DUT and Irradiation Parameters

Part Number	RTAX2000D
Package	CQ352B
Foundry	United Microelectronics Corp.
Technology	0.15 µm CMOS
DUT Design	TOP_AX2000S_TID
Die Lot Number	D8QLF1
Quantity Tested	6
Serial Number	300 krad(SiO2): 9392, 9395, 9410 200 krad(SiO2): 9428, 9433, 9434
Radiation Facility	Defense Microelectronics Activity
Radiation Source	Co-60
Dose Rate (±5%)	10 krad(SiO2)/min
Irradiation Temperature	Room
Irradiation and Measurement Bias (VCCI/VCCA)	Static at 3.3 V/1.5 V

B. Test Method

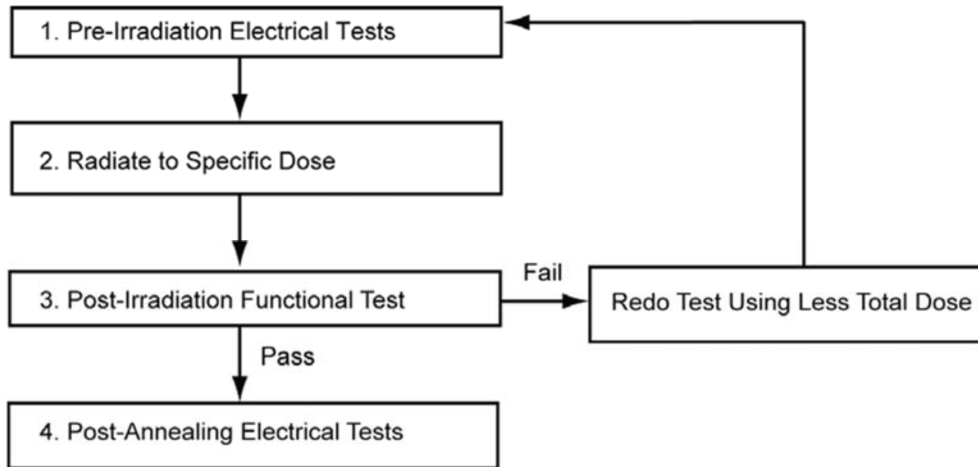

Figure 1 Parametric Test Flow Chart

The test method generally follows the guidelines in the military standard TM1019.8. Figure 1 is the flow chart describing the steps for functional and parametric tests, irradiation, and post-irradiation annealing.

The accelerated aging, or rebound test mentioned in TM1019.8, is unnecessary; because there is no adverse time-dependent effect (TDE) in Microsemi products manufactured by deep sub-micron CMOS technologies. Elevated temperature annealing basically reduces the effects originating from radiation-induced leakage currents. As indicated by test data in the following sections, the predominant radiation effects in RTAX2000D are due to radiation-induced leakage currents.

Room temperature annealing is performed in this test; the duration is approximately 7 days.

C. Design and Parametric Measurements

The DUT uses a high utilization, generic design (TOP_AX2000S_TID) to evaluate total dose effects for typical space applications. Appendix B contains the schematics and Verilog files of this design.

Table 2 lists measured electrical parameters and the corresponding logic design. The functionality is measured on the output pin (O_BS) of a combinational buffer-string with 14,000 buffers, output pins (O_ANDP_CLKF, O_ORP_CLKF, O_FF_CLKF, O_ANDC_CLKF, O_ORC_CLKF, O_ANDP_CLKG, O_ORP_CLKG, O_FF_CLKG, O_ANDC_CLKG, O_ORC_CLKG, O_ANDP_CLKH, O_ORP_CLKH, O_FF_CLKH, O_ANDC_CLKH, O_ORC_CLKH, O_ANDP_HCLKA, O_ORP_HCLKA, O_FF_HCLKA, O_ANDC_HCLKA, and O_ORC_HCLKA) of four (4) shift registers with 10,728 bits total, and half of the output pins (OUTX0, OUTX1, OUTX2, OUTX3, OUTX4, OUTX5, OUTX6 and OUTX7) of the embedded RAM configured as 16K×16.

ICC is measured on the power supply of the logic-array (ICCA) and I/O (ICCI) respectively. The input logic threshold (VIL/VIH) is measured on single-ended inputs EN8, DA, IO_I1, IO_I2, IO_I3, IO_I4, IO_I5 and IO_I6, and also on differential inputs DIO_I1P, DIO_I2P, DIO_I3P, DIO_I4P, DIO_I5P, DIO_I6P and DIO_I7P. The differential inputs are configured as LVPECL instead of LVDS; because LVPECL using 3.3 VDC, is worse than LVDS which uses 2.5 VDC. During the measurement on the differential inputs, the N (negative) side of the differential pair is biased at 1.8 V. The output-drive voltage (VOL/VOH) is measured on QA0 and YQ0. The propagation delay is measured on the output (O_BS) of the buffer string; the definition is the time delay from the triggering edge at the CLOCK input to the switching edge at the output O_BS. Both the delays of low-to-high and high-to-low output transitions are measured; the reported delay is the average of these two measurements. The transition characteristics, measured on the output O_BS, are shown as oscilloscope captures.

Table 2 Logic Design for Parametric Measurements

Parameters	Logic Design
1. Functionality	All key logic functions (O_BS, O_ANDP_CLKF, O_ORP_CLKF, O_FF_CLKF, O_ANDC_CLKF, O_ORC_CLKF, O_ANDP_CLKG, O_ORP_CLKG, O_FF_CLKG, O_ANDC_CLKG, O_ORC_CLKG, O_ANDP_CLKH, O_ORP_CLKH, O_FF_CLKH, O_ANDC_CLKH, O_ORC_CLKH, O_ANDP_HCLKA, O_ORP_HCLKA, O_FF_HCLKA, O_ANDC_HCLKA, and O_ORC_HCLKA), and outputs of embedded RAM (OUTX0, OUTX1, OUTX2, OUTX3, OUTX4, OUTX5, OUTX6 and OUTX7)
2. ICC (ICCA/ICCI)	DUT power supply
3. Input Threshold (VIL/VIH)	Single ended inputs (EN8/YQ0, DA/QA0, IO_I1/IO_O1, IO_I2/IO_O2, IO_I3/IO_O3, IO_I4/IO_O4, IO_I5/IO_O5, IO_I6/IO_O6), and differential inputs (DIO_I1P/DIO_O1, DIO_I2P/DIO_O2, DIO_I3P/DIO_O3, DIO_I4P/DIO_O4, DIO_I5P/DIO_O5, DIO_I6P/DIO_O6, DIO_I7P/DIO_O7)
4. Output Drive (VOL/VOH)	Output buffer (EN8/YQ0, DA/QA0)
5. Propagation Delay	String of buffers (CLOCK to O_BS)
6. Transition Characteristic	String of buffers output (O_BS)

III. Test Results

A. Functionality

Every DUT passed the pre-irradiation and post-annealing functional tests. The as-irradiated DUT is functionally tested on the output (O_FF_HCLKA) of the largest shift register.

B. Power Supply Current (ICCA and ICCI)

Figure 2 through Figure 6 plot the influx standby ICCA and ICCI versus total dose for each DUT. The post-annealing ICC for four different bit patterns, all '0', all '1', checkerboard and inverted-checkerboard, in the RAM are basically the same.

In compliance with TM1019.8 subsection 3.11.2.c, the post-irradiation-parametric limit (PIPL) for the post-annealing ICCI in this test is defined as the addition of highest ICCI, ICCDA and ICCDIFFA values in Table 2-6 of *the RTAX-S/SL and RTAX-DSP Radiation-Tolerant FPGAs* datasheet:

http://www.microsemi.com/soc/documents/RTAXS_DS.pdf

For ICCA, the PIPL is 500 mA; the PIPL of ICCI equals to $35 + 10 + 3.7 \times 2 = 52.4$ (mA). Note that there are 2 pairs of differential LVPECL inputs in each DUT.

Table 3 summarizes the pre-irradiation, post-irradiation right after irradiation and before anneal, and post-annealing ICCA and ICCI data.

Table 3 Pre-Irradiation, Post Irradiation and Post-Annealing ICC

DUT	Total Dose	ICCA (mA)			ICCI (mA)		
		Pre-irrad	Post-irrad	Post-ann	Pre-irrad	Post-irrad	Post-ann
9392	300 krad	2	147.09	8	63	196.13	48.85
9395	300 krad	5	120.01	9	58	210.22	62.93
9410	300 krad	3	110.22	8	55	194.44	58.83
9428	200 krad	2	10.90	3	58	87.53	34.76
9433	200 krad	2	21.00	3	54	90.54	40.60
9434	200 krad	2	7.52	3	55	104.72	33.97

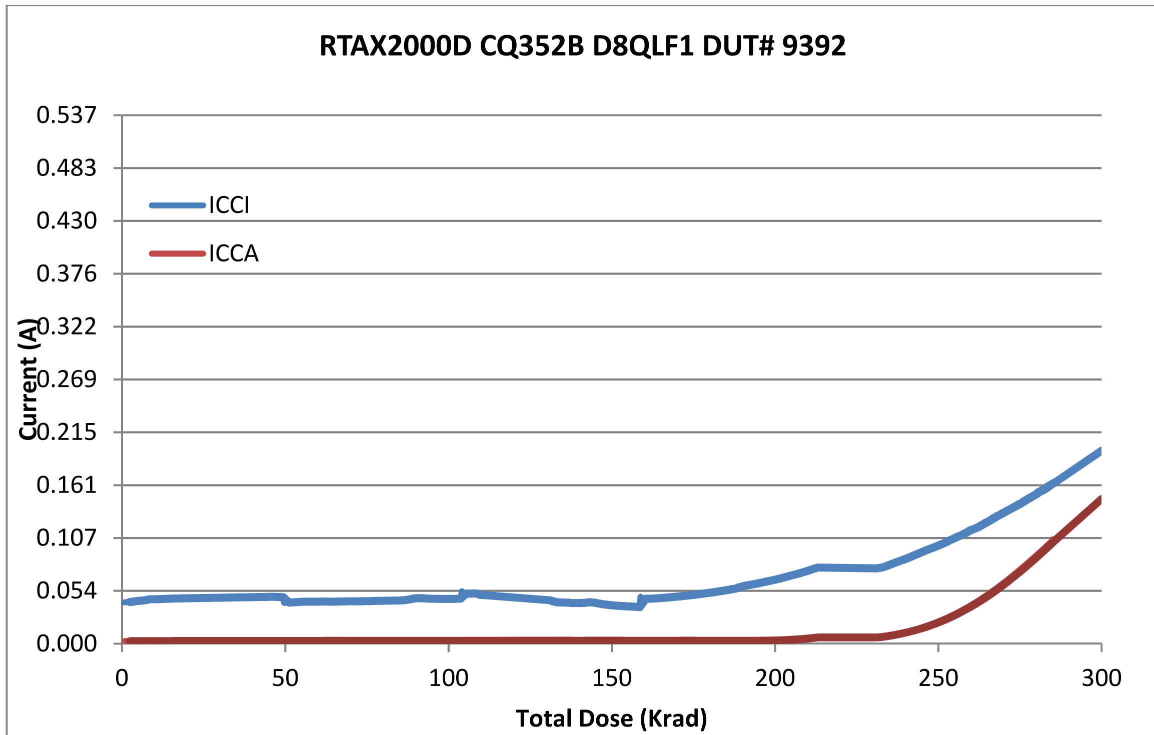

Figure 2 DUT 9392 Influx ICCA and ICCI

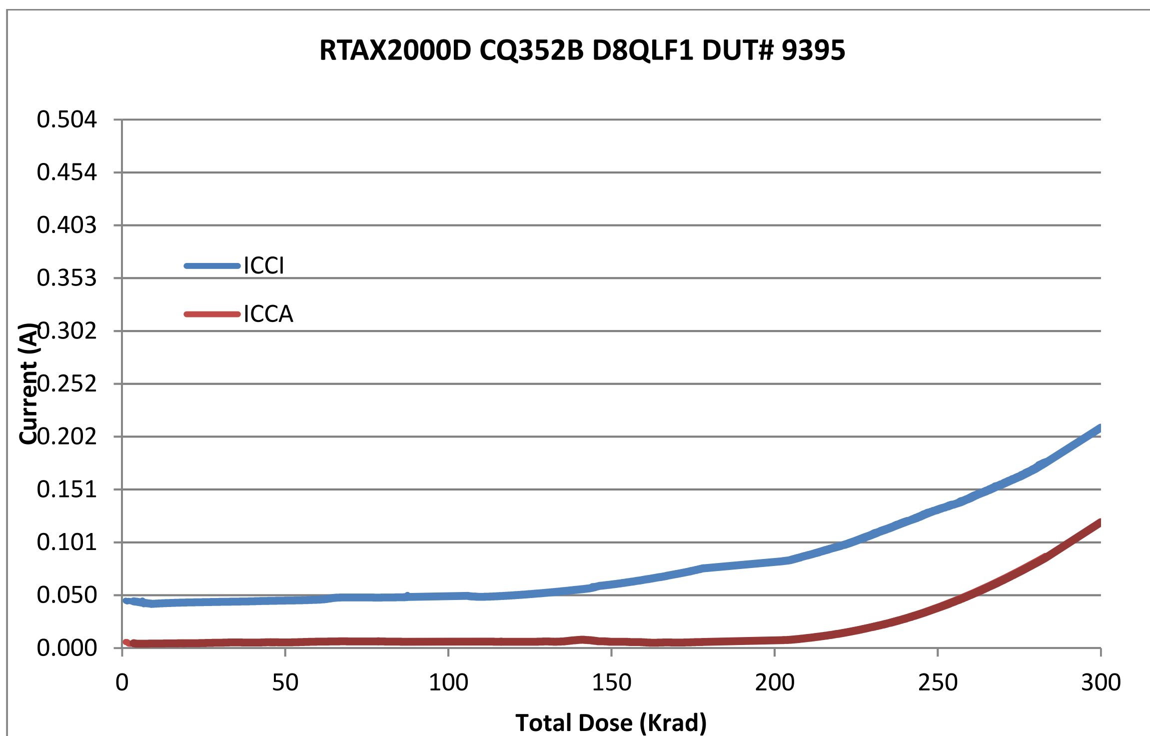

Figure 3 DUT 9395 Influx ICCA and ICCI

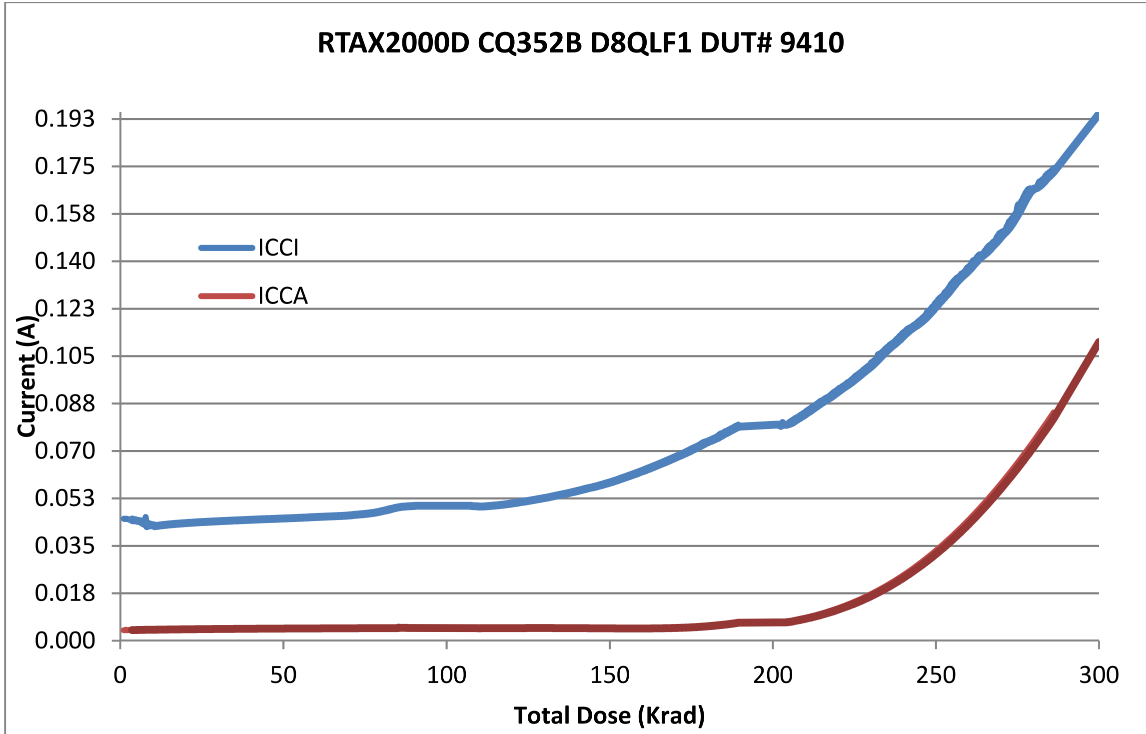

Figure 4 DUT 9410 Influx ICCA and ICCI

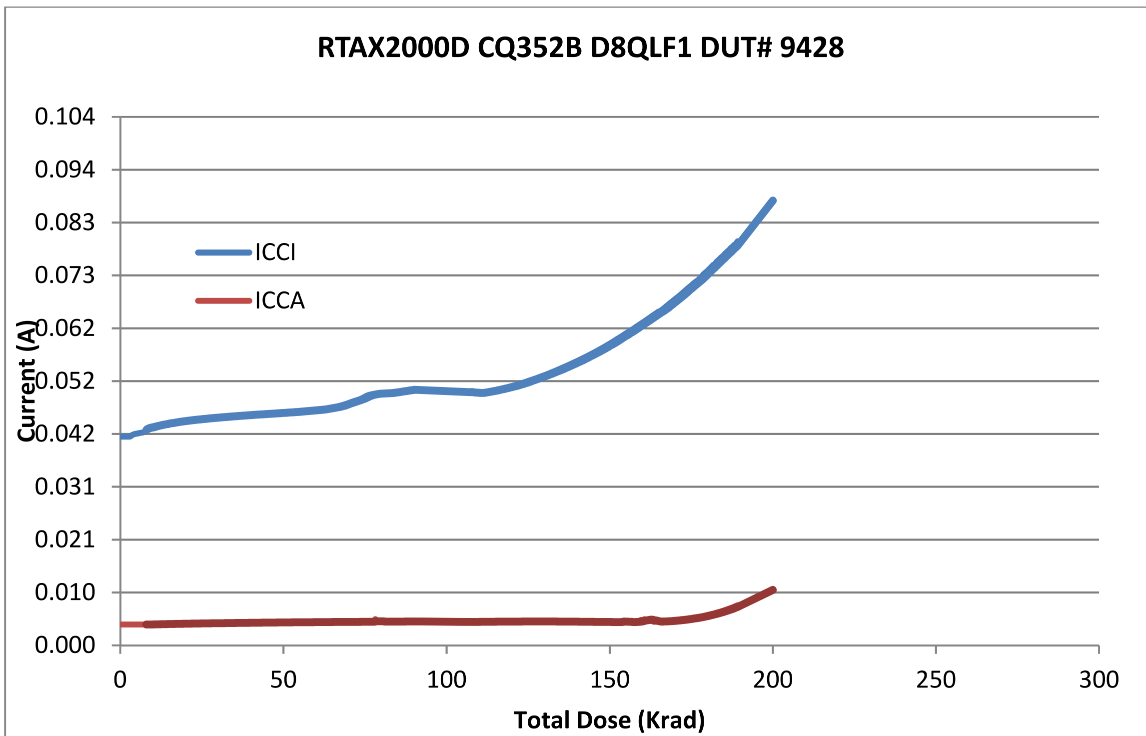

Figure 5 DUT 9428 Influx ICCA and ICCI

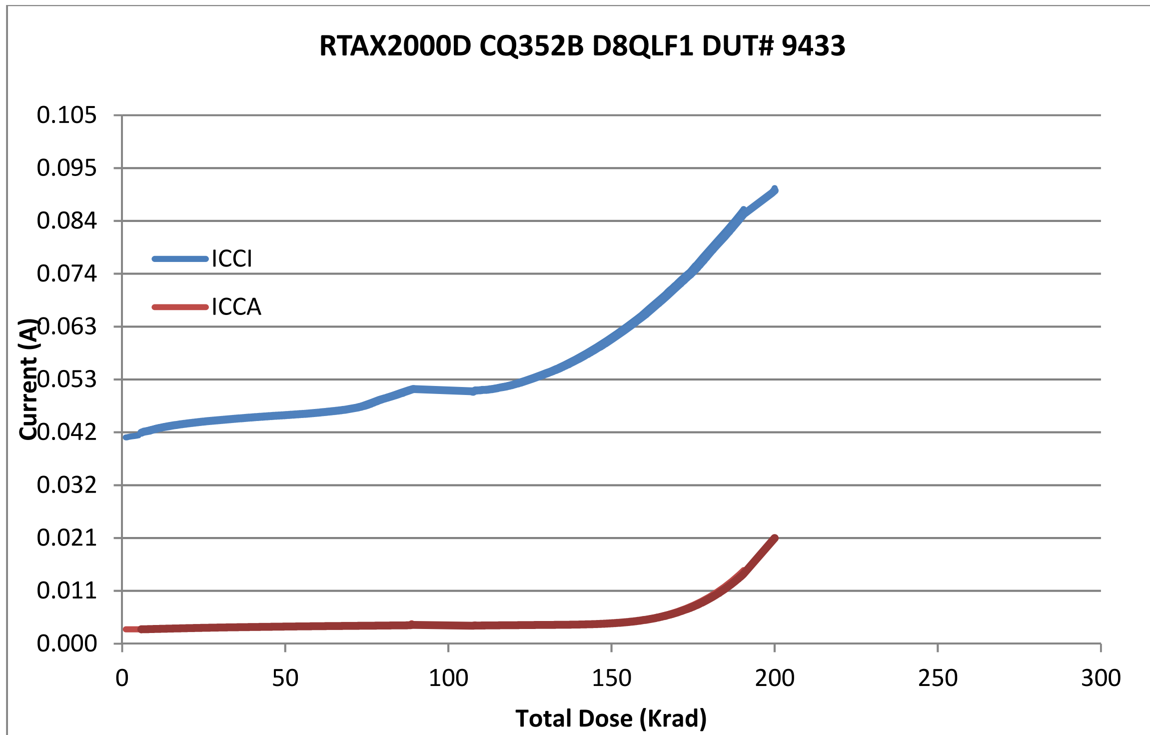

Figure 6 DUT 9433 Influx ICCA and ICCI

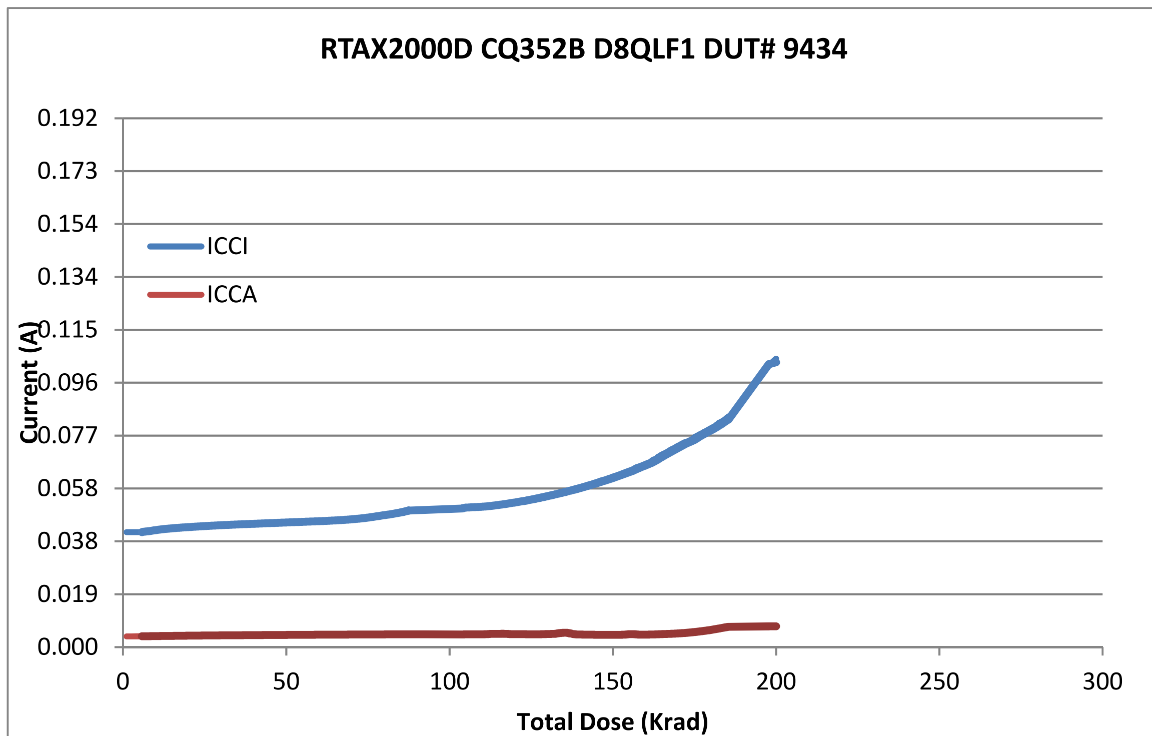

Figure 7 DUT 9434 Influx ICCA and ICCI

C. Output-Drive Voltage (VOL/VOH)

The pre-irradiation and post-annealing VOL/VOH values for various pins are listed in Tables 4 and 5. The post-annealing data are within the specification limits.

Table 4 Pre-Irradiation and Post-Annealing VOL (mV) at Various Sinking Currents and Pins

Sourcing Current	Pin\DUT	9392 (300 krad)		9395 (300 krad)		9410 (300 krad)		9428 (200 krad)		9433 (200 krad)		9434 (200 krad)	
		Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
24 mA	IO_Outs_EAQ_14	201	211	201	188	201	182	188	184	202	205	201	192
	ALU_test_mon_QBI	199	202	200	176	198	172	190	182	201	198	200	195
	Shiftout_0	229	220	227	216	229	221	211	203	230	220	227	219
16 mA	Array_out_EAQ_1	153	125	153	146	152	152	145	137	158	152	154	151
	IO_Outs_EAQ_19	185	170	183	168	185	171	174	161	185	173	183	170
	Math_acc_18x18_ok	161	167	160	167	159	166	155	156	163	163	160	160
12 mA	Math_acc_9x9_SIMD_ok	153	169	152	125	151	143	146	135	157	160	153	160
	IO_Outs_EAQ_0	160	152	159	150	159	152	151	144	160	152	159	152
	Ram_test_mon_QBI	160	149	159	122	159	175	152	141	161	168	159	154
8 mA	IO_Outs_EAQ_17	181	169	180	167	179	168	174	164	182	171	180	170
	Shiftout_2	193	178	193	177	193	178	188	174	195	180	192	180
	rcell_outz_HSB_0	186	174	186	173	185	176	182	174	191	180	186	176

Table 5 Pre-Irradiation and Post-Annealing VOH (mV) at Various Sourcing Currents and Pins

Sourcing Current	Pin\DUT	9392 (300 krad)		9395 (300 krad)		9410 (300 krad)		9428 (200 krad)		9433 (200 krad)		9434 (200 krad)	
		Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an	Pre-rad	Post-an
24 mA	IO_Outs_EAQ_14	2711	2637	2714	2715	2713	2695	2724	2725	2714	2702	2712	2717
	ALU_test_mon_QBI	2713	2621	2715	2709	2715	2683	2723	2720	2714	2709	2713	2716
	Shiftout_0	2681	2675	2685	2682	2682	2677	2699	2696	2684	2683	2683	2681
16 mA	Array_out_EAQ_1	2766	2762	2767	2764	2769	2771	2776	2772	2766	2763	2767	2764
	IO_Outs_EAQ_19	2738	2740	2740	2744	2738	2741	2747	2752	2740	2743	2739	2744
	Math_acc_18x18_ok	2761	2760	2762	2762	2762	2761	2767	2766	2761	2761	2762	2762
12 mA	Math_acc_9x9_SIMD_ok	2760	2752	2762	2768	2763	2782	2769	2766	2761	2757	2761	2757
	IO_Outs_EAQ_0	2755	2749	2758	2754	2756	2751	2763	2760	2757	2754	2755	2752
	Ram_test_mon_QBI	2753	2750	2756	2755	2754	2753	2762	2816	2756	2756	2755	2759
8 mA	IO_Outs_EAQ_17	2717	2712	2720	2717	2720	2716	2724	2721	2721	2718	2718	2716
	Shiftout_2	2708	2705	2709	2708	2708	2706	2713	2713	2709	2710	2709	2709
	rcell_outz_HSB_0	2714	2709	2715	2712	2716	2711	2718	2714	2714	2711	2714	2712

D. Propagation Delay

The propagation delay was measured in-situ, post-irradiation, and post-annealing. The results are plotted in Figure 8, and listed in Table 6. As shown in Figure 8, the propagation delay moves with the total dose, but the change is small throughout the irradiation. Referring to influx static current plots (Figure 2 through Figure 6), a device probably heats up as the dose increases. The rising temperature could be the root cause of the increasing trend at high doses. The post-annealing data, on the other hand, show decreased delay in every case.

The radiation delta in every case is well within the 10% degradation criterion. The user can take the worst case for the design margin consideration.

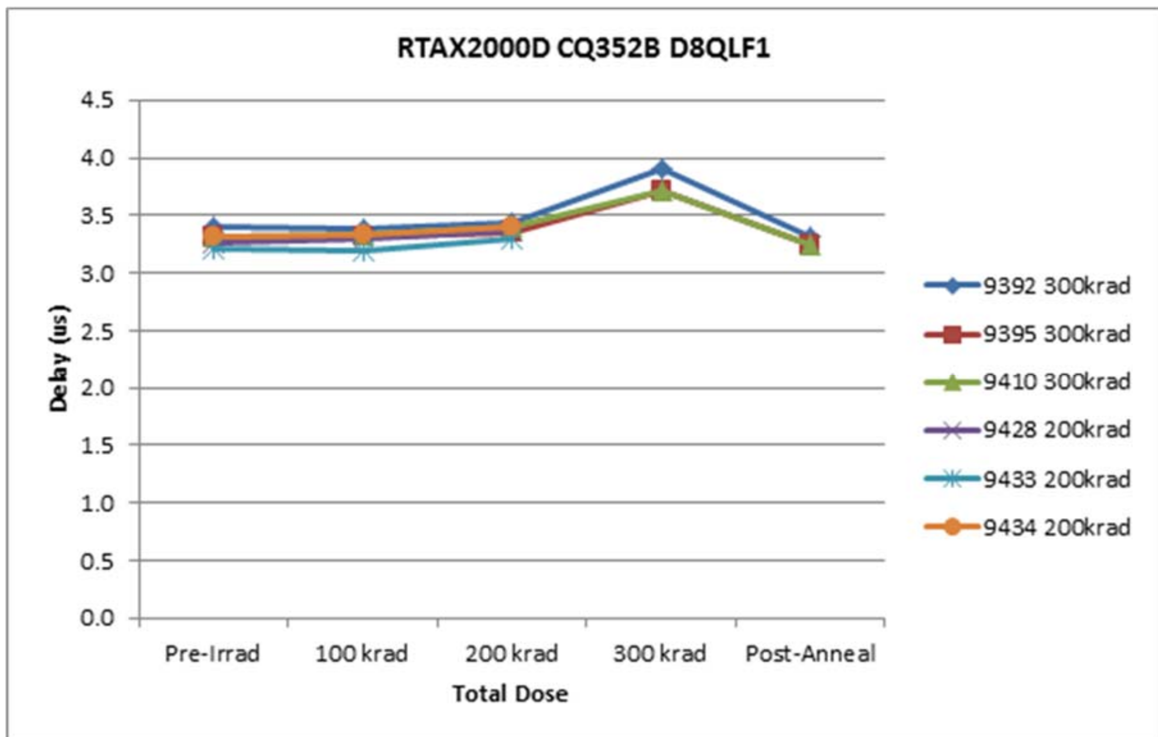

Figure 8 In-Situ Propagation Delay versus Total Dose

Table 6 Radiation-Induced Propagation Delay Degradations

Delay (µs)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	9392	300 krad	3.41	3.39	3.44	3.91	3.32
	9395	300 krad	3.32	3.32	3.35	3.72	3.25
	9410	300 krad	3.32	3.33	3.4	3.71	3.24
	9428	200 krad	3.27	3.29	3.36	-	3.19
	9433	200 krad	3.21	3.2	3.29	-	3.11
	9434	200 krad	3.32	3.33	3.41	-	3.23
Radiation Δ (%)							
	DUT	**Total Dose**	**Pre-rad**	**100 krad**	**200 krad**	**300 krad**	**Post-ann**
	9392	300 krad	-	-0.58 %	0.88 %	14.67 %	-2.63 %
	9395	300 krad	-	0 %	0.91 %	12.05 %	-2.1 %
	9410	300 krad	-	0.31 %	2.41 %	11.75 %	-2.4 %
	9428	200 krad	-	0.62 %	2.76 %	-	-2.44 %
	9433	200 krad	-	-0.31 %	2.5 %	-	-3.11 %
	9434	200 krad	-	0.31 %	2.72 %	-	-2.71 %

E. Transition Characteristics

Figure 9a to Figure 19b show the pre-irradiation and post-annealing transition edges. In each case, the radiation-induced transition-time degradation is insignificant.

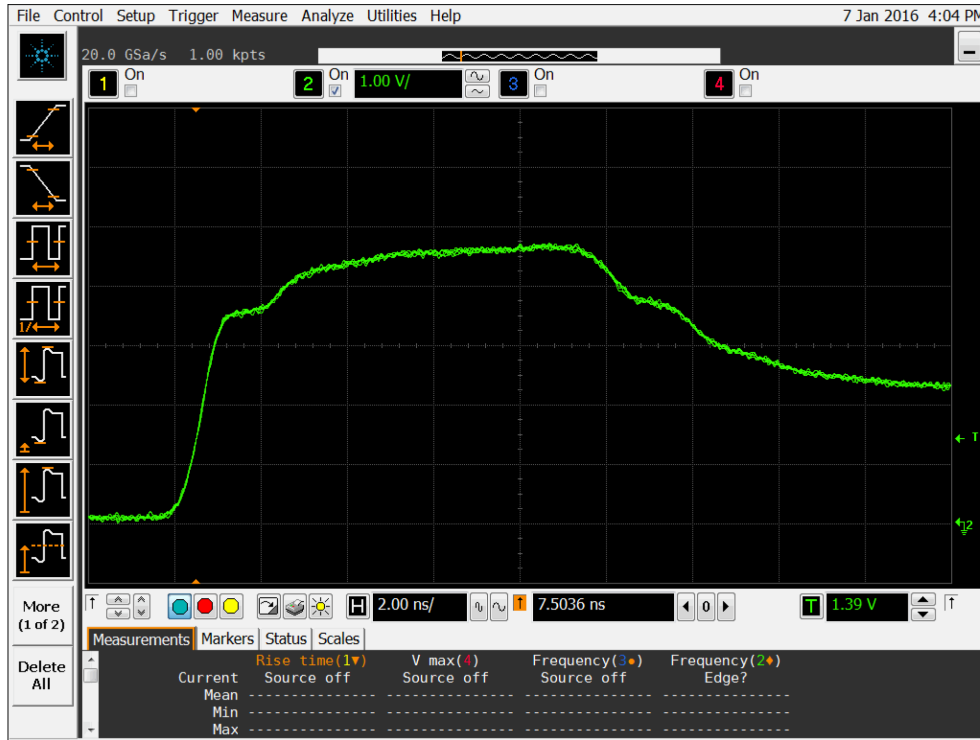

Figure 9a DUT 9392 Pre-Irradiation Rising Edge

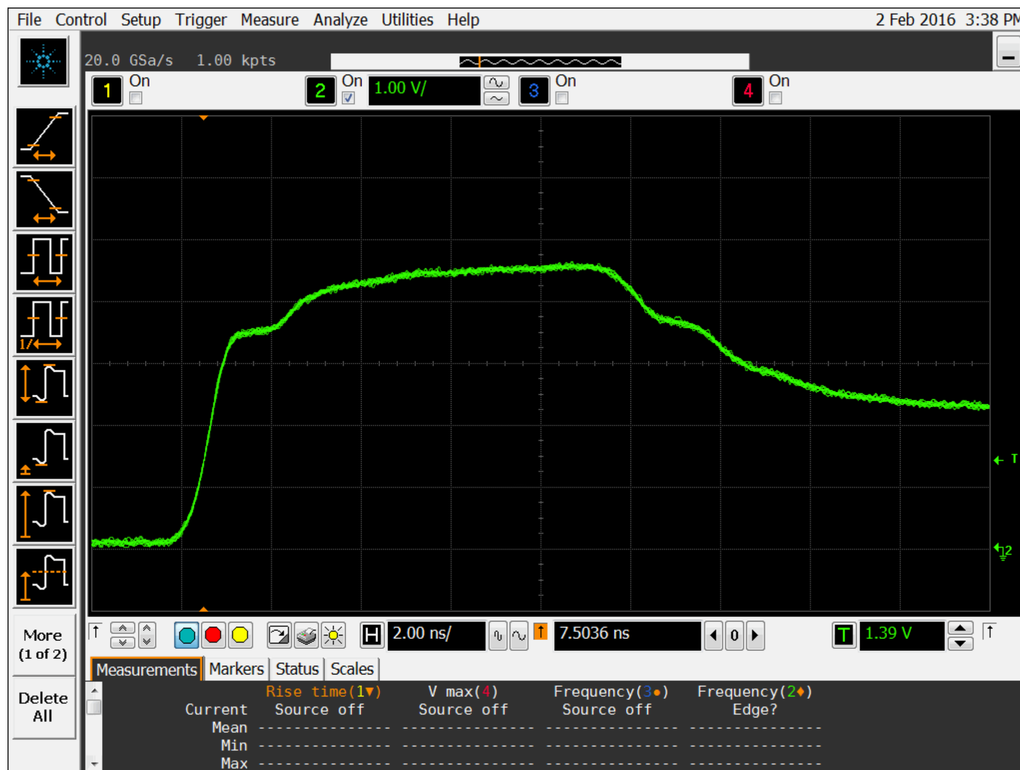

Figure 9b DUT 9392 Post-Annealing Rising Edge

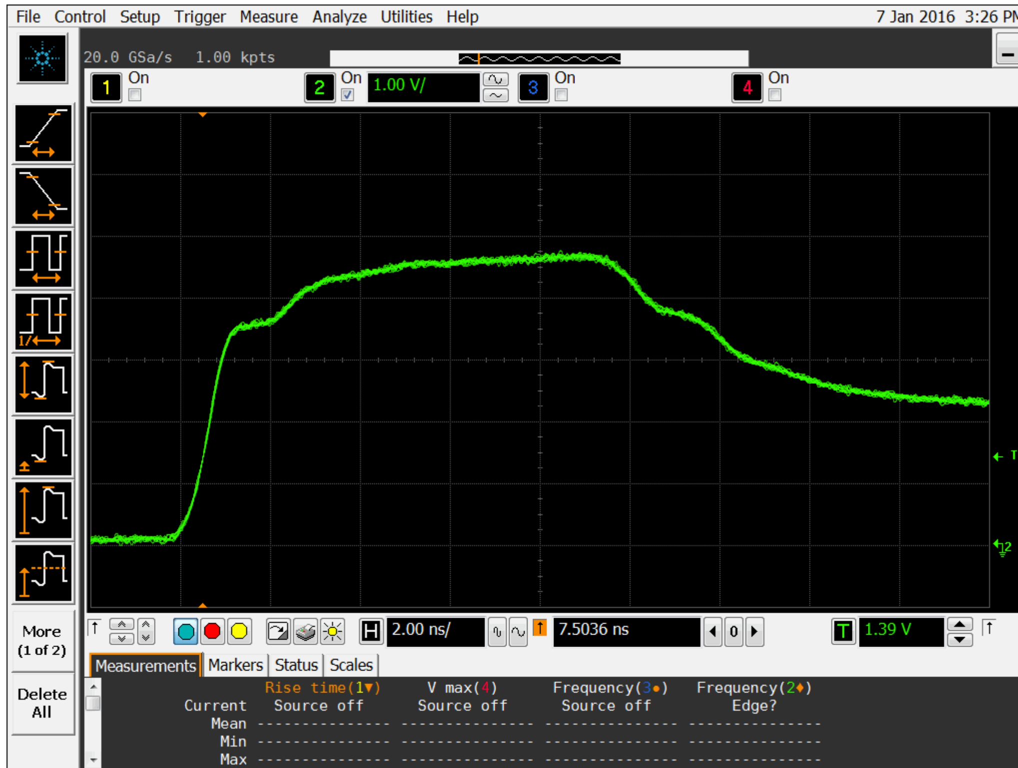

Figure 10a DUT 9395 Pre-Irradiation Rising Edge

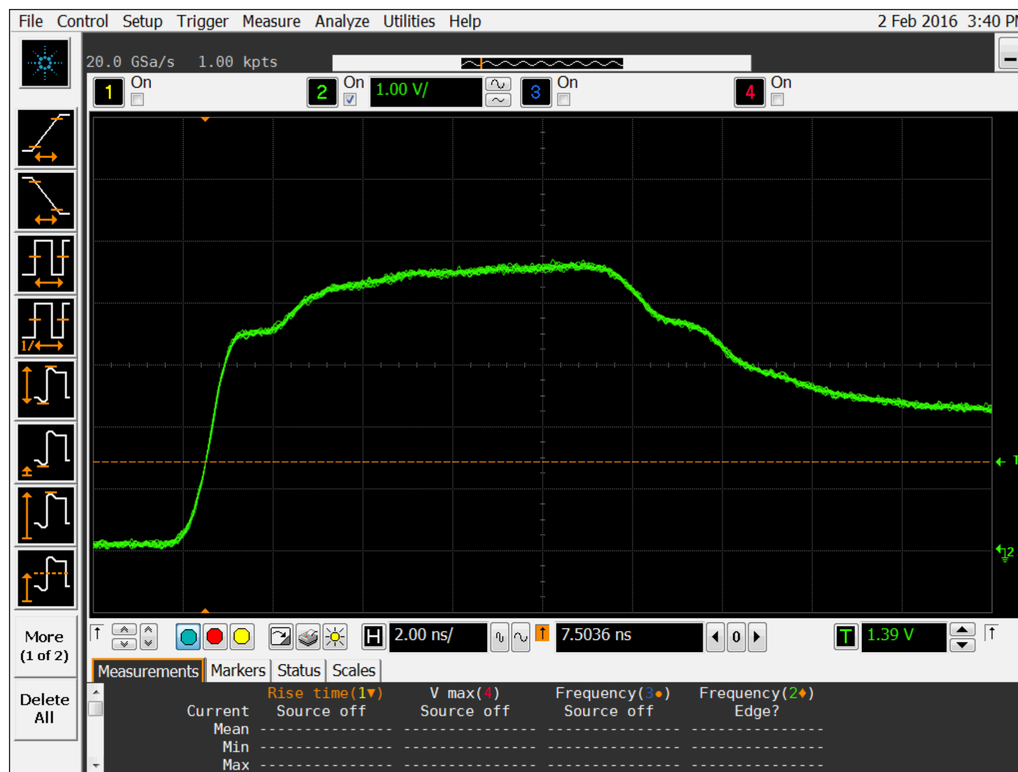

Figure 10b DUT 9395 Post-Annealing Rising Edge

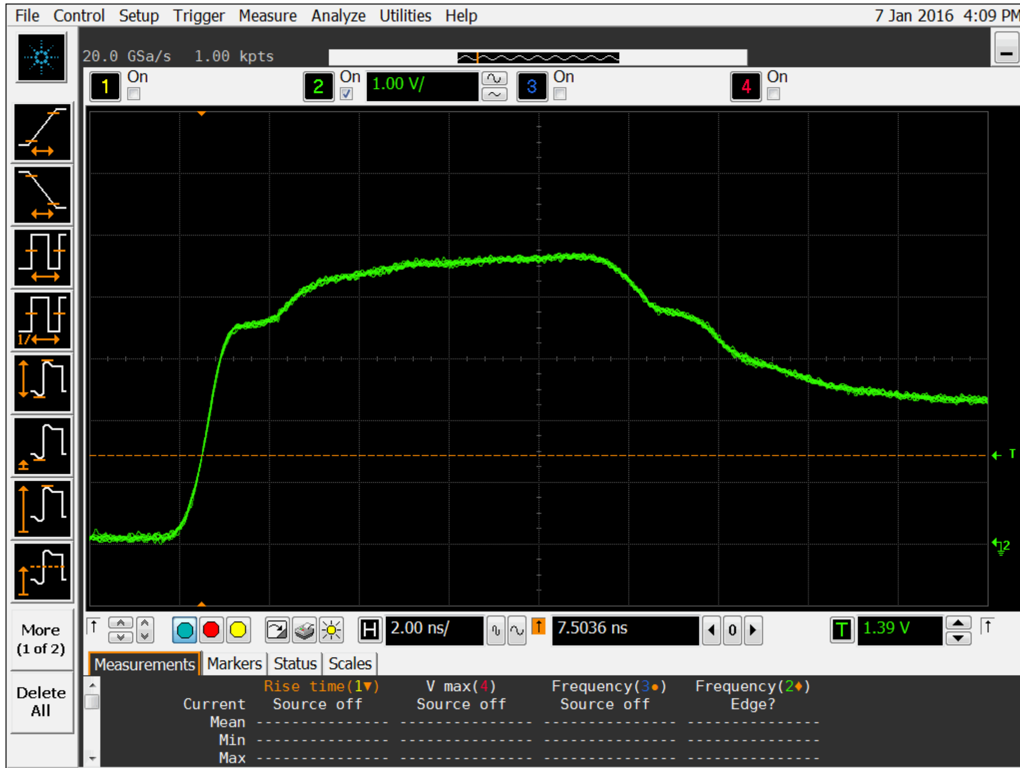

Figure 11a DUT 9410 Pre-Radiation Rising Edge

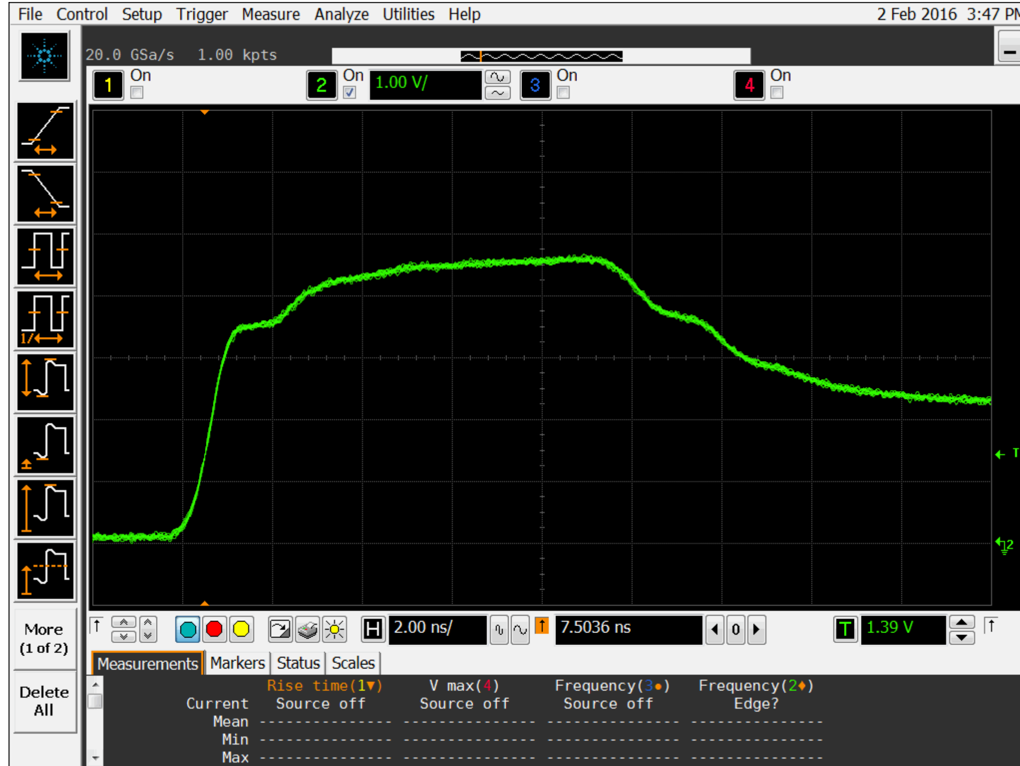

Figure 11b DUT 9410 Post-Annealing Rising edge

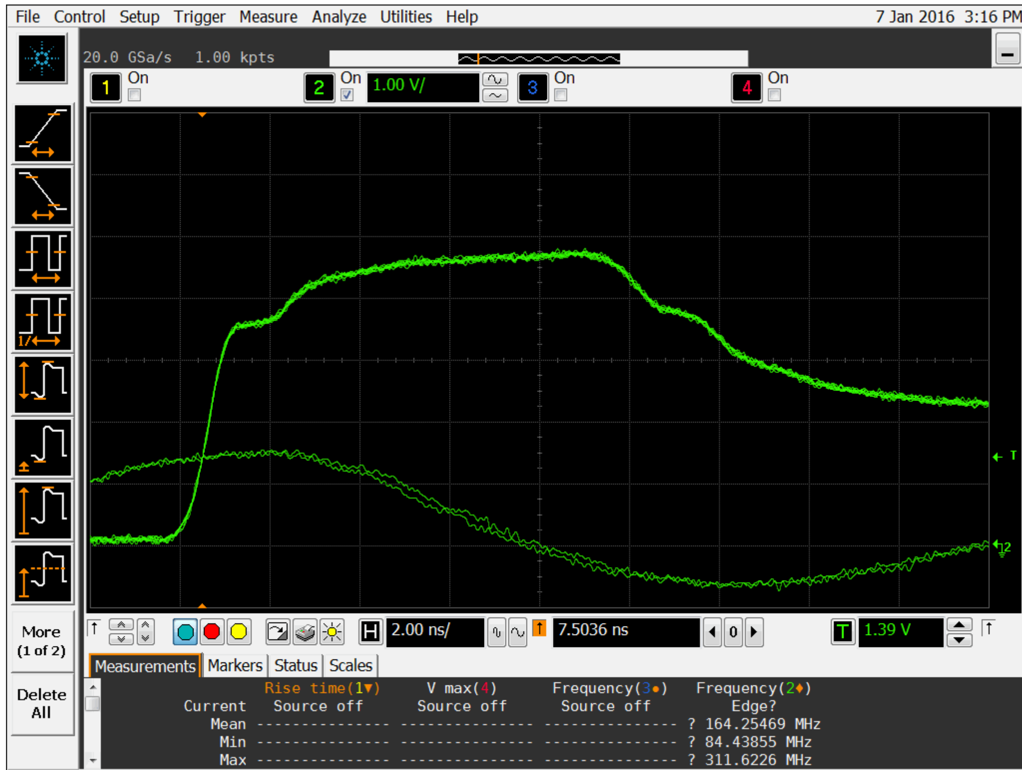

Figure 12a DUT 9428 Pre-Irradiation Rising Edge

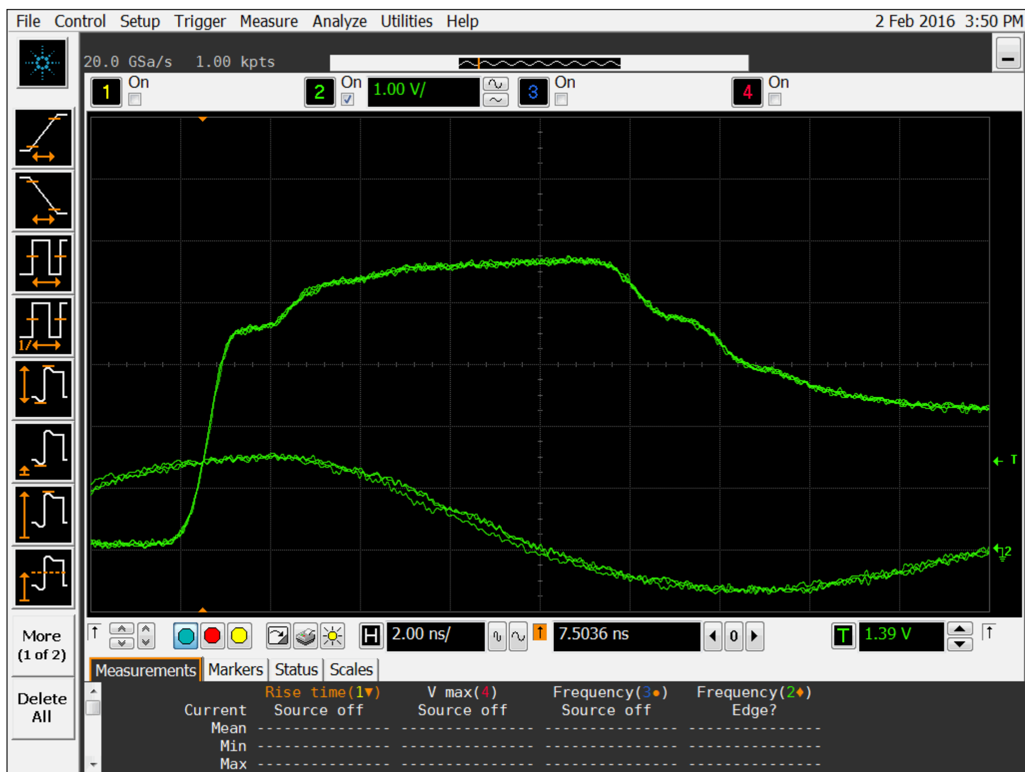

Figure 12b DUT 9428 Post-Annealing Rising Edge

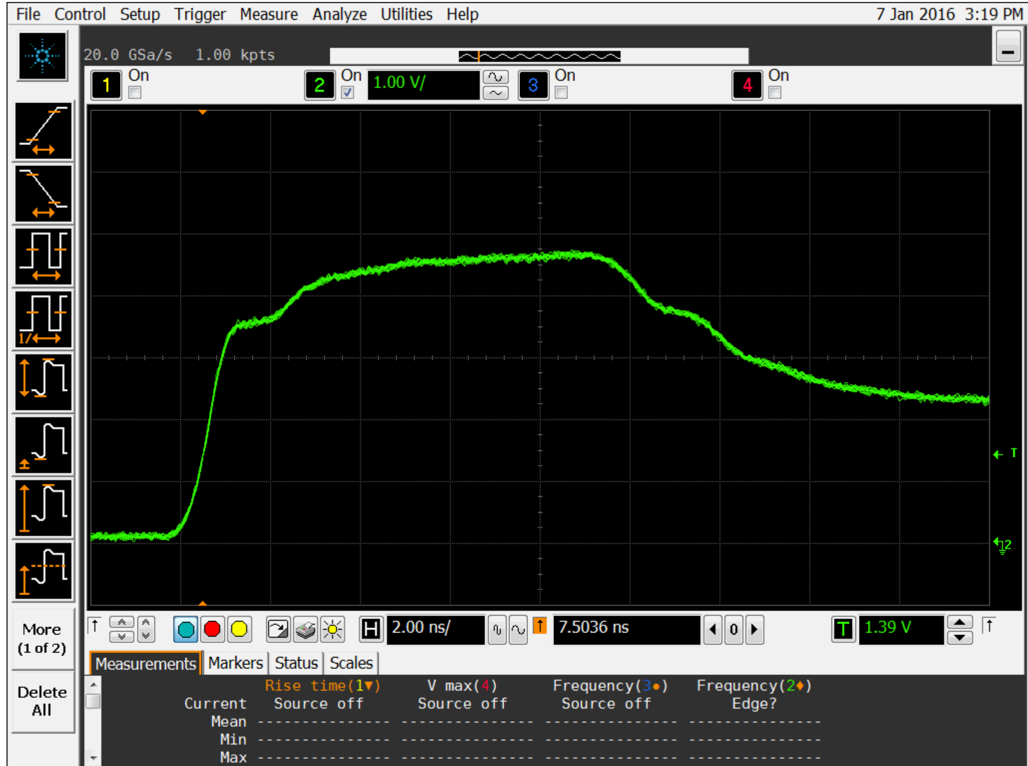

Figure 13a DUT 9433 Pre-Irradiation Rising Edge

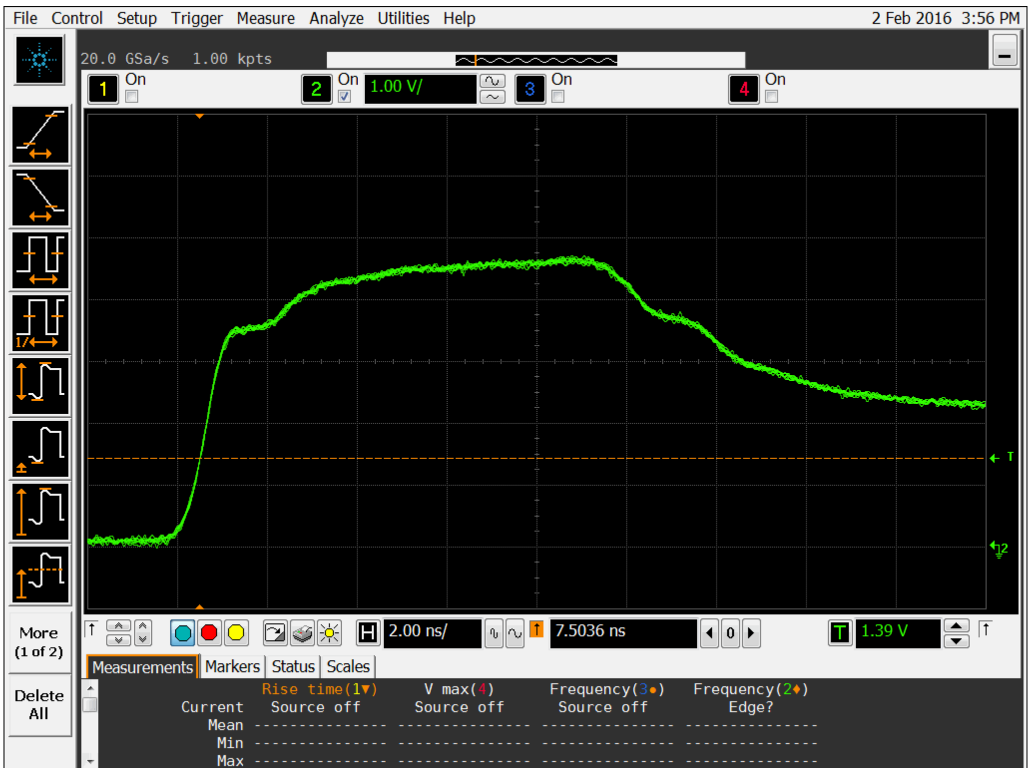

Figure 13b DUT 9433 Post-Annealing Rising Edge

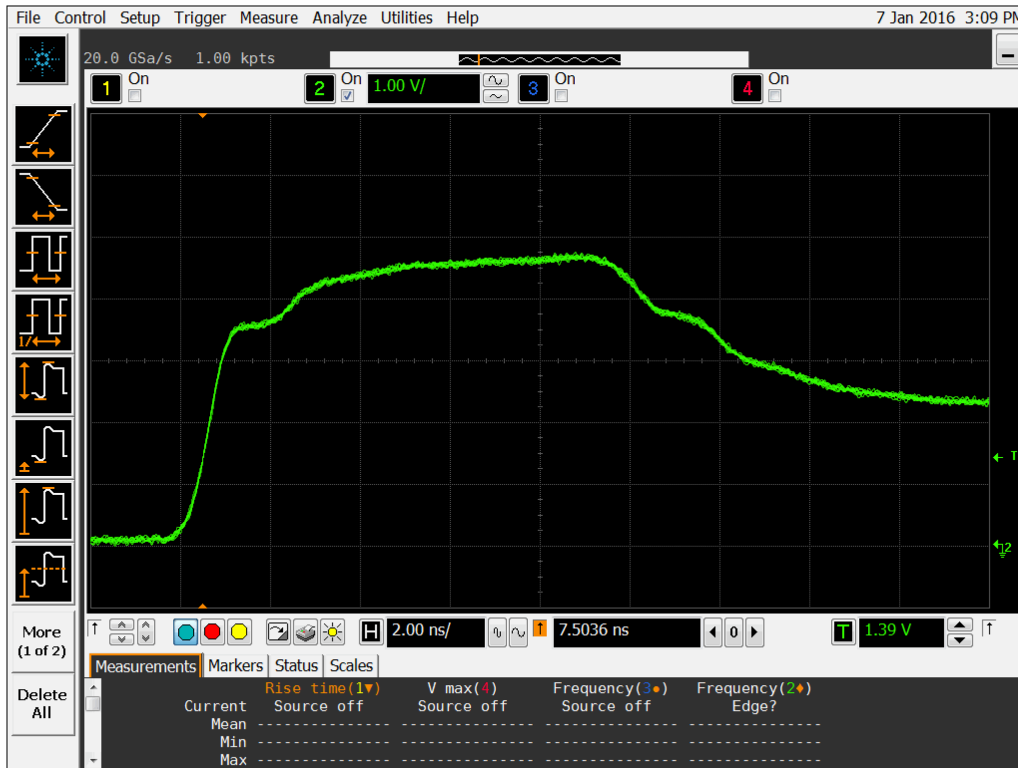

Figure 14a DUT 9434 Pre-Irradiation Falling Edge

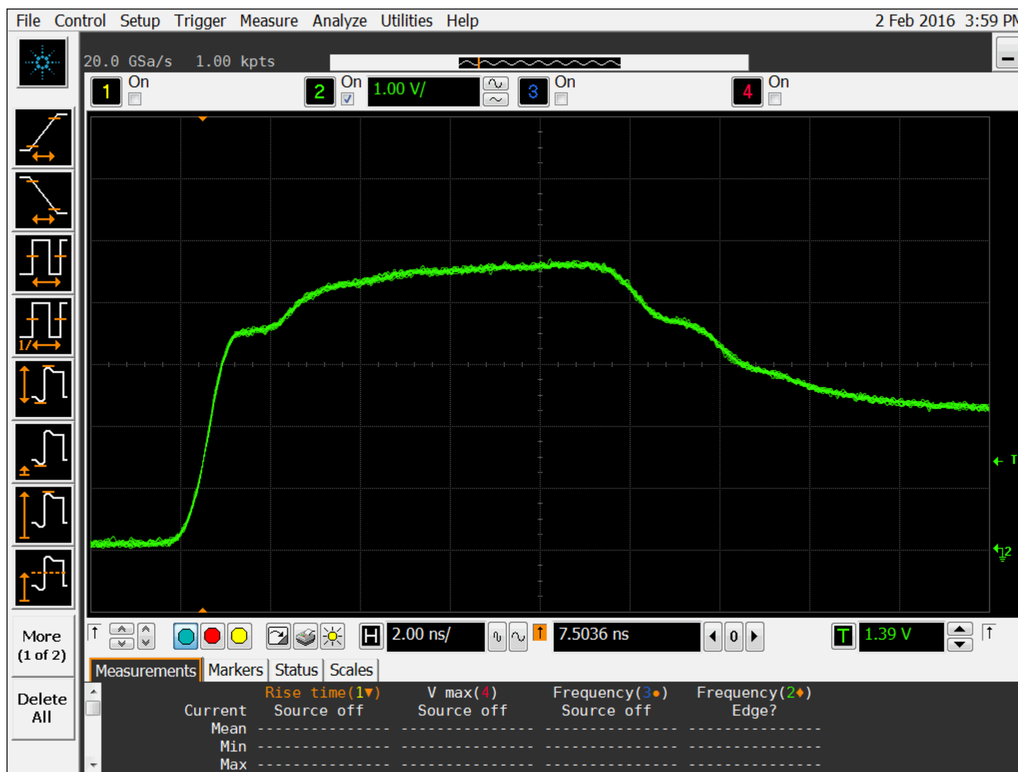

Figure 14b DUT 9434 Post-Annealing Falling Edge

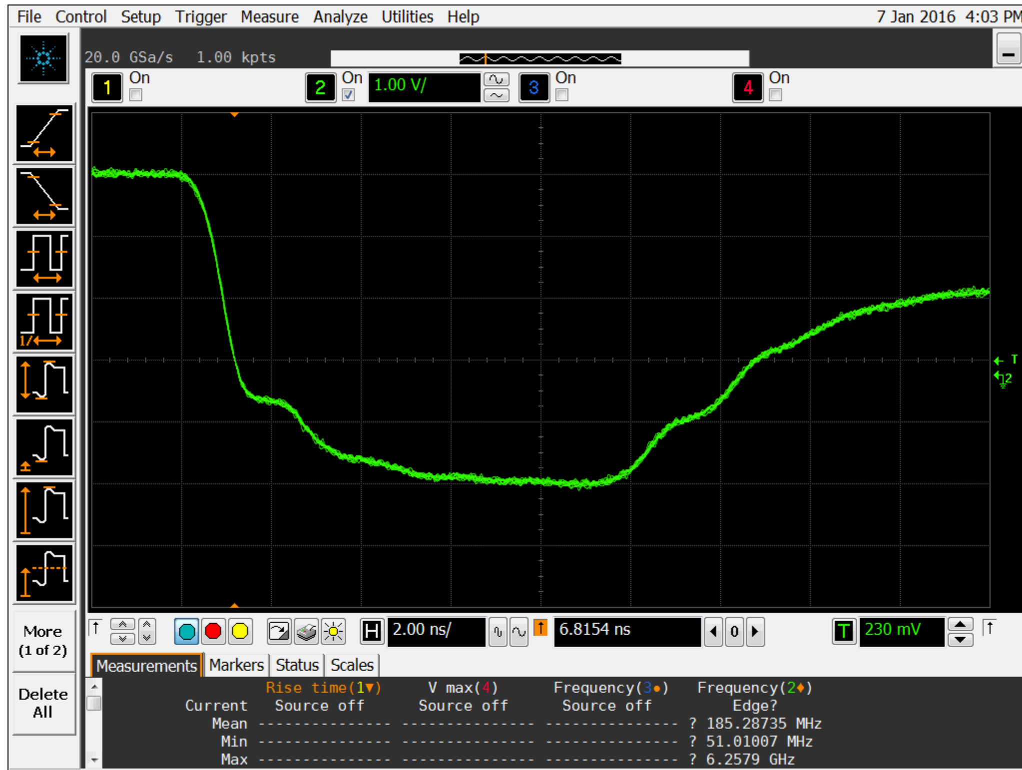

Figure 15a DUT 9392 Pre-Irradiation Falling Edge

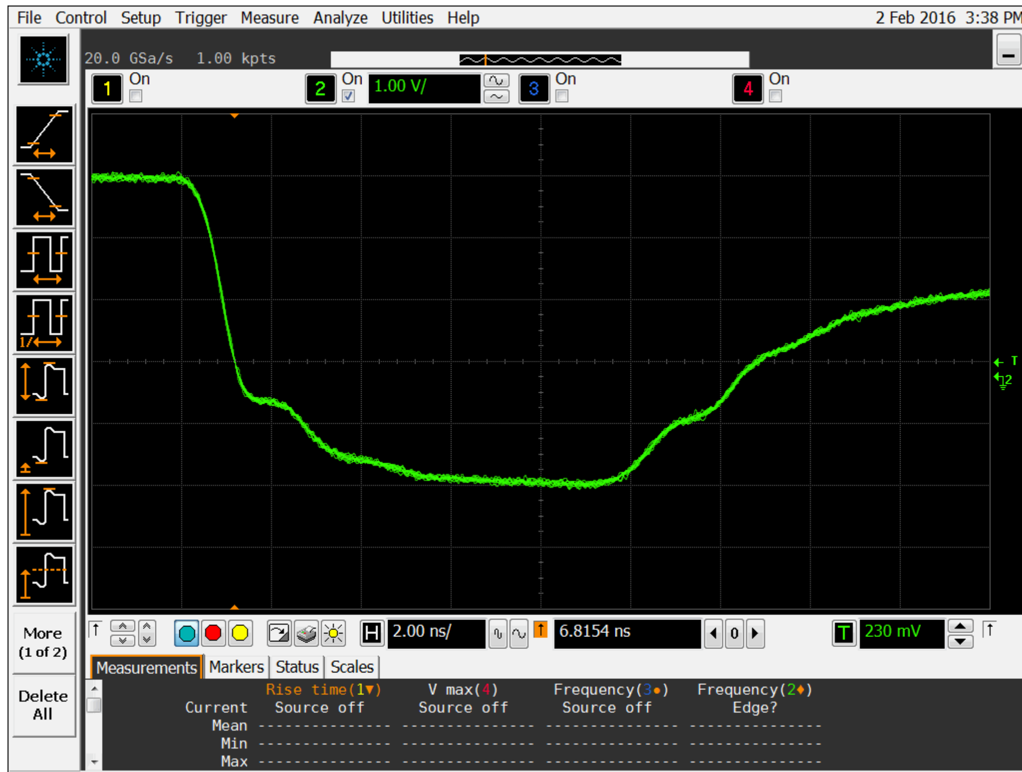

Figure 15b DUT 9392 Post-Annealing Falling Edge

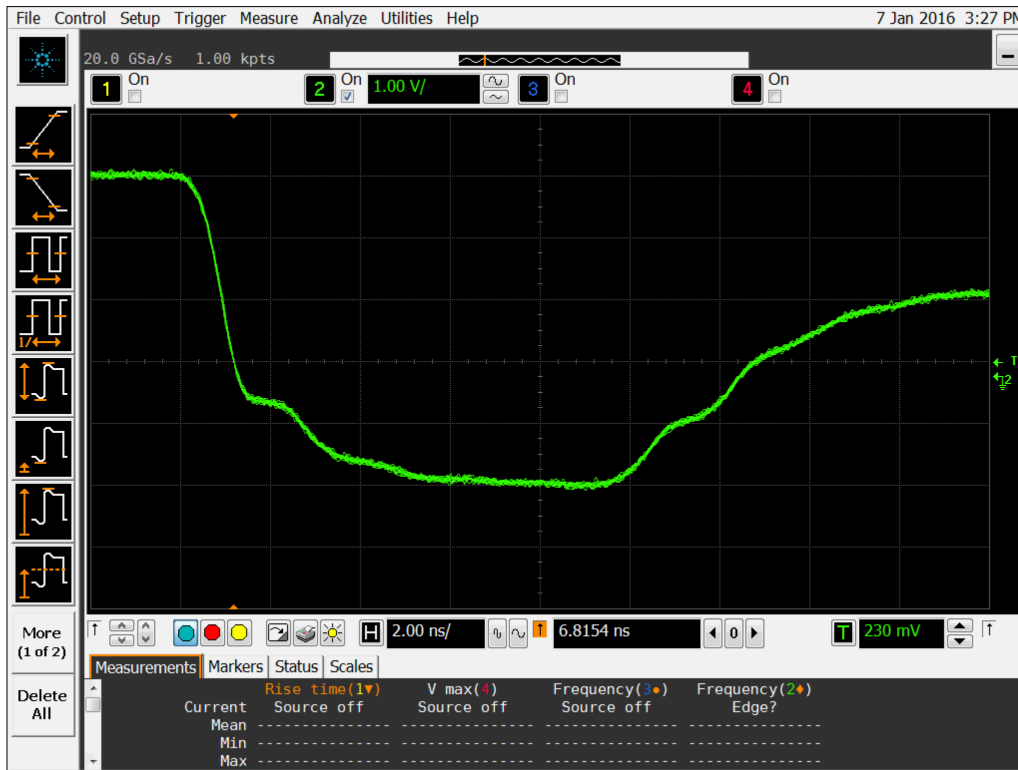

Figure 16a DUT 9395 Pre-Irradiation Falling Edge

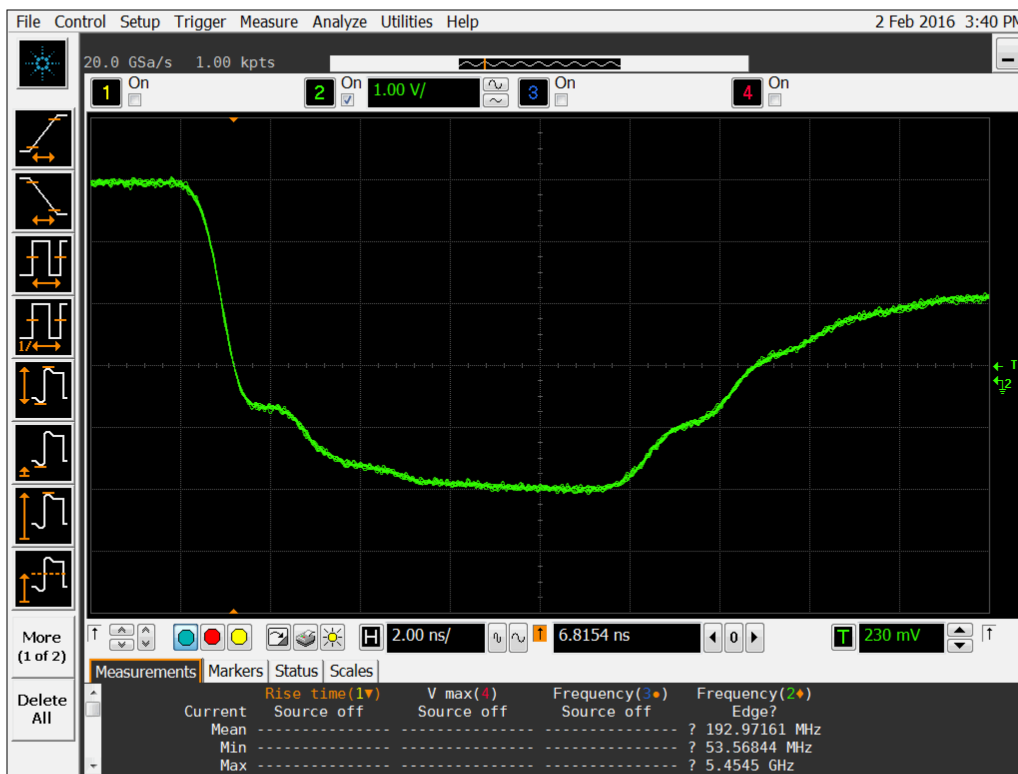

Figure 16b DUT 9395 Post-Annealing Falling Edge

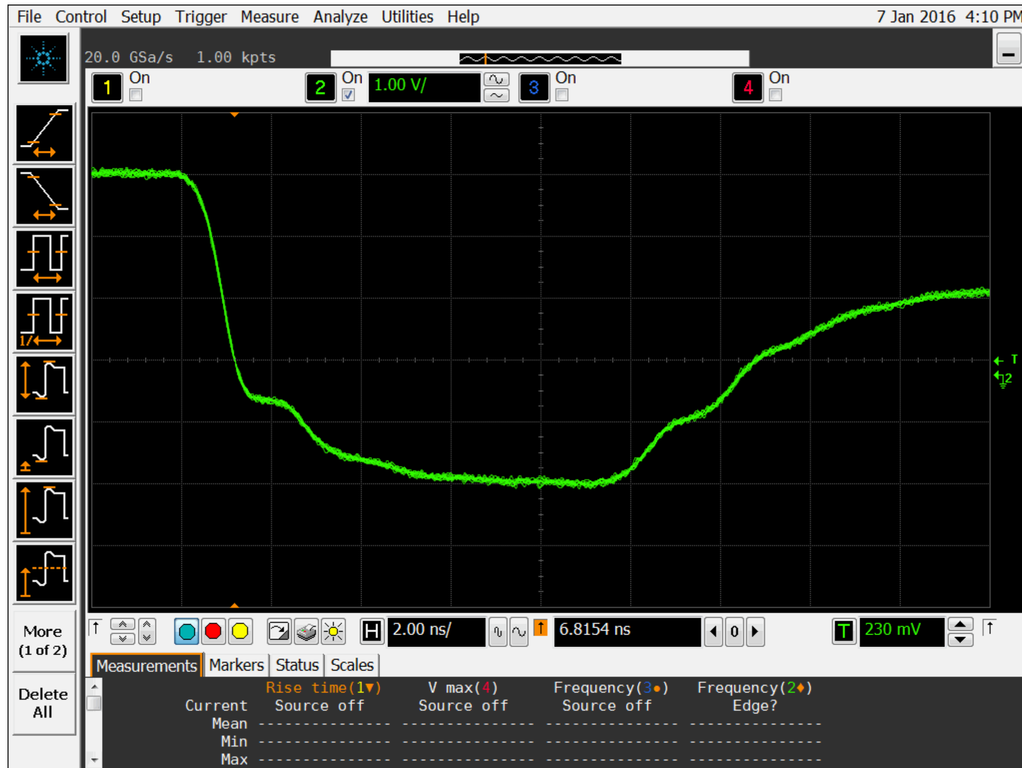

Figure 17a DUT 9410 Pre-Irradiation Falling Edge

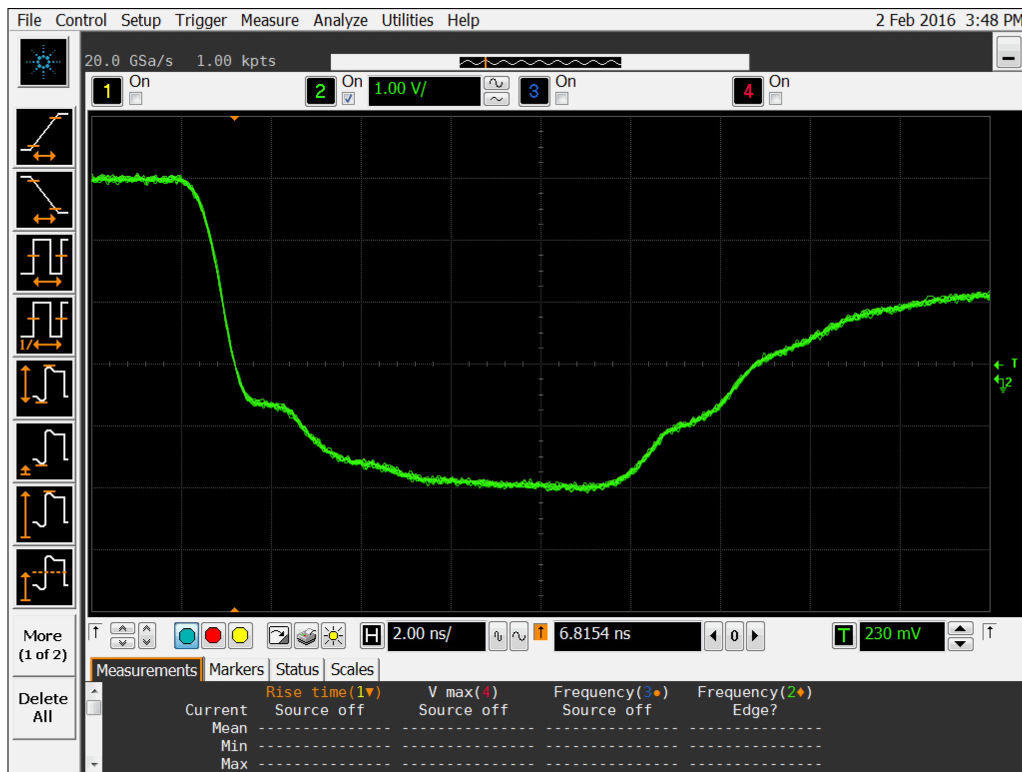

Figure 17b DUT 9410 Post-Annealing Falling Edge

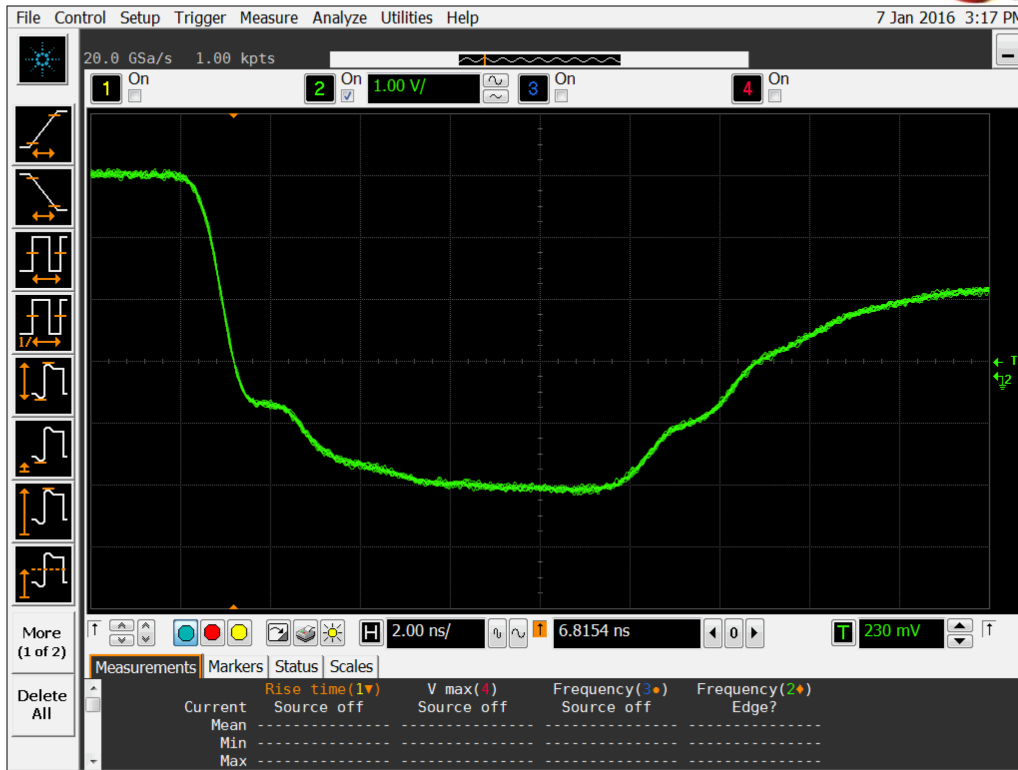

Figure 18a DUT 9428 Pre-Irradiation Falling Edge

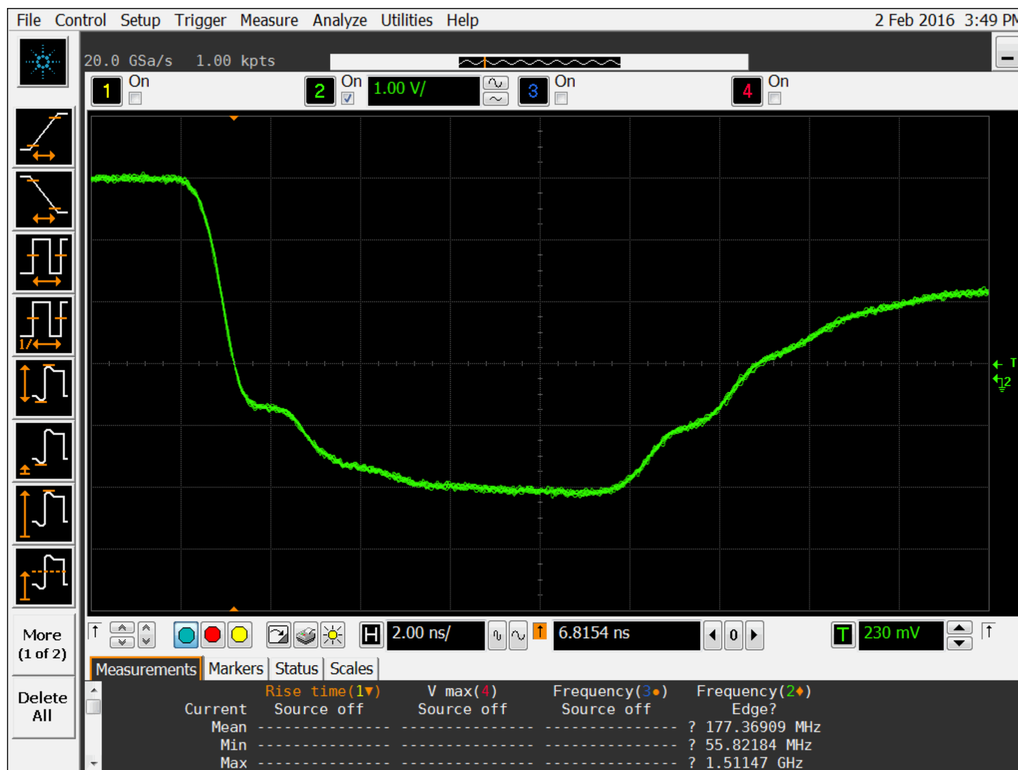

Figure 18b DUT 9428 Post-Annealing Falling Edge

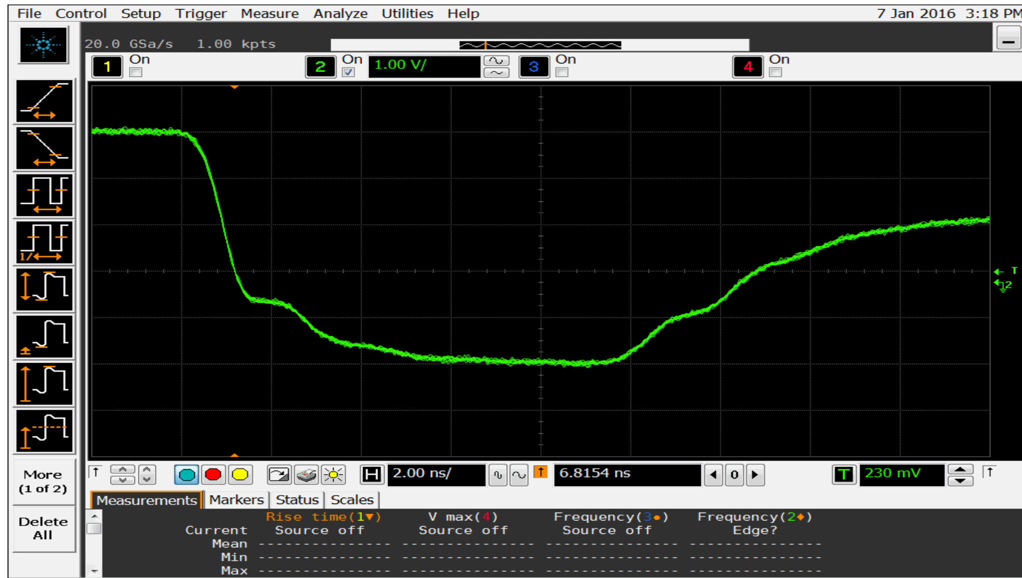

Figure 19a DUT 9433 Pre-Irradiation Falling Edge

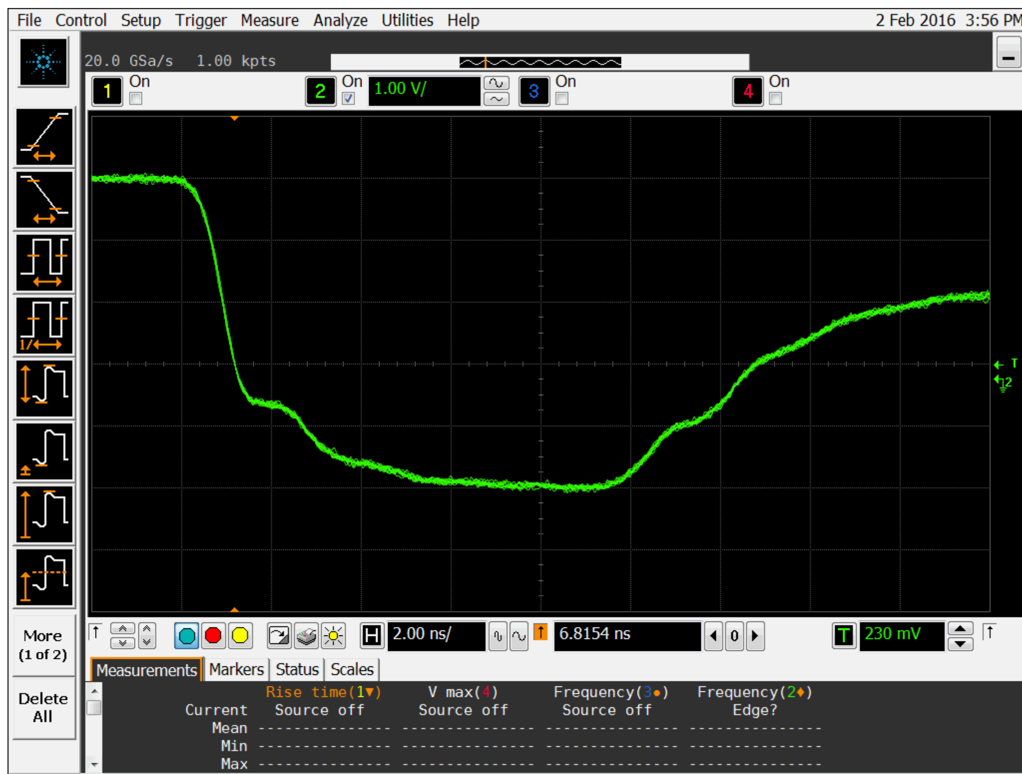

Figure 19b DUT 9433 Post-Annealing Falling Edge

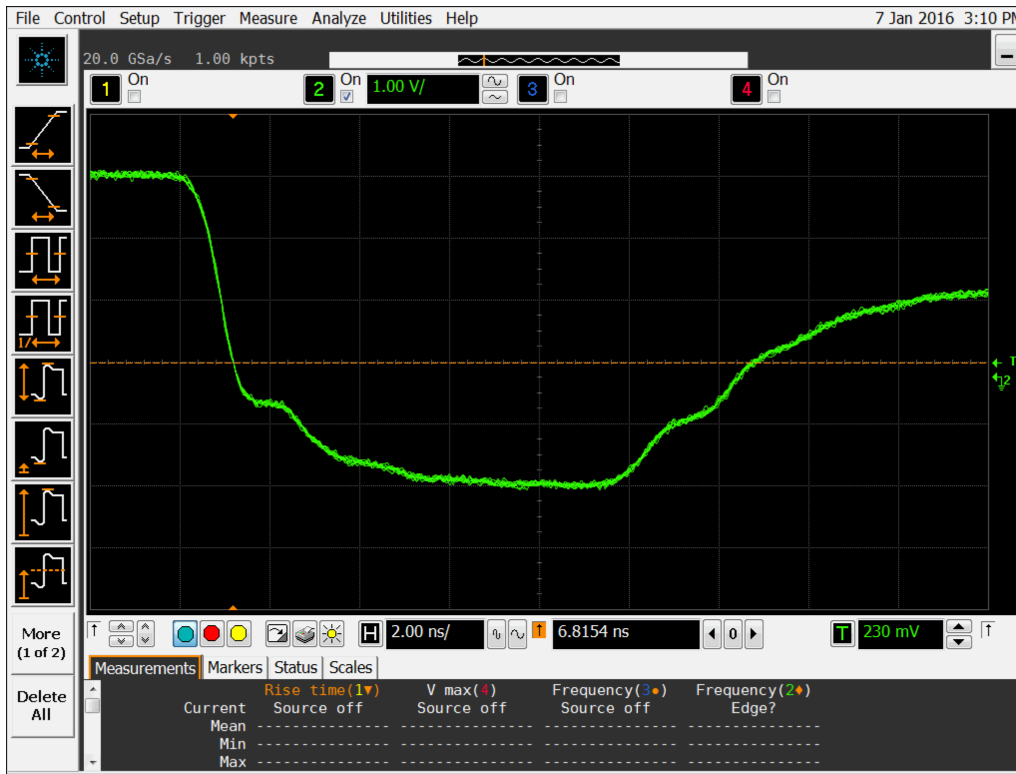

Figure 20a DUT 9434 Pre-Irradiation Falling Edge

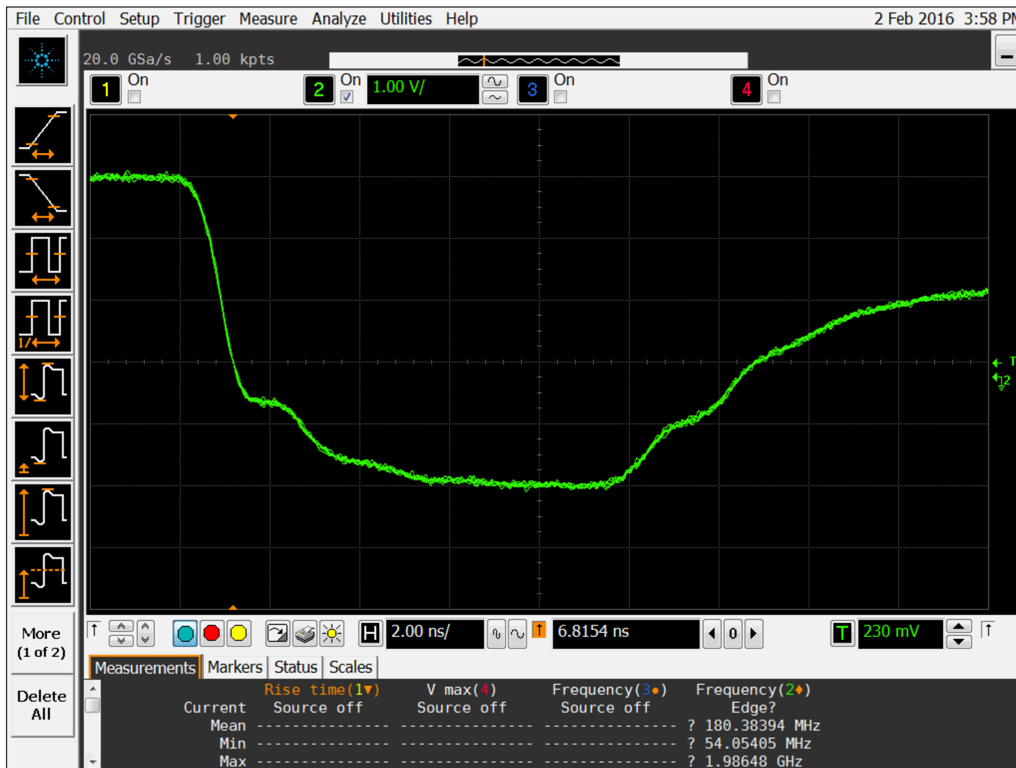

Figure 20b DUT 9434 Post-Annealing Falling Edge

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