LX7157

3A Step-Down Converter

PRODUCTION DATASHEET

DESCRIPTION

LX7157 is a step-down PWM regulator IC with integrated high side P-Ch MOSFET and low side N-CH MOSFET. The 3MHz switching frequency facilates small output filter components.

The operational input voltage range of LX7157 is from 3V to 5.5V. LX7157 uses current mode operation with internal compensation allowing for fast transient response with minimum external components.

LX7157 employs a pulse SKIP method at light load to improve the light load efficiency; as a result, the battery life is extended. The internal soft-start limits the inrush current.

Cycle-by-cycle current limit protects the regulator against over-current conditions. The LX7157 operates in hiccup mode to further enhance the robustness of the converter for heavy over-load or short-circuit fault, and it recovers automatically once the fault is cleared.

The thermal protection shuts down the regulator under an over-temperature condition.

IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

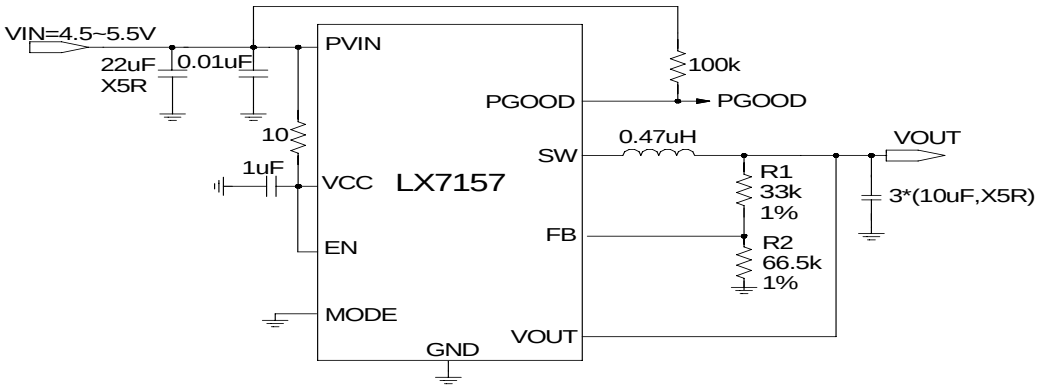
KEY FEATURES

- 3A Step-down Regulator
- Operational Input Supply Voltage Range: 3V-5.5V
- Integrated PMOS and NMOS
- Internal Compensation
- Internal Slope Compensation
- Load Current from zero to 3A
- 3MHz Switching Frequency
- SKIP pulse to improve light load efficiency
- Input UVLO and OV Protection
- Enable
- Power Good
- Internal Soft-start
- Cycle-by-Cycle Over Current Protection
- Hiccup Mode Operation Under OCP
- RoHS Compliant for Pb Free

APPLICATIONS

- Set-Top Box
- LCD TV's
- Notebook/Netbook
- Server and Workstations
- Routers
- Video Cards
- PC Peripherals
- PoE Powered Devices

PRODUCT HIGHLIGHT



PACKAGE ORDER INFO

T_A (°C)		
	LD	**12L MLPD (3.0 x 3.5 mm)**
	RoHS Compliant / Pb-free	
-10 to +85	**LX7157CLD**	

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. LX7157CLD-TR)

THERMAL DATA

θ_{JA} = 46 °C/W

THERMAL RESISTANCE - JUNCTION TO AMBIENT

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow. θ_{JA} number above is with 4-layer PCB board.

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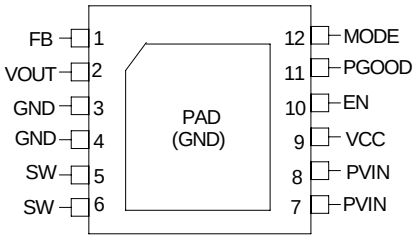
ABSOLUTE MAXIMUM RATINGS

PVIN, VCC, EN, FB, PGOOD, VOUT, MODE..... -0.3V to 7V
SW..... -0.3V to 7V
SW (Shorter than 50ns) ..... -2V to 7V
Maximum Operating Junction Temperature ..... 0°C to 150°C
Storage Temperature Range.....-65°C to 150°C
ESD Protection at all I/O Pins..... ±2kV HBM[1]
Peak Package Solder Reflow Temp. (40 seconds maximum exposure)..... 260°C (+0,-5)

Notes: Exceeding these ratings could cause damage to the device. All voltages are with respect to GND. Currents are positive into, negative out of specified terminal. [1] PVIN & SW pins are ESD sensitive.

PACKAGE PIN OUT



LD PACKAGE

(Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature of $0°C \leq T_A \leq 85°C$ except where otherwise noted with the following test conditions: VCC=PVIN=5V. Typical parameter refers to T_J=25°C

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Recommended Operating Range						
VCC, PVIN (Note 1)			3		5.5	V
Operating Current						
Input Current	I_Q	I_{LOAD}=0, MODE=GND		1.9		mA
Input Current at Shut Down	I_{IN}	EN=GND		0.1	3	µA
VCC Input UVLO						
Under Voltage Lockout	VCC	VCC rising		2.38	2.93	V
UVLO Hysteresis				80		mV
Feedback						
Feedback Voltage Internal Reference	V_{REF}	T_A = 25°C	0.792	0.800	0.808	V
		Temperature range	0.788		0.812	V
FB Pin Input Current	I_{FB}				100	nA
Line Regulation		V_{IN} from 3V to 5.5V, I_{OUT} = 1.5A		0.50		%/V
Load Regulation		I_{LOAD} = 0 to 3A		-0.30		%/A
Output Device						
R_{DSON} of High Side	R_{DSON_H}			60		mohm
R_{DSON} of Low Side	R_{DSON_L}			40		mohm
Current Limit	I_L			5.3		A
Thermal Shut Down Threshold	T_{SH}			150		°C
Hysteresis	T_H			20		°C
PVIN OVP						

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ELECTRICAL CHARACTERISTICS

Unless otherwise specified, the following specifications apply over the operating ambient temperature of 0°C ≤ T_A ≤ 85°C except where otherwise noted with the following test conditions: VCC=PVIN=5V. Typical parameter refers to T_J=25°C

Parameters	Symbol	Test Conditions/Comments	Min	Typ	Max	Units
Rising Threshold	OVP_R			6.5		V
Falling Threshold	OVP_F		5.5	6.1		V
FB UVLO						
FB UVLO Threshold	V_{FBULVO}			70%		V_{REF}
Oscillator Frequency						
PWM Switching Frequency Range	f		2.7	3	3.3	MHz
Switching Frequency at Fold back	f_{FB}	FB<0.3V		0.75		MHz
Soft Start						
Soft Start Time	T_{SS}	From EN high to V_{OUT} reach regulation.	280	340	420	µs
Hiccup Time	T_{HICCUP}	FB=0.2V		11		ms
Mode						
Input High	M_{VIH}		2			V
Input Low	M_{VIL}				0.4	V
EN Input						
Input High	EN_{VIH}		2			V
Input Low	EN_{VIL}				0.4	V
Hysteresis	EN_H			0.1		V
Input Bias	EN_{II}			0.01	1	µA
Power-Good						
Power-good High Threshold	V_{PG}	V_{FB} rising, In percentage of output voltage set-point		89		%
Power-good Low Threshold	V_{PGHY}	V_{FB} falling		83	86	%
Power-good Filter				6		Clock-cycles
Power-good Internal FET Rdson	PG_{RDSON}	VCC=5V		18		ohm
PGOOD FET Leakage Current				0.01	1	µA

Note 1: Minimum input voltage 3.5V is required in order to have 3A output current.

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FUNCTIONAL PIN DESCRIPTION

Name	Pin #	Description
FB	1	Voltage feedback pin. Connect to the output terminal through a resistor divider network to set the output voltage of the regulator to the desired value. The upper resistor of the divider is part of the closed loop stability and must be selected properly to insure the stability of the regulator. Table 1 shows the proper values of this network for selected output voltages.
VOUT	2	Output sensing PIN, connected to the output voltage. Output Voltage Range is 0.8V to 1.8V.
PGND	3, 4 PAD	Ground
SW	5, 6	Switch-node pin. Connect it to the junction of the inductor.
PVIN	7, 8	Input voltage terminal of the regulator. A minimum of 10uF, X5R type ceramic capacitor must be connected as close as possible from this pin to GND plane to insure proper operation.
VCC	9	Analog input voltage terminal. Connect this pin to VIN with a 10ohm resistor and connect a 1uF ceramic capacitor from VCC to GND.
EN	10	Pull this PIN higher than 2V will enable the CHIP.
PGOOD	11	Power-good pin. This is an open-drain output and should be connected to a voltage rail with an external pull-up resistor. During the power on, this pin switches from Low to HI state when FB voltage reaches above the power good threshold and the internal soft start has finished its operation.
MODE	12	When this PIN is connected to GND, skip mode is enabled to improve the light load efficiency. When this PIN is tied to an external CLOCK signal with 30%~70% duty cycle, the IC will be in synchronous mode and switching frequency is synchronized to the external CLOCK. The Sync frequency is in the range of 1MHz to 2MHz. This pin should not be left open or connected to VCC. For output voltages of 1.2V to 1.8V, synchronization clock can be up to 2MHz. For output voltages between 1V and 1.2V, maximum sync clock is 1.5MHz and below 1V, max sync clock is 1.2MHz.

FUNCTIONAL BLOCK DIAGRAM

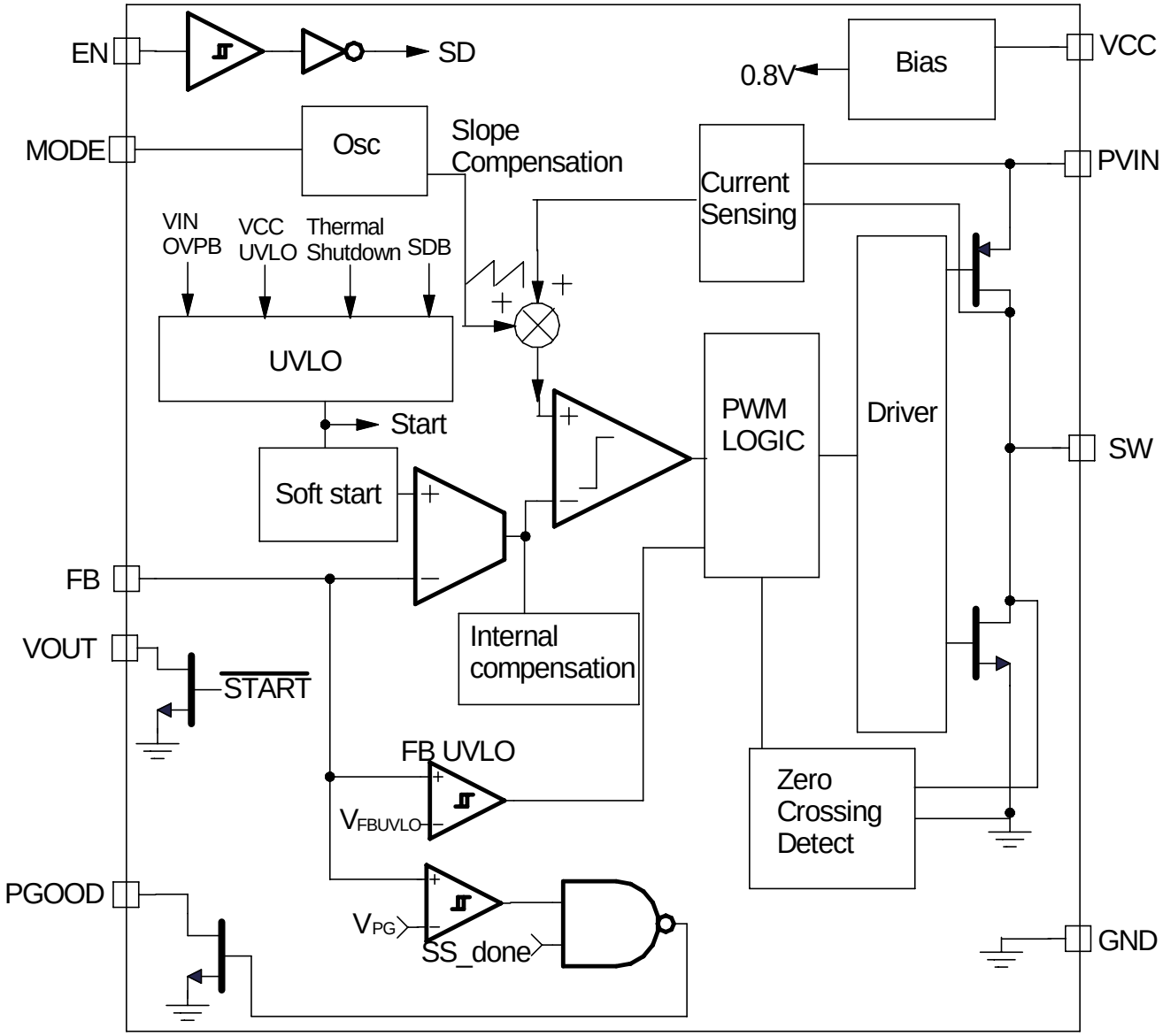

Figure. 1. Functional Block Diagram.

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TYPICAL APPLICATION

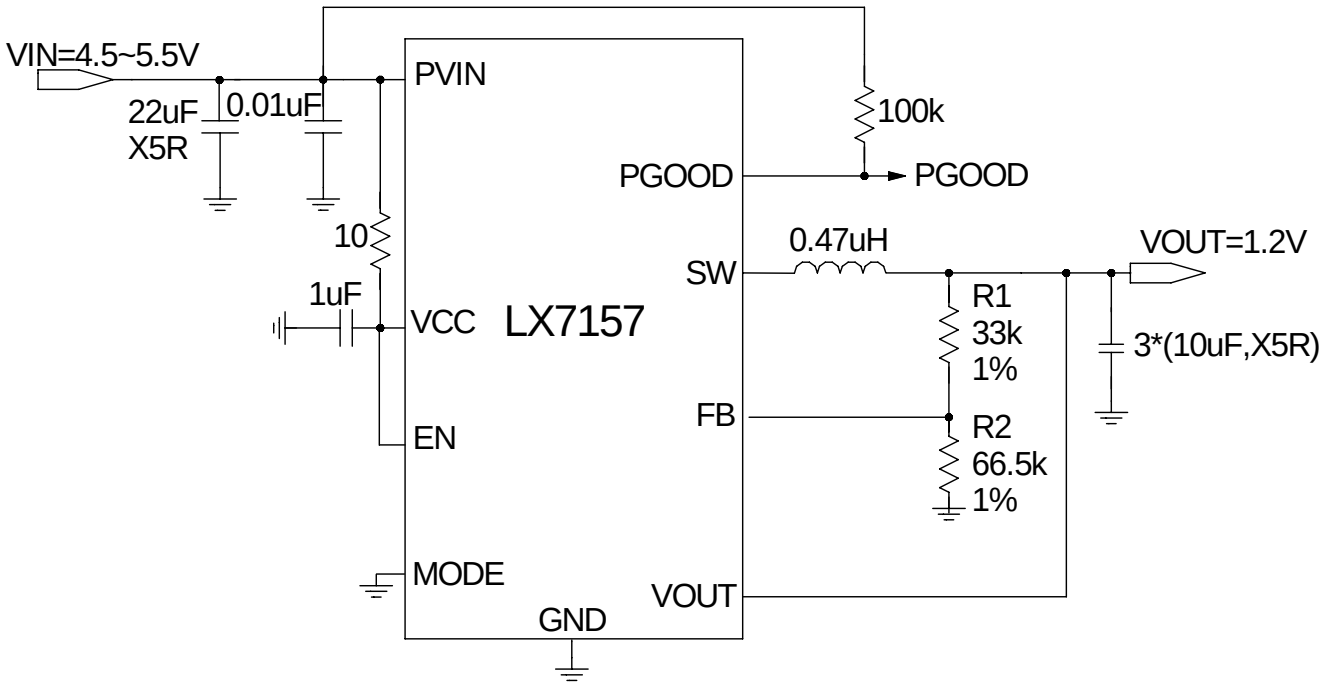

Figure 2. LX7157 with 3 x 10uF output capacitors

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TYPICAL WAVEFORMS @ 25°C (REFER TO FIGURE 2)

Figure 3. DC Operation at 3A

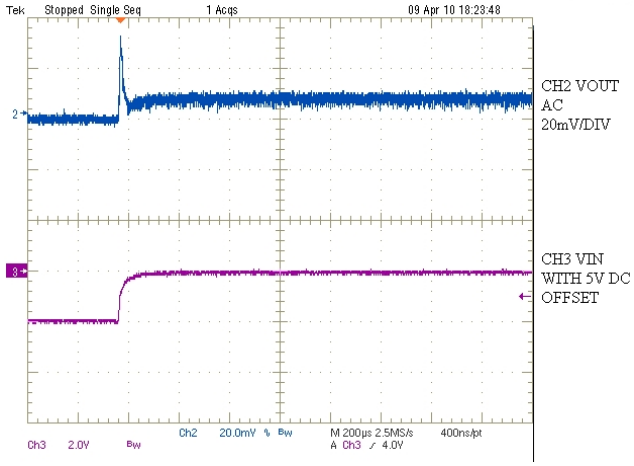

Figure 4. Line transient

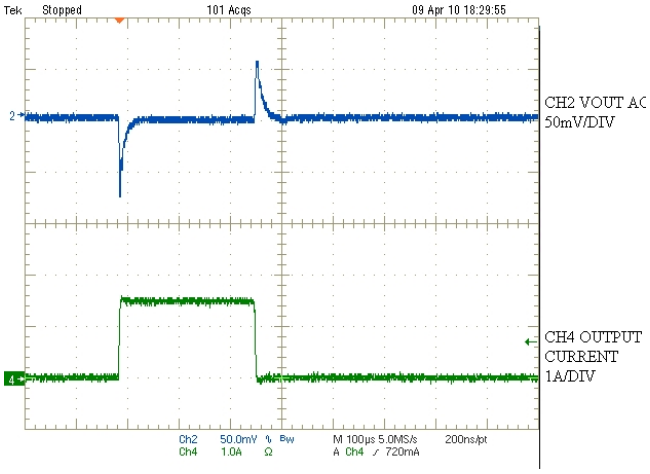

Figure 5. Output load step from 100mA to 1600mA

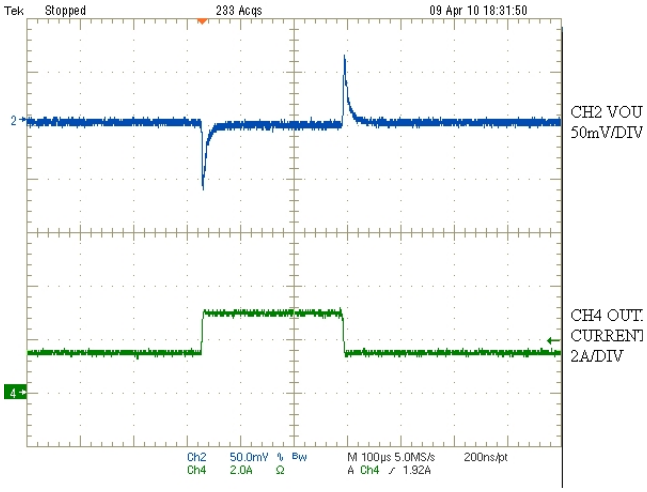

Figure 6. Output load step from 1500mA to 3000mA

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TYPICAL APPLICATION

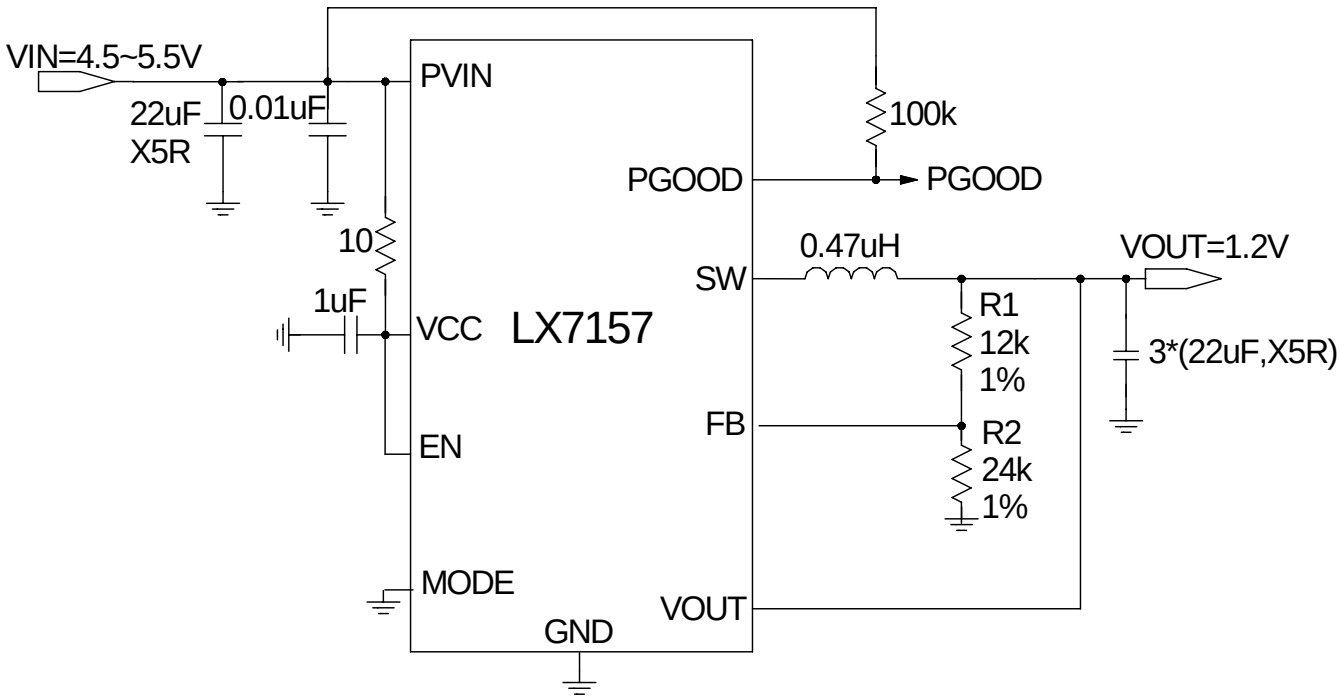

Figure 7. LX7157 with 3 x 22uF output capacitors

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TYPICAL WAVEFORMS @ 25°C (REFER TO FIGURE 7)

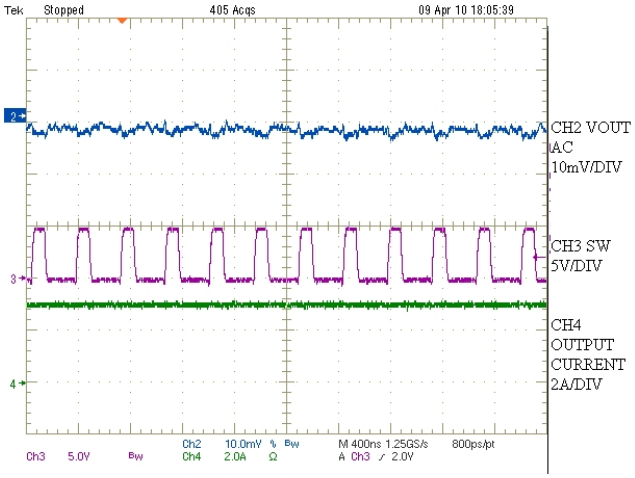

Figure 8. DC Operation at 3A

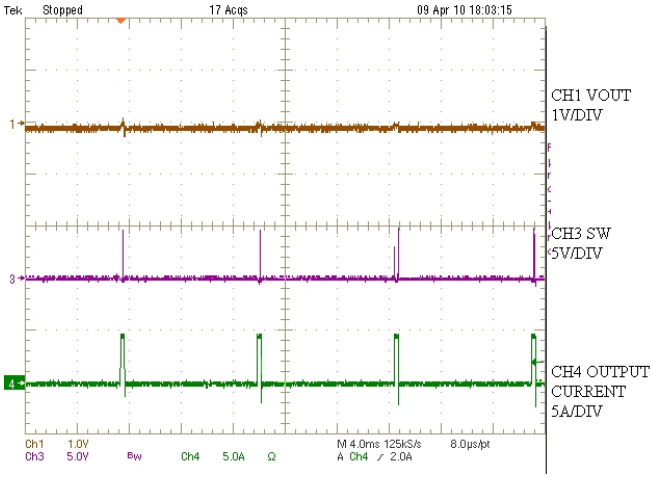

Figure 9. Output Short

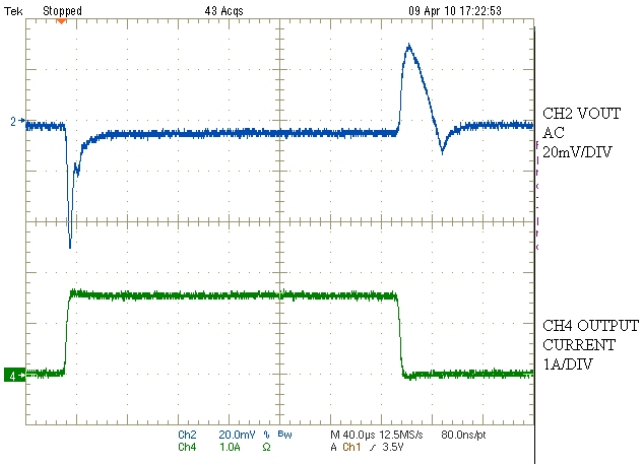

Figure 10. Output load step from 100mA to 1600mA

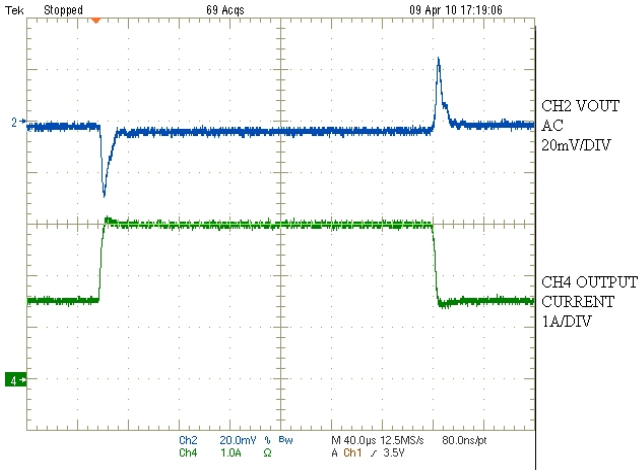

Figure 11. Output load step from 1500mA to 3000mA

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TYPICAL WAVEFORMS @ 25°C (REFER TO FIGURE 3)

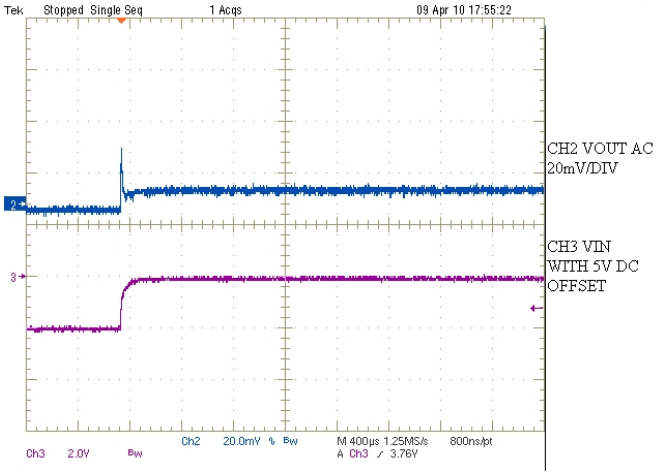

Figure 12. Line transient

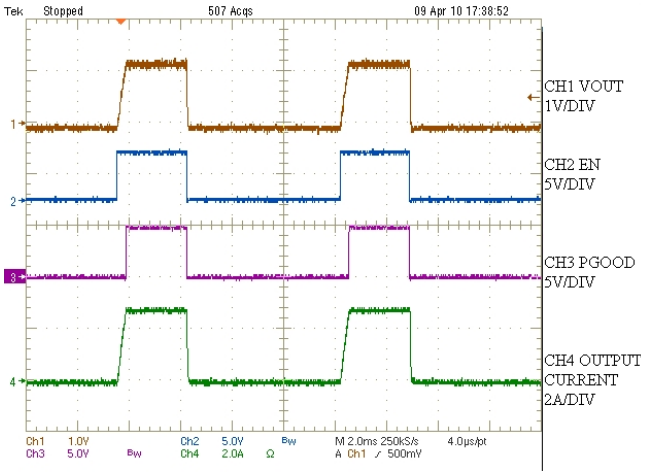

Figure 13. Startup with load

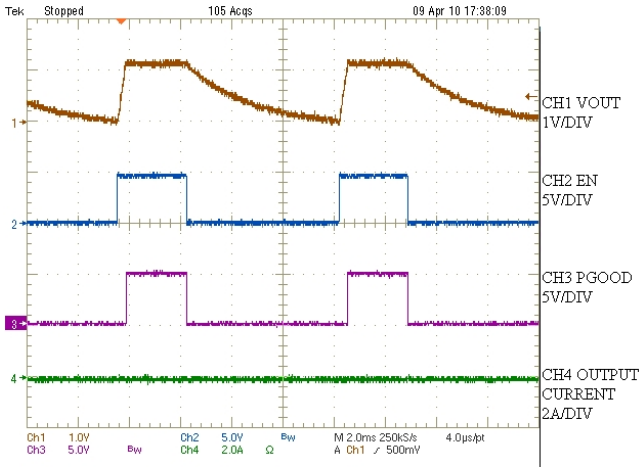

Figure 14. Startup with no load

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APPLICATION INFORMATION

OUTPUT VOLTAGE CALCULATION

Output voltage is set by reference voltage and external voltage divider. The reference voltage is fixed at 0.8V. The divider consists of two ratioed resistors so that the output voltage applied at the FB pin is 0.8V when the output voltage is at the desired value. The following equation and picture show the relationship between output voltage and voltage divider.

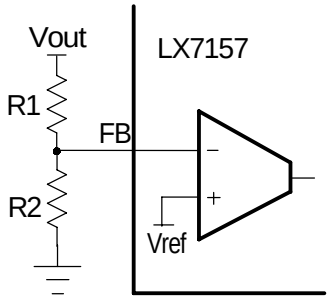

Figure 15 Voltage Divider

$$V_{OUT} = V_{REF} \times (1 + \frac{R_1}{R_2}) \quad \ldots\ldots\ldots\ldots\ldots\ldots\ldots\ldots (1)$$

The value of upper feedback resistor R1 has to be set properly in order to have stable system. The recommended value of R1 is shown in the table 1, R2 can be derived from equation 1.

Table 1. Recommended upper resistor value of feedback resistor divider for typical application (L=0.47uH).

Output Capacitor	R1 (ohm)
2x10uF (X5R,6.3V)	80.6k
3x10uF (X5R,6.3V)	33k
2x22uF (X5R,6.3V)	30k
3x22uF (X5R,6.3V)	12k

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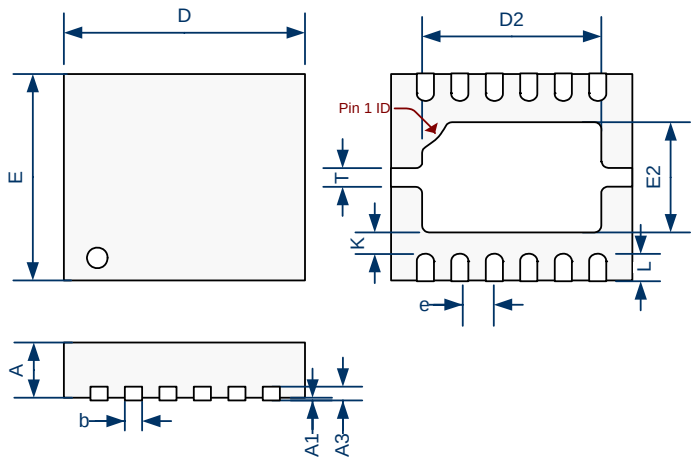
PACKAGE DIMENSIONS

LD 12 Pin Plastic DFN 3.5x3 mm Dual Exposed Pad



Dim	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.70	0.80	0.027	0.031
A1	0	0.05	0	0.002
A3	0.20 REF		0.008 REF	
b	0.18	0.30	0.007	0.012
D	3.50 BSC		0.138 BSC	
D2	2.45	2.70	0.096	0.106
e	0.50 BSC		0.019 BSC	
E	3.00 BSC		0.118 BSC	
E2	1.45	1.70	0.057	0.067
L	0.35	0.55	0.014	0.022
T	0.20	0.30	0.008	0.012

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