Device Selection and Optimizing of Half Bridge RF Generators

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The following Application Note is a SPICE Model tutorial on Half Bridge Topologies and device selection. We will also discuss their relative performance with matched and reactive loads. This tutorial is based on new Large Signal RF Spice Models developed at Microsemi PPG. The circuits include all significant strays at appropriate values. This format allows us to explore operational elements that are exceedingly difficult, if not impossible, to measure accurately even in a laboratory environment. In addition, it provides a valuable tool for the understanding of circuit operation under varying load conditions and device type.

N Channel – N Channel Half Bridge

The Half Bridge Topology is used for this Device Characterization. Figure 1 illustrates the classical N Channel - N Channel Half Bridge RF Generator. The High Side Switch X2 and the Low Side Switch X1 form the two active devices in the Half Bridge. X1 and X2 commutate in an alternating fashion providing a pseudo Square Wave drive to the input of the RF Network, at V5. The RF network provides an impedance match from the Drain Impedance of X1, X2 of Figure 1. The match is 3Ω to the 50Ω load. During the evaluation, different devices will be examined. This will necessitate changes in the network in order to provide an appropriate drain load match. This L Match network is resonant at the frequency of the device evaluation.

This resonant network only performs the impedance translation at the design frequency. The common design formulas account only for a resistive source and load. Since the output devices have parasitic capacitance, after the network is designed, the series value of L4 may be adjusted to account for this capacitance. A value of L4 ≈ 0% to 25% higher than the calculated value is sometimes required to bring the network to peak efficiency.

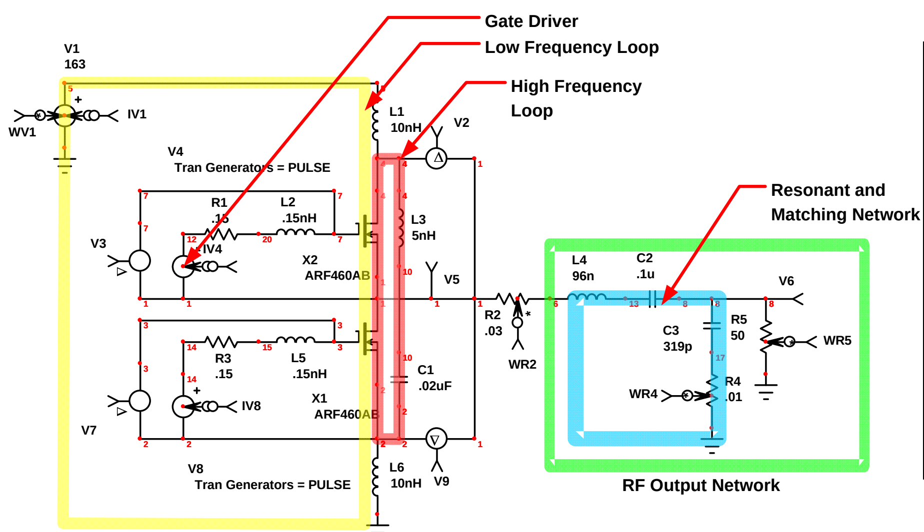

Table 1

Circuit Performance	
Vsupply	+197V
Pout	2036W
Pin	2351W
PLoss	315W
Eff	86.6%
Pulse Gate Drive	PW=27ns
Ths	45°C
Tj X2	100°C
TjX1	100°C
Drain Z=3Ω	Out Z=50Ω

Figure 1. N - N Channel Half Bridge

Figure 1 illustrates an N-N Channel Half Bridge circuit Topology. The circuit contains two current loops. A low frequency loop is highlighted in yellow. The High Frequency Loop is highlighted in red. These loops are illustrated with near-minimum stray inductance. Great care should be taken to achieve inductance values near the illustrated values of Figure 1. If we allow L2 to reach 100nH or greater, performance will be severely degraded. The inductance of the Inner Loop, L3, is an extremely Critical Stray Component. Values greater than a few nH can cause stability problems and excessive harmonics.

Given the preceding Half-Bridge Design discussion, we have evaluated several ARF devices in this topology using a Spice circuit simulation based or our new device models, and correlated the performances with previous bench work by the author. Circuit Parameters have been adjusted for the Highest Efficiency and Highest Power Output while limiting the MOSFETs junction temperature to a maximum of ≈ 100°C and limiting the Drain to Voltage to $\mathbf{V_{DS}}$ Maximum. We have set the heat sink temperature at 45°C.

Figure 2 shows the resulting output of the simulations from 2MHz to 40MHz for each of the devices that were selected for this Application Note.

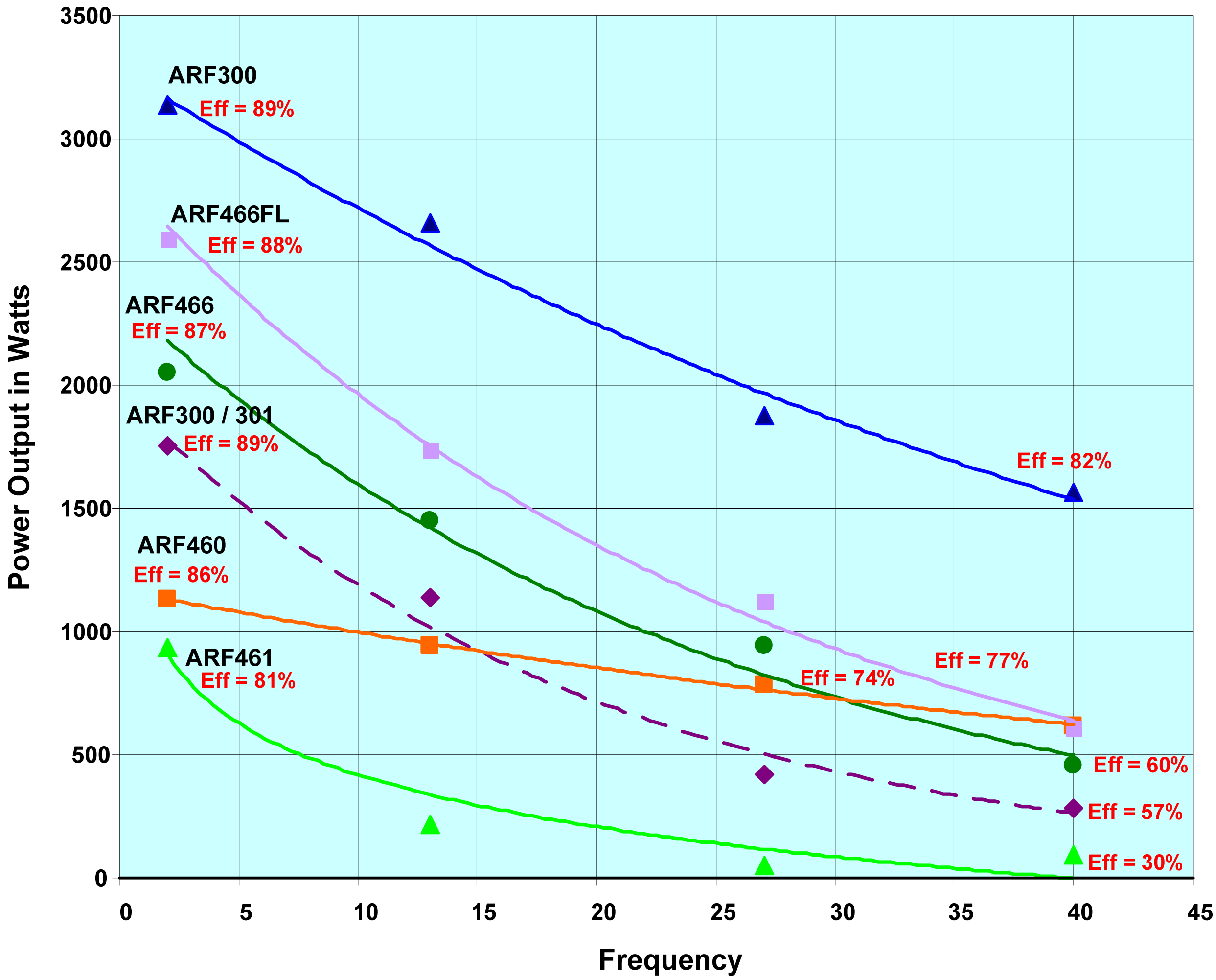

Figure 2. RF Output Power vs. Frequency

In Figure 2 we see that the device with the dashed line plot seems very different than the other four devices. The ARF300-ARF301 Half Bridge is limited in power by the characteristics of the P Channel device, the ARF301. The proper drain load for the ARF301 is about 8Ω, for the ARF300 it is about 3Ω. The ARF300 is the device with the lowest $\mathbf{R_{DS(on)}}$ the ARF461 is the highest at 2Ω. The advantage of the ARF301 is the simplified drive circuit in Half Bridge configurations, see *Note 1*.

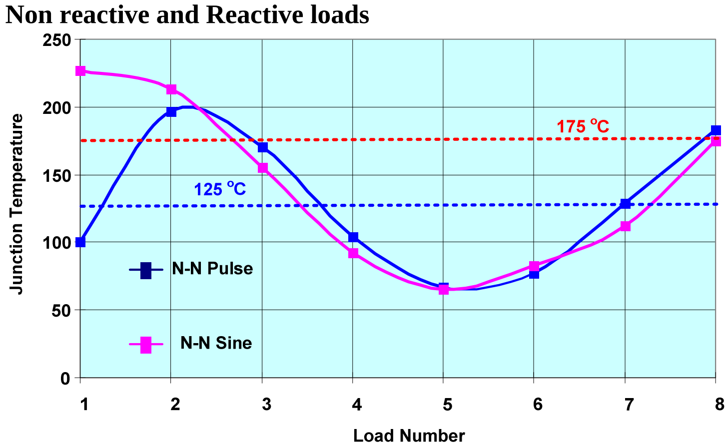

Figure 3. Loads vs. Configuration, N-N Sine, see *Note 1*.

Table 2
Data for Figure 3

Load Number	Rs	Xs	Reactive Load
Base Line	50	0	jXs
1	100	0	0
2	69.5	431nH	36.7
3	40	352.6nH	30
4	28.1	174.5nH	14.9
5	25	0	0
6	28.1	709pF	-14.9
7	40	390pF	-30
8	69.5	317pF	-36.7

Each of the loads illustrated in Figure 3 and the inset Table 2, present a 2:1 VSWR mismatch to 50Ω. They are equally spaced every 45° around a 2:1 VSWR load circle. In the circuit of Figure 1, the 50Ω load is transformed by the output matching network (L5+L6 and C2) to approximately 3Ω at the Drains of transistors X1 and X2. A load other than 50Ω is "mismatched" and its effect on the circuit is quite different. From a reliability standpoint, keeping the load between 3-4 on the left and at or below 7 on the right is the preferred operating space. In addition, minimizing the time spent at or above 175°C is advisable.

An output load impedance lower than 50Ω will be transformed to a higher impedance load at the devices. The transistors can more easily supply the full output voltage to this higher impedance. Consequently, the output power is less and the junction temperature is lower. Load impedance greater than 50Ω on the output is transformed though the matching network to an impedance lower than 3Ω at the transistor junction. This causes the devices to be overloaded and mistuned. This puts the full voltage on this lower impedance, creating more output power at lower efficiency, which in turn causes the rise in junction temperature. Figure 3 clearly demonstrates the importance of maintaining a proper load on the output of the RF Generator. The addition of a fast protection circuit to limit power dissipation is well advised.

Conclusion

In the preceding we have focused on Optimizing Power Output for Half Bridge RF Generators, using ARF devices and operating from 2MHz to 40MHz. For Class-D operation, the power losses in the switching devices are comprised of two loss terms. These are the Switching Loss and the Conduction Loss. In Figure 2 we see that as we lower the $\mathbf{R_{DS(on)}}$, the power output and the efficiency are increased. This indicates that the Conduction Loss is dominating across the 2MHz to 40MHz band for the devices evaluated. Figure 3 teaches us that we will damage devices with excessive power dissipation not overvoltage.

Note 1. For a detailed discussion of N-N Pulse vs. N-N Sine drive, please see ARF300 – ARF301 In N-N and N-P Half Bridge RF Generators with Pulse and Sine Drive, Microsemi Application Note 1808.