SG3561A

POWER FACTOR CONTROLLER

DATA SHEET

DESCRIPTION

This monolithic integrated circuit provides all the necessary functions for designing an active power factor correction circuit in conjunction with off-line power converters. Although the IC is optimized for electronic ballast applications, it can also be used in switched mode AC-DC power converters. Included in the 8-pin DIP package are; an under voltage lockout with a micropower start-up with a 2V hysteresis, an internal temperature compensated bandgap reference, a unity gain stable error amplifier, one quadrant multiplier stage, a current sense comparator and a totem pole output stage for directing driving of the power MOSFET. In addition to the above, an internal logic circuit detects the zero crossing of the inductor current and maintains discontinuous current mode of operation such that it allows no current gaps to appear. This type of operation provides a higher P.F. correction, as well as lower harmonic distortion over the fixed frequency discontinuous current mode. The SG3561A is characterized for operation over the ambient temperature range of -25°C to +85°C.

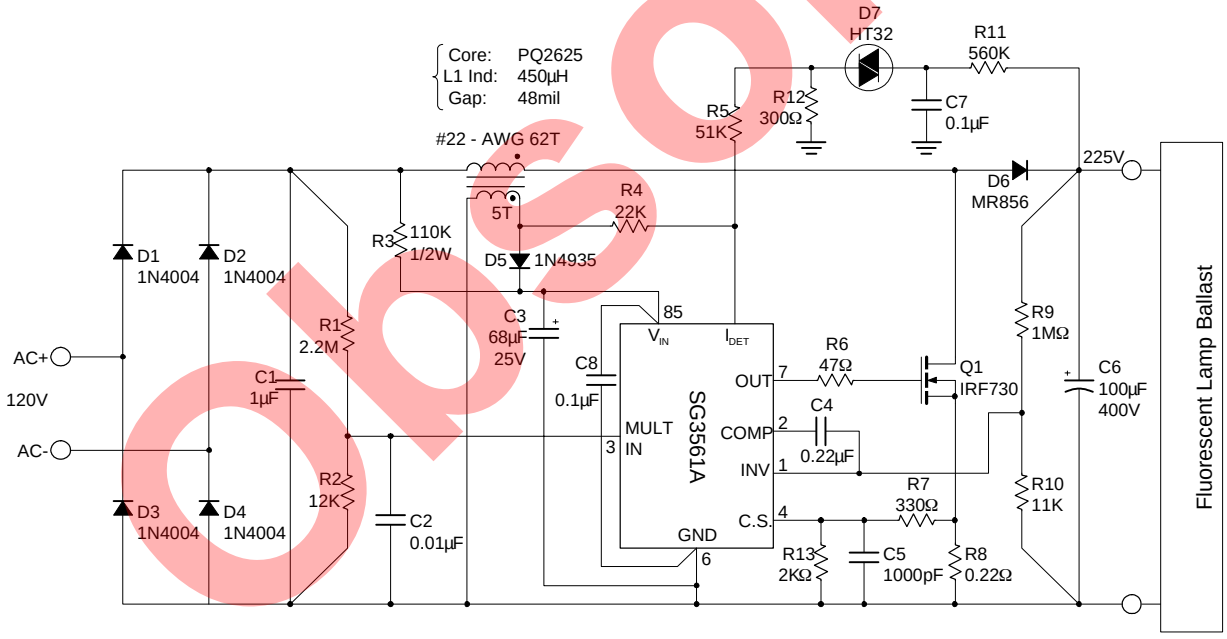
IMPORTANT: For the most current data, consult *MICROSEMI*'s website: **http://www.microsemi.com**

KEY FEATURES

- MICRO-POWER START-UP MODE (250µA typ.)
- LOW OPERATING CURRENT CONSUMPTION
- INTERNAL 1.5% REFERENCE
- TOTEM POLE OUTPUT STAGE
- AUTOMATIC CURRENT LIMITING OF BOOST STAGE
- DISCONTINUOUS MODE OF OPERATION WITH NO CURRENT GAPS
- NO SLOPE COMPENSATION REQUIRED
- AVAILABLE IN 8 & 14-PIN PLASTIC DIP AND 8-PIN SOIC PACKAGE
- SEE LX1562/1563 FOR NEW DESIGNS

PRODUCT HIGHLIGHT

TYPICAL APPLICATION OF THE SG3561A IN AN 80W FLUORESCENT LAMP BALLAST WITH ACTIVE POWER FACTOR CONTROL



PACKAGE ORDER INFO

T_A (°C)	M Plastic DIP 8-Pin	N Plastic DIP 14-Pin	DM Plastic SOIC 8-Pin
	RoHS Compliant / Pb-free Transition DC: 0503		RoHS Compliant / Pb-free Transition DC: 0440
-25 to 85	SG3561AM	SG3561AN	SG3561ADM

Note: Available in Tape & Reel. Append the letters "TR" to the part number. (i.e. SG3561AM-TR)

Rev. 1.2a,2005-03-09

LINFINITY MICROELECTRONICS INC.
11861 WESTERN AVENUE, GARDEN GROVE, CA. 92841, 714-898-8121, FAX: 714-893-2570

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (V_{IN}) ..... -0.3V to 28V
Peak Driver Output Current ..... ±500mA
Driver Output Clamping Diodes
$V_Q > V_{CC}$ or $V_Q < -0.3V$ ..... ±10mA
Detector Clamping Diodes
$V_{DET} > 6V$ or $V_{DET} < 0.9V$ ..... ±10mA
Error Amp, Multiplier, and Comparator Input Voltages ..... -0.3V to 6V
Detector Input Voltage (Note 2) ..... 0.95 to 6V
Operating Junction Temperature
Plastic (M, N and DM Packages) ..... 150°C
Storage Temperature Range ..... -65°C to 150°C
Peak Package Solder Reflow Temp. (40 seconds max. exposure) ..... 260°C (+0,-5)

Note 1. Values beyond which damage may occur. All voltages are specified with respect to ground, and all currents are positive into the specified terminal.
Note 2. With no limiting resistor.

THERMAL DATA

M PACKAGE:

THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	95°C/W

N PACKAGE:

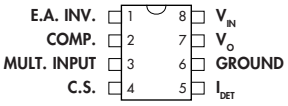
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	65°C/W

DM PACKAGE:

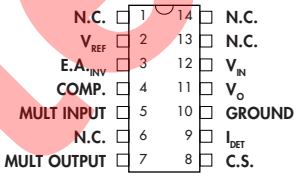
THERMAL RESISTANCE-JUNCTION TO AMBIENT, θ_{JA}	165°C/W

Junction Temperature Calculation: $T_J = T_A + (P_D \times \theta_{JA})$.
The θ_{JA} numbers are guidelines for the thermal performance of the device/pc-board system. All of the above assume no ambient airflow.

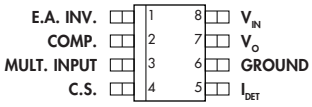
PACKAGE PIN OUTS



M PACKAGE
(Top View)



N PACKAGE
(Top View)



DM PACKAGE
(Top View)

RoHS / Pb-free 100% Matte Tin Lead Finish

RECOMMENDED OPERATING CONDITIONS (Note 3)

Parameter	Symbol	Recommended Operating Conditions			Units
		Min.	Typ.	Max.	
Supply Voltage Range	V_{IN}	11		25	V
Peak Driver Output Current			±300		mA
Operating Ambient Temperature Range:					
SG3561A	T_A	-25		85	°C

Note 3. Range over which the device is functional.

ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, these specifications apply over the operating ambient temperatures for the SG3561A with -25°C ≤ T_A ≤ +85°C; V_{IN}=12V. Low duty cycle pulse testing techniques are used which maintains junction and case temperatures equal to the ambient temperature.)

Parameter	Symbol	Test Conditions	SG3561A			Units
			Min.	Typ.	Max.	
Under-Voltage Lockout Section						
Start Threshold Voltage			9.2	10	10.8	V
UV Lockout Hysteresis			1.6	2.0	2.4	V
Supply Current Section						
Start-Up Supply Current		$V_{IN} < V_{TH}$		0.25	0.5	mA
Operating Supply Current		V_{IN} = 12V, Output Not Switching		6	12	mA
Dynamic Operating Supply Current	AVE	V_{IN} = 12V, 50KHz, CGS = 1000pF		10	15	mA
Reference Section (Note 4)						
Initial Accuracy		I_{REF} = 0mA, T_J = 25°C	2.463	2.50	2.538	V
Line Regulation		12V < V_{IN} < 25V		0.1	10	mV
Load Regulation		0 < I_{REF} < 2mA		0.1	10	mV
Temperature Stability				20		mV
Error Amplifier Section						
Input Offset Voltage (Note 4)			-15		15	mV
Input Bias Current			-2	-0.1		µA
Large Signal Open Loop Voltage Gain		(Note 4)	60	86		dB
Slew Rate				0.6		v/µsec
Power Supply Rejection Ratio (Note 4)			60	86		dB
Output Source Current		V_{OH} = 3.5V	2			mA
Output Sink Current		V_{OL} = 2.0V	2			mA
Output Voltage Range (Note 6)		No Load on E.A. Output	1.2		4	V
Unity Gain Bandwidth				1.0		MHz
Phase Margin				57		°

(Electrical Characteristics continued next page.)

ELECTRICAL CHARACTERISTICS (Cont'd.)

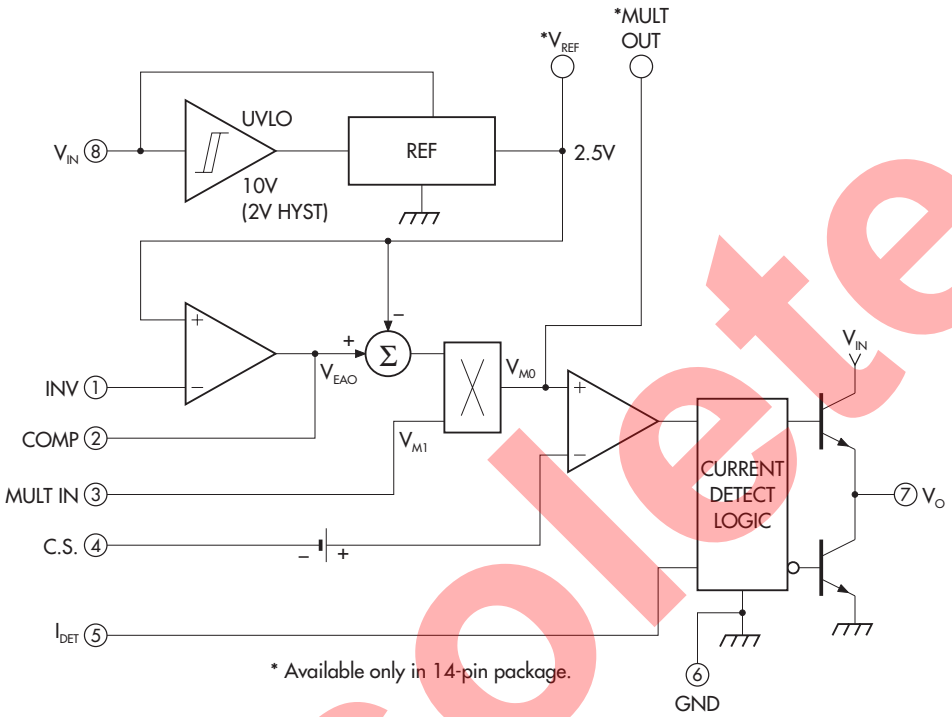
Parameter	Symbol	Test Conditions	SG3561A Min.	SG3561A Typ.	SG3561A Max.	Units
Multiplier Section						
M1 Input Voltage Range			0		2	V
M2 Input Voltage Range			V_{REF}		V_{REF} +1	V
Input Bias Current (M1)			-2		2	µA
Multiplier Gain (Note 5), (Note 4)		V_{M1} = 1V, V_{EA0} = 3.5V	0.52	0.65	0.78	/V
		V_{M1} = 2V, V_{EA0} = 3.5V		0.65		/V
Multiplier Gain Temperature Stability				-0.2		%/°C
Maximum Multiplier Output Voltage		V_{M1} = 1V, V_{EA0} > 4V		0.9		V
		V_{M1} = 2V, V_{EA0} > 4V		1.8		V
Current Sense Comparator Section						
Input Bias Current		0V ≤ V_{CS} ≤ 1.7V	-5	1	5	µA
Current Sense Delay to Output		E.A.$_{OUT}$ = 3.7V		200	500	ns
Detect Section						
Input Voltage Threshold			1	1.3	1.6	V
Hysteresis				175		mV
Input LO Clamp Voltage		I_{DET} = 100µA			0.95	V
Input HI Clamp Voltage		I_{DET} = 3mA	6.1	7.1		V
Input Current		1V ≤ V_{DET} ≤ 6V	-10		10	µA
Input HI/LO Clamp Diode Current		V_{DET} < 0.9V, V_{DET} > 6V			±3	mA
Output Driver Section						
Output High Voltage		I_L = -10mA, V_{IN} = 12V	7	9		V
Output Low Voltage		I_L = 10mA, V_{IN} = 12V		0.8	1.5	V
Output Rise Time		C_L = 1000pF		100	200	ns
Output Fall Time		C_L = 1000pF		90	200	ns

Notes: 4. Because the reference is not brought out externally, these specifications are tested at probe only, and cannot be tested on the packaged part. They are guaranteed by design, and shown for illustrative purposes only.

5. $K = \frac{V_{MO}}{(V_{M1}) \times (V_{EA0} - V_{REF})}$

6. This parameter, although guaranteed, is not tested in production.

BLOCK DIAGRAM / PIN DESCRIPTIONS



FUNCTIONAL DESCRIPTION

Pin	#	Description
V_{IN}	8	Input supply voltage. $V_{IN} \leq 8V$ $I_{IN} \leq 0.5mA$ $V_{IN\ MAX} < 25V$ $V_{IN} \geq 10V$ $I_{IN} \leq 15mA$
GND	6	Input supply voltage return. Must always be the lowest potential of all the pins.
INV	1	Inverting input of the Error Amplifier. The output of the Boost converter should be resistively divided to 2.5V and connected to this pin.
COMP	2	The output of the Error Amplifier. A feedback compensation network is placed between this pin and the INV pin.
MULT	3	Input to the multiplier stage. The full-wave rectified AC is divided to less than 2V and is connected to this pin.
C.S.	4	Input to the PWM comparator. Current is sensed in the Boost stage MOSFET by a resistor in the source lead, and is fed to this pin through a low-pass filter
I_{DET}	5	A current driven logic input with internal clamp. A second winding on the Boost inductor senses the flyback voltage associated with the zero crossing of the inductor current and feeds it to the I_{DET} pin through a limiting resistor. The logic circuit processes this signal, such that the converter operates in a discontinuous conduction current mode, where there is no current gap between the switching cycles.
V_O	7	PWM output pin. A totem-pole output stage specially designed for direct driving the MOSFET.

FIGURE INDEX

Application Information

FIGURE #

Typical Applications

FIGURE #

APPLICATION INFORMATION

FUNCTIONAL DESCRIPTION

The operation of the circuit is best described by referring to the diagram in Figure 1.

The multiplier stage generates an output voltage (V_{M0}) from the rectified waveform of the AC input (V_{M1}) and the amplitude of the error amplifier output (V_{EA}). This voltage controls the peak inductor current by turning the power MOSFET off at a threshold, where the current sense voltage (V_{CS}) reaches a given nominal value. This causes the power MOSFET to latch-off until the current in the inductor drops to zero. Once this happens, the secondary winding of the inductor changes its voltage polarity, and gets detected by an internal comparator stage. The polarity of the windings are chosen such that a low I_{DET} voltage turns on the power MOSFET and maintains operation until the above process repeats itself. An external trigger voltage to the IDET is required to start-up the converter until the auxiliary winding of the inductor takes over the operation.

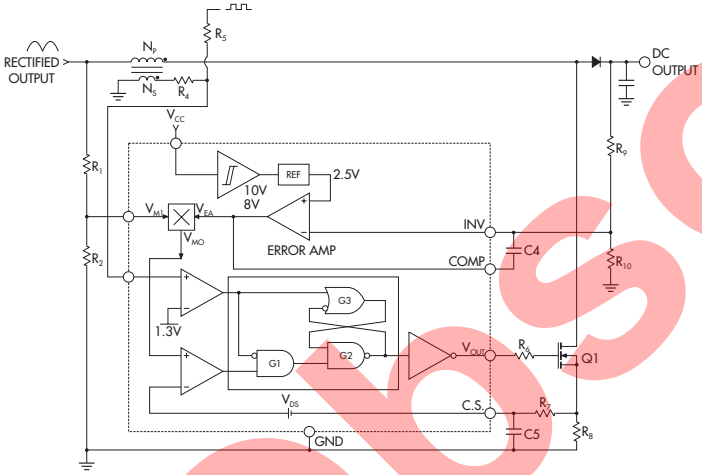


FIGURE 1 — GENERAL APPLICATION CIRCUIT

UNDERVOLTAGE LOCKOUT

The purpose of the undervoltage lockout is to perform two functions: 1) to maintain a low quiescent current during power-up, 2) to guarantee that the IC is fully functional before the output stage is activated. To realize this, a micropower comparator with a start-up threshold of 10V and a built-in hysteresis of 2V is incorporated. This comparator acts as a switch for the pre-regulator stage, which supplies a stable bias to the internal circuitry of the IC. Figure 2 shows a simplified schematic of this section, as well as the external components required, in-order to generate bootstraping voltage from the secondary winding of inductor. The operation of the circuitry is as follows.

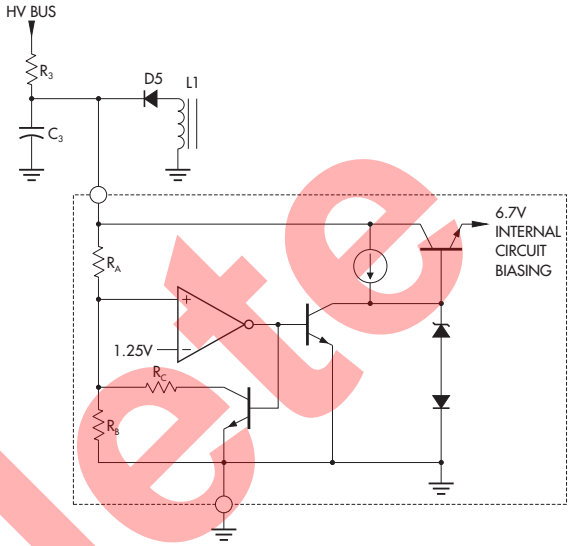


FIGURE 2 — START UP CIRCUITRY

Start-up capacitor C_3 is first charged by the current through resistor R_3. Once this voltage exceeds 10V, then the IC starts operating, requiring more supply current than R_3 can provide. This causes the energy stored in the capacitor to supply the IC with the operating current until the bootstrap winding on L1 takes over the power to maintain operation.

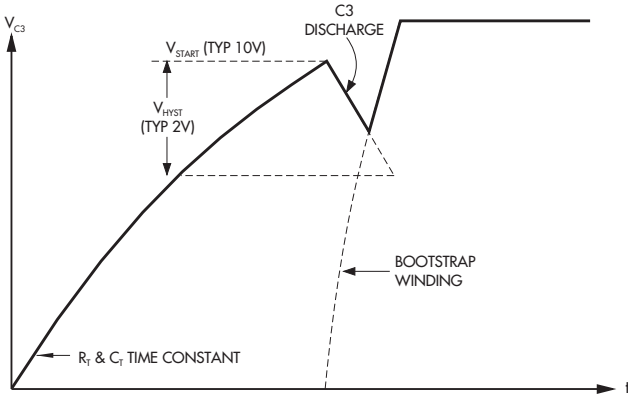


FIGURE 3 — START UP VOLTAGE

$$V_{START} = 1.25\left[\frac{R_A}{R_B \,||\, R_C} + 1\right] \qquad V_{HYST} = 1.25\,\frac{R_A}{R_C}$$

APPLICATION INFORMATION

VOLTAGE REFERENCE

The voltage reference is a low drift bandgap design which provides a stable +2.5V output with ±1.5% initial tolerance. This pin is internally connected to the non-inverting input of error amplifier and is only available in a 14-pin package. It can provide up to 2mA of current for powering any external circuitries and is not internally current limited.

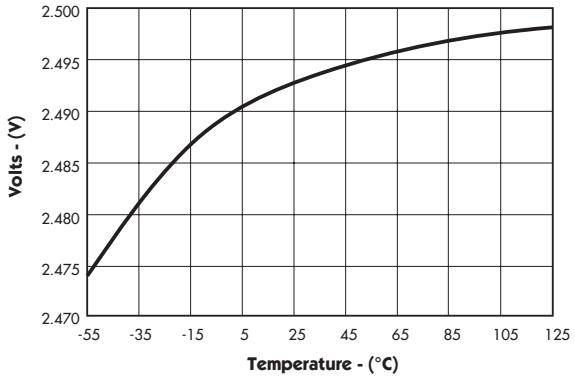
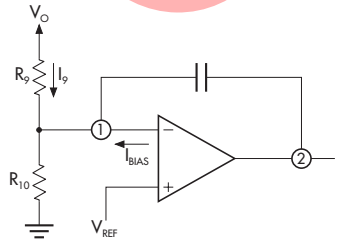


FIGURE 4 — REFERENCE VOLTAGE vs. TEMPERATURE

ERROR AMPLIFIER

The error amplifier is an internally compensated PNP input stage with access to the inverting input and output pin. The N.I. input is internally connected to the voltage reference and is available only in a 14-pin package. The amplifier is designed for an open loop gain of 85dB, along with a typical bandwidth of 1MHz and 57 degrees of phase margin. The amplifier's input bias current (2µA max.) results in a DC error in output voltage. In order to minimize this effect, the current flow in resistor R_9 must be much greater than the bias current; As an example, for a 1% error in output, the current must be at least 200µA. The error amp output is provided for an external compensation of the feedback loop. This compensation is typically just a capacitor connected between this pin and the inverting input pin. The compensation capacitor is designed to set the bandwidth such that it adequately rejects the low frequency ripple which is present at the output voltage.



$$BW = \frac{1}{2\pi R_9 C_4}$$

FIGURE 5 — TYPICAL COMPENSATION CIRCUIT

MULTIPLIER

The SG3561A features a one quadrant multiplier stage having two inputs: one is internally driven by a DC voltage (this being the difference of E.A. output and V_{REF} (M2)), and the other (M1) is available for external connection. The output is internally tied to an input of the PWM comparator. The rectified AC input is typically divided down to less than 1V and is connected to the "M1" input by a resistor divider. The output of the multiplier which is a function of both inputs, controls the inductor peak current during each cycle of operation.

The multiplier is mostly linear if the M1 input is limited to less than 1V and the E.A. output is kept below 3.5V (under all specified load and line conditions). The output clamps to a maximum value of 0.9V typically if the E.A. output is higher than 4V and V_{M1} = 1V.

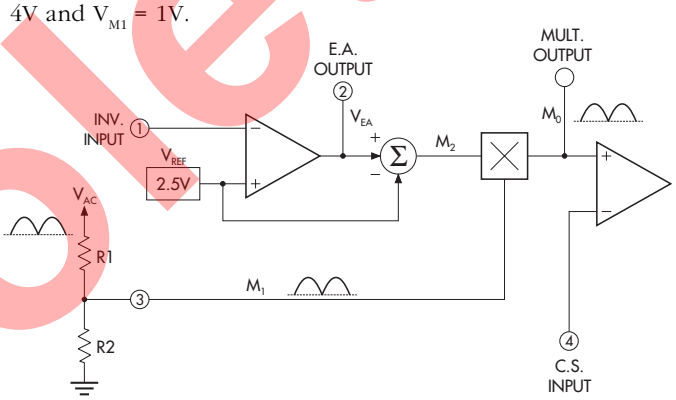


FIGURE 6 — MULTIPLIER CIRCUIT

$$K = \frac{V_{M0}}{V_{M1}(V_{EA} - V_{REF})}$$

where: K ≡ Gain
V_{MO} ≡ Mult. Output
V_{M1} ≡ Mult. Input
V_{EA} ≡ E.A. Output

CURRENT SENSE COMPARATOR / PWM LATCH

Current Sense comparator is configured as a PNP input differential stage with one input internally tied to the multiplier output and the other available for current sensing. Current is converted to voltage using an external sense resistor in a series with the power MOSFET (Q1). When voltage across this resistor exceeds the threshold set by the multiplier output, the current sense comparator terminates the gate drive to Q1, as well as resetting the PWM latch. The latch ensures that the output remains in a low state once the switch current falls back to zero.

An offset is built into current sense input to ensure that the output remains in a low state when the load is removed from the output of the converter. This offset is guaranteed to be higher than the multiplier offset during the above condition.

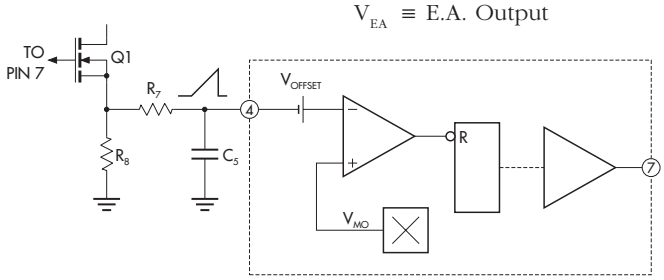
APPLICATION INFORMATION

CURRENT SENSE COMPARATOR / PWM LATCH (continued)

Sense resistor R_8 is designed according to the following formula:

$$R8 \leq \frac{V_{M0}}{I_{L\,MAX}}$$

where: K ≡ Gain
V_{MO} ≡ Mult. Output under min. line condition
V_{M1} ≡ Mult. Input
V_{EA} ≡ E.A. Output



R7 and C5 form a low pass filter to eliminate the leading edge current spike.

FIGURE 7 — CURRENT SENSE CIRCUIT

PWM DRIVER STAGE

The SG3561A output driver is designed for direct driving of power MOSFETs. It is a totem pole stage with ±0.5A peak current capability. This typically results in a 100 nanosecond rise and fall times into a 1000pF capacitive load. Additionally, the output is held low during the under voltage condition to ensure that the power MOSFET remains in the off state.

CURRENT DETECT LOGIC

The function of "current detect logic" is to sense the operating state of the boose inductor and to enable the output driver accordingly. To achieve this, the downward slope of the inductor current is detected by monitoring the voltage across a separate winding and is connected to the detector input (I_{DET}) pin. Once the inductor current drops to zero, the sensed voltage reverses, setting the I_{DET} input to a low-level, thus enabling the output driver. Since this is a negative voltage, a level shifter as shown in Figure 8 is provided to prevent the I_{DET} pin from going below the ground. The maximum current drawn from this pin must be limited to less than 3mA.

A high level voltage occurs when the inductor discharges. Referring to Figure 9, once the C.S. comparator inhibits the output driver and resets the flip-flop, the inductor voltage reverses and sets the I_{DET} pin to a high level. This ensures the reset instruction of the current sense comparator and reduces its noise susceptibility. An internal zener diode with maximum current capability of 3mA limits the positive voltage swing to 7 volts typically.

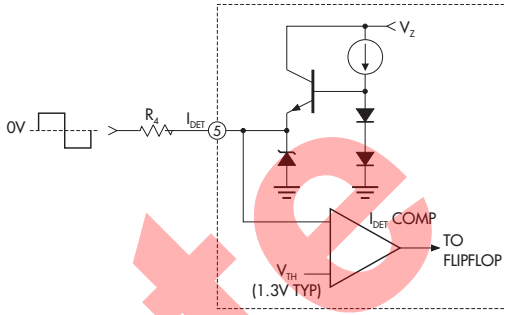


FIGURE 8 — I_{DETECT} INPUT CIRCUIT

Since the output driver is inhibited during the power-on cycle, an external trigger signal is required to start-up the converter before the I_{DET} winding takes over the operation. The trigger signal can be derived either from the second stage of the converter (i.e. the ballast voltage generator), or if stand alone operation is desired from a circuit as shown in Figure 9. Additionally, this signal should be low enough that the voltage from the detector winding is allowed to dominate during the normal operation.

The equations below describe the selection of R_4 and R_5 in Figure 10.

$$2500\ V_{WP} \geq R_4 \geq 400V_{WP} \qquad \text{where } V_{WP} \equiv \text{Peak detector voltage}$$

$$R_5 = 0.8\ R_4\left(\frac{V_{TR}}{1.6}\right) \qquad V_{TR} \equiv \text{Trigger voltage}$$

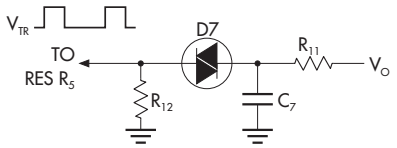


FIGURE 9 — TYPICAL START UP CIRCUIT USING DIAC

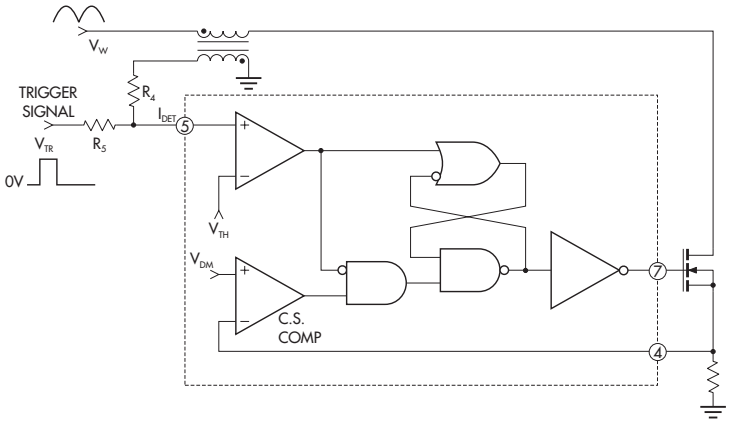


FIGURE 10 — I_{DETECT} LOGIC CIRCUIT

APPLICATION INFORMATION

TYPICAL APPLICATION

The application circuit shown in Figure 11 uses the SG3561A as the controller to implement a boost type power factor regulator. The IC controls the regulator, such that the inductor current is always operating in a discontinuous conduction mode with no current gaps. This mode of operation has several advantages over the fixed frequency discontinuous conduction mode: 1) The switching frequency adjusts itself to the AC line envelope, causing a sinusoidal current draw, 2) Since there is no current gap between the switching cycles, the inductor voltage does not oscillate, causing less radiated noise, 3) The lower peak inductor current causes less power dissipation in the power MOSFET.

A set of formulas have been derived specifically for this mode, and are used throughout the design procedure:

The following are specifications for the boost converter:

Input Voltage Range	-	100 to 130V RMS
Output Voltage	-	230V DC
Output Power	-	80W
Efficiency	-	95% at full load
Power Factor	-	> 0.99 at full load
Total Harmonic Distortion	-	< 10% at full load

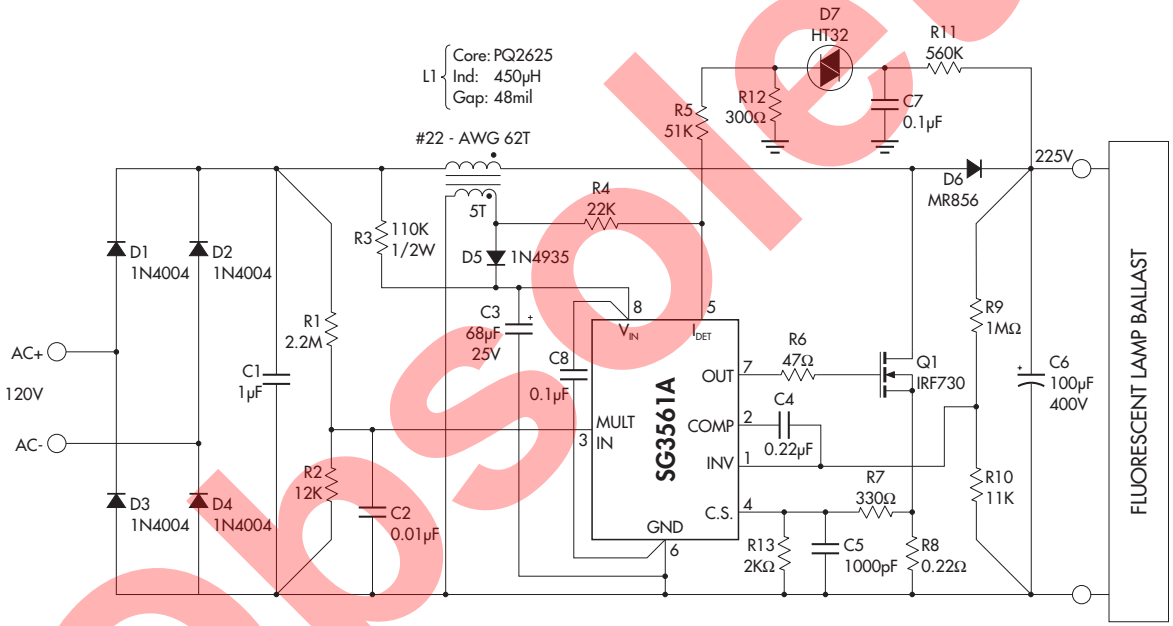


FIGURE 11 — TYPICAL APPLICATION WITH 120V INPUT

OUTPUT VOLTAGE REQUIREMENT

Since the converter is a boost type topology, it requires the output voltage to always be higher than the input voltage. It is recommended to choose this voltage at least 15% higher than the maximum input voltage.

$$V_O \geq 1.15 * 130\sqrt{2} = 211 \text{ Volts}$$

INDUCTOR PEAK CURRENT

It can be shown by referring to Figure 12 that the inductor peak current is always twice the average input current.

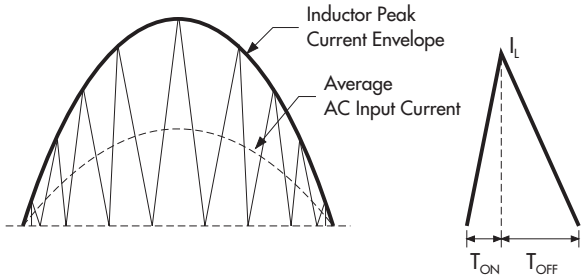


FIGURE 12 — INDUCTOR CURRENT

APPLICATION INFORMATION

INDUCTOR PEAK CURRENT (continued)

$$I_{IN(t)} = \sum AVE\,[I_L(t)]$$

$$I_{IN} = \frac{1}{T}\left[\frac{(I_L)(T)}{2}\right]\frac{I_L}{2}$$

$$I_{INpeak} = I_P = \frac{I_{LP}}{2}$$

I_{LP} = Inductor peak current at peak input voltage.

Maximum peak input current can be calculated by using:

$$I_P = \frac{2P_O}{\eta V_P}$$

where: $\eta \equiv$ Converter efficiency
$V_P \equiv$ Peak AC input voltage

assuming: $\eta = 95\%$, $P_O = 80W$, $V_{Pmin} = 100\sqrt{2} = 141$

$$I_P = \frac{2 * 80}{(.95)(141)} = 1.2A$$

$$I_{LP/min\ AC} = 2 * 1.2 = 2.4A$$

INDUCTOR DESIGN

The most important part of the circuit is to design the energy storage element. To do this, we use the following equation to calculate the inductance value:

$$L_1 = \frac{\eta\frac{V_O - V_P}{V_O} T V_P^2}{4 P_O}$$

where: $\eta \equiv$ Efficiency
$V_O \equiv$ Output DC Voltage
$V_P \equiv$ Peak AC Input Voltage
$T \equiv$ Switching period
$P_O \equiv$ Output Power

$$L_1 = \frac{.95\left(\frac{230 - 120\sqrt{2}}{230}\right) 20 * 10^{-6} * (120\sqrt{2})^2}{4 * 80} = 448\mu H$$

Once the inductance is calculated, we can either use the area product method (AP) or other K_g (based on copper losses method), for selecting proper core. In this example, we apply the K_g approach using the following steps:

Step 1: Calculate K_g using

$$K_g = \frac{\Omega}{P_{CU}}\left(\frac{L_1 I_{LP}^2}{B}\right)^2$$

where: $L_1 \equiv$ Required inductance
$\Omega \equiv 1.724 * 10^{-8}$ m
$B \equiv$ Maximum flux density
$I_{LP} \equiv$ Maximum peak inductor current
$P_{CU} \equiv$ Maximum copper dissipation

INDUCTOR DESIGN (continued)

Assume: $P_{CU} = 1.6W$ (2% of total output)

$$K_g = \frac{1.724 * 10^{-8}}{1.6}\left[\frac{450 * 10^{-6} * (2.4)^2}{0.15}\right]^2 = 3.21 * 10^{-12}\ m^5$$

Step 2: Choose a core with higher K_g than the one calculated in Step 1.

$$K_g/core = k\frac{A_W A_E^2}{I_W}$$

where: $k \equiv$ Winding coefficient (typ. k=0.4)
$A_W \equiv$ Bobbin window area
$A_E \equiv$ Effective core area
$I_W \equiv$ Mean length per turn

K_g factor for TDK PQ2625:
$A_W = 47.7mm^2$
$A_E = 118mm^2$
$I_W = 56.2mm$

$$K_g = 0.4\frac{(47.7)(118)^2}{56.2}(mm)^5 = 4.7 * 10^{-12}\ m^5$$

Step 3: Determine number of turns.

$$N = \frac{L I_{LP}}{B A_E}$$

$$N = \frac{450 * 10^{-6} * 2.4}{0.15 * 118 * 10^{-6}} = 61 \text{ turns}$$

$$A_{WIRE} = k\frac{A_W}{N} = 0.4\frac{47.7}{61} = 0.31mm^2 = 480mil^2$$

choose #22 AWG with r = 0.0165Ω/feet resistance.

$$R_W = N * I_w * r$$
$$R_W = 0.185\Omega$$

Step 4: Calculate air gap.

$$I_g = \frac{\mu_O N^2 A_E}{L}$$

$$I_q = \frac{4\pi * 10^{-7} * (61)^2 * 118 * 10^{-6}}{450 * 10^{-6}} = 0.122cm = 48 \text{ mil}$$

Step 5: $N_S \approx N_P\frac{V_S}{V_O}$

$$N_S = 61\frac{15}{230} = 4T \text{ where: } V_S \equiv \text{secondary voltage}$$

N_S may be adjusted to account for the drop in start-up capacitor.

APPLICATION INFORMATION

POWER MOSFET SELECTION

The voltage rating of MOSFET and rectifier must be higher than the maximum value of the output voltage.

$V_{DS} \geq 1.2V_{O\ MAX}$ $\quad V_{DS} \geq 282V$

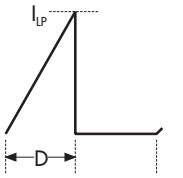
The RMS current can be approximated by multiplying the RMS current at the peak of the line by 0.7.

$I_{RMS} = 0.7\ I_{LP}\ \sqrt{D/3}$ $\quad$ D ≡ On-time duty cycle

D = 0.39 at V_{AC} = 100V

I_{LPI} = 2.4A

$I_{RMS} = (0.7)\ (2.4)\ (\sqrt{.39/3}) = 0.61A$



I_{RMS}/triangle = $I_{LP}\ \sqrt{D/3}$

$R_{DS} \leq \frac{P_{DC}}{I_{RMS}^2}$

P_{DC} ≡ allowable power dissipation

$R_{DS} \leq \frac{1}{0.61}$ $\quad = 1.6\Omega$

choose IRF730 with $R_{DS} = 1\Omega$ and V_{DS} = 400V.

CURRENT SENSE AND MULTIPLIER COMPONENT SELECTION

Resistors R_1 and R_2 are selected such that the peak voltage at M1 input (pin 3) is 1V at the maximum line voltage.

$\frac{R_1}{R_2} = V_{AC\ PEAK} - 1$

$\frac{R_1}{R_2} = 183$ $\quad$ if $\mathbf{R_1 = 2.2M}$ $\quad$ then R_2 = 12K

The value of R_8 can be selected using the following equations:

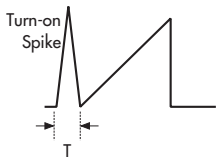
$V_{M0} = k\ V_{M2} * V_{M1}$ $\quad V_{M1}$ = Maximum voltage at M1 input under min. line condition

$V_{M0} = (0.75)\ (3.5 - 2.5)\ (0.77) = 0.58$

$R_8 = \frac{V_{MO}}{I_{LP}} = \frac{0.58}{2.4} = \frac{0.58}{2.4} = 0.24\Omega$ $\quad$ choose $R_8 = 0.22\Omega$

To eliminate the turn-on current spike, a low pass filter with a high corner frequency must be designed such that:

$R_7C_4 \geq 1.6T$



if T = 100nsec

$R_7C_4 \geq 0.16\mu sec$

assuming C_4 = 1000pF $\quad R_7 \geq 160\Omega$

The values of R_7 and C_4 may be optimized further based on each specific application. Additionally R_{13} can be used to adjust the overall loop gain in order to maintain regulation at the minimum input voltage.

ERROR AMPLIFIER COMPONENT SELECTION

The values of R_9 and R_{10} are calculated based on the operating output voltage. The value of C_5 is mainly selected to reject the 120Hz ripple associated with the output voltage. Lack of adequate ripple rejection causes input current distortion; however, too much rejection will make a slow loop response and a high voltage overshoot during the turn-on.

$\frac{R_9}{R_{10}} = \frac{V_O}{V_{REF}} - 1$

$\frac{R_9}{R_{10}} = \frac{230}{2.5} - 1 = 91$

assuming $R_9 = 1M\Omega$ $\quad$ Then: R_{10} = 11K

For output voltages higher than 250V, safety regulations may require two ¼W resistors to be placed in series.

Assuming a 40dB rejection at 120Hz:

$\text{Gain} = \frac{1}{2\pi\ f\ R_9\ C_5}$ $\quad$ Gain/120Hz ≤ 0.01

$C_5 \geq \frac{100}{2\pi(120)(10^6)}$

$C_5 \geq 0.133\mu f$ $\quad$ choose $C_5 = 0.22\mu f$

$BW = \frac{1}{2\pi\ R_9\ C_5} = \frac{1}{2\pi\ (10^6)(.22 * 10^{-6})} = 0.72Hz$

INPUT RECTIFIER AND CAPACITOR SELECTION

The current through each diode is a half-wave rectified sine wave. The maximum current happens at minimum line with a peak value of 1.2A.

$I_{AVE} = \frac{I_{PEAK}}{\pi} = \frac{1.2}{\pi} = 0.38A$

choose **1N4004 with 1A rating.**

$P_{DISS} = (I_{AVE})\ (V_F) = 0.38 * 0.9 = 0.344W$

$T_J = T_A + P_D\ x\ \theta_{JA}$ $\quad$ assuming θ_{JA} = 65°C/W for 1/8" lead length.

$T_J = 80 + (.344)(65) = 102°C$

APPLICATION INFORMATION

INPUT RECTIFIER AND CAPACITOR SELECTION (continued)

Assuming φ is the percentage of allowable input current ripple, C_1 can be calculated using the following equations:

$$R_{EFF} = \frac{2\,P_O}{\eta\,I_P^{\,2}}$$

$$C_1 \geq \frac{1}{\varphi\,2\pi\,R_{EFF}\,f_{SW}}$$

f_{SW} ≡ Switching frequency of inductor current at peak input voltage.

if φ = 3%

$$R_{EFF} = \frac{2 * 80}{(.95)(1.2)^2} = 117\Omega$$

$$C_1 \geq \frac{1}{(.03)(2\pi)(117)(50000)} = 0.9\mu F$$

choose **1µF, 250V capacitor**.

BIAS SUPPLY COMPONENT SELECTION

A bleeding resistor (R_3) off of either output voltage or capacitor C_1 can be selected such that it provides sufficient start-up current for the IC, as well as charging the start-up capacitor C_3.

$$R_3 = \frac{V_{P\,MIN}}{I_{ST}}$$

$$R_3 = \frac{140}{0.5 * 10^{-3}} = 280K$$

$$P_{R3} = \frac{V_{IN\,MAX}}{R_3} \leq 0.25W$$

$$R_3 \geq 4V_{IN\,MAX}^{\,2}$$

I_{ST} ≡ Start-up current
$V_{P\,MIN}$ ≡ Peak AC voltage at min. AC line
$V_{IN\,MAX}$ ≡ Max. RMS input

$280K \geq R_3 \geq 68K$ choose $\mathbf{R_3 = 110K}$

The start-up capacitor must be chosen such that it supplies power to the IC until the voltage on the bootstrap winding exceeds the start threshold (this is typically around 10 volts). C_3 must also be designed to have low ripple voltage at twice the line frequency.

$$C_{3\,(\Delta V_R)} \geq \frac{I}{2\,f_{LINE}\,\Delta V_R}$$

$$C_{3\,(\Delta T)} \geq \frac{I\Delta T}{\Delta V_H}$$

I ≡ Operating current
f_{LINE} ≡ Line frequency
ΔV_r ≡ Ripple voltage
ΔT ≡ Time allowed for bootstrap winding to reach start-up threshold

$$C_{3\,(\Delta V_R)} \geq \frac{15 * 10^{-3}}{2 * 60 * 2} = 62\mu F$$

assuming ΔT = 2ms

$$C_{3\,(\Delta T)} \geq \frac{15 * 10^{-3} * 2 * 10^{-3}}{1.8V} = 17\mu f$$

choose C_3 = 68µF.

OUTPUT CAPACITOR SELECTION

There are mainly two criterias for selecting the output capacitor: A large enough capacitance to maintain a low ripple voltage, and a low ESR value in order to prevent high power dissipation due to RMS currents.

The output capacitance can be approximated from the following equation:

$$C_6 \geq \frac{I_{DC}}{2\pi\,f_{LINE}\,\Delta V}$$

where: I_{DC} ≡ DC output current
ΔV ≡ Output ripple

$$I_{DC} = \frac{80}{230} = 0.348A$$

assuming 5% peak to peak ripple,

$$C_6 \geq \frac{0.348}{2\pi\,(60)\,(11.5)} = 81\mu F$$

choose $\mathbf{C_6 = 100\mu F.}$

CURRENT DETECT COMPONENT SELECTION

The values of R_4 and R_5 can be calculated using the following equations:

$$400V_{WP} \geq R_4 \geq 2500V_{WP}$$

$$R_5 = 0.8R_4\left(\frac{V_{TR}}{1.6}\right)$$

where:

V_{WP} ≡ Maximum detector winding voltage

V_{TR} ≡ Trigger voltage

APPLICATION INFORMATION

CURRENT DETECT COMPONENT SELECTION (continued)

Assuming V_{WP} = 15V and peak trigger voltage from the start-up circuitry is 7V, the values R_4 and R_5 using above formulas are:

$6K\Omega \leq R_4 \leq 37.5K\Omega$ choose R_4 = 22K

$R5 = 0.8\ (22)\left(\frac{7}{1.6} - 1\right) = 59.4K\Omega$ choose R_5 = 51K

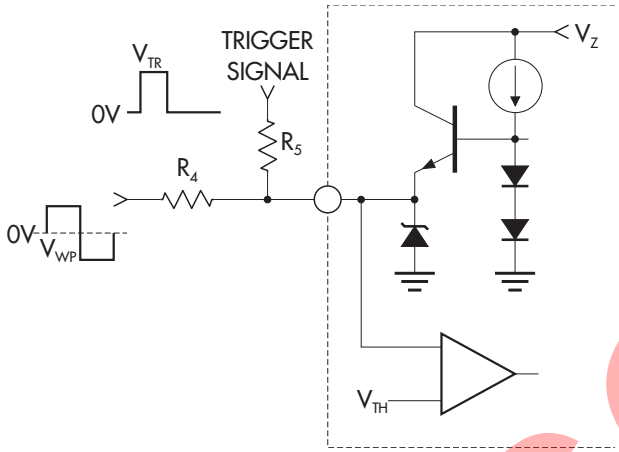


FIGURE 13 — CURRENT DETECT EXAMPLE

TYPICAL APPLICATIONS

120V

Pin numbers are for 8-pn dip package.

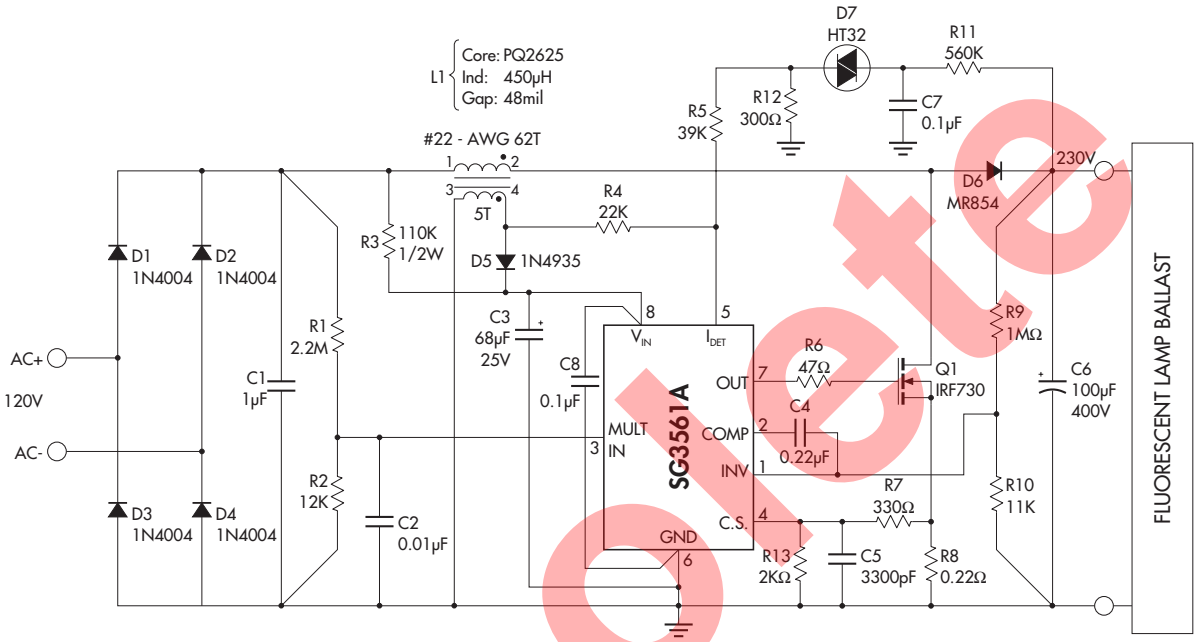


FIGURE 14 — TYPICAL APPLICATION OF THE SG3561A IN AN 80W FLUORESCENT LAMP BALLAST WITH ACTIVE POWER FACTOR CONTROL.

Electrical Specification — 120VAC Input — 230VDC / 80W Output

Ref.	Component	Manuf.	Ref.	Component	Manuf.
IC	SG3561AM	Linfinity	C1	1µF/250V	
L1	PQ2625/H7C1 Core	TDK	C2	0.01µF/50V	
Q1	IRF730, 400V	I.R.	C3	68µF/25V	
D1-D4	1N4004, Diode, 1A	Motorola	C4	0.22µF/50V	
D5	1N4935, Diode, 1A	Motorola	C5	3300pF/50V	
D6	MR854, 3A, 400V	Motorola	C6	100µF/400V	
D7	HT32, DIAC	TECCOR	C7	0.1µF/50V	
R1	2.2MΩ		C8	0.1µF/50V	
R2	12KΩ				
R3	110K, ½W				
R4	22K				
R5	51K				
R6	47Ω				
R7	330Ω				
R8	0.22Ω, ½W - Carbon type				
R9	1MΩ, 1% Res				
R10	11KΩ, 1% Res				
R11	560KΩ				
R12	300Ω				
R13	2KΩ				

TYPICAL APPLICATIONS

220V

Pin numbers are for 8-pn dip package.

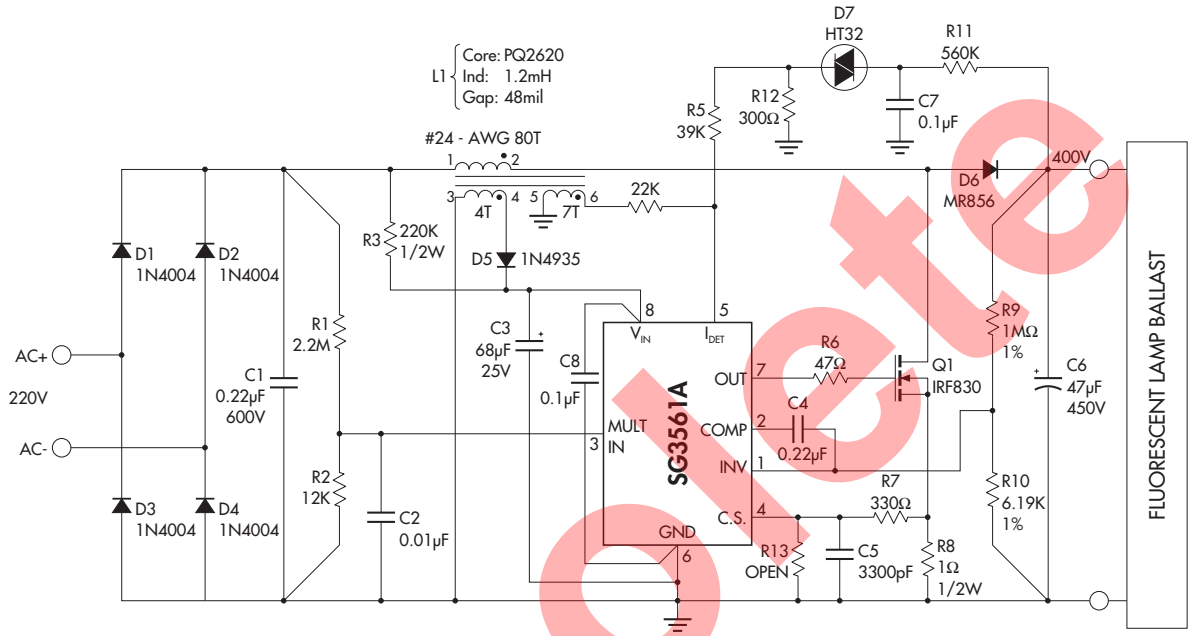


FIGURE 15 — TYPICAL APPLICATION OF THE SG3561A IN AN 80W FLUORESCENT LAMP BALLAST WITH ACTIVE POWER FACTOR CONTROL.

Electrical Specification — 220VAC Input — 400VDC / 80W Output

Ref.	Component	Manuf.	Ref.	Component	Manuf.
IC	SG3561A	Linfinity	C1	0.22µF/600V	
L1	PQ262/H7C1 Core	TDK	C2	0.01µF/50V	
Q1	IRF830, 500V	I.R.	C3	68µF/25V	
D1-D4	1N4004, Diode, 1A	Motorola	C4	0.22µF/50V	
D5	1N4935, Diode, 1A	Motorola	C5	3300pF/50V	
D6	MR856, 3A, 600V	Motorola	C6	47µF/450V	
D7	HT32, DIAC	Teccor	C7	0.1µF/50V	
R1	2.2MΩ		C8	0.1µF/50V	
R2	12KΩ				
R3	220K, ½W				
R4	22K				
R5	39K				
R6	47Ω				
R7	330Ω				
R8	1Ω, ½W - Carbon type				
R9	1MΩ, 1% Res				
R10	2.7MΩ				
R11	560KΩ				
R12	300Ω				
R13	2KΩ				

TYPICAL APPLICATIONS

277V

Pin numbers are for 8-pn dip package.

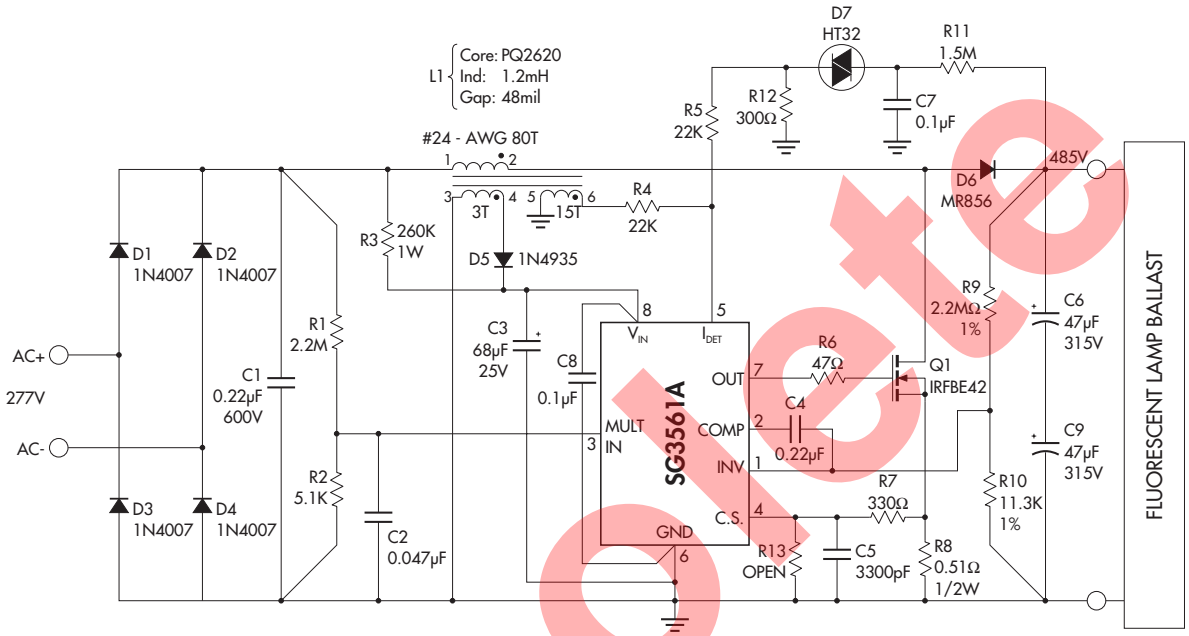


FIGURE 16 — TYPICAL APPLICATION OF THE SG3561A IN AN 80W FLUORESCENT LAMP BALLAST WITH ACTIVE POWER FACTOR CONTROL.

Electrical Specification — 277VAC Input — 485VDC / 80W Output

Ref.	Component	Manuf.	Ref.	Component	Manuf.
IC	SG3561A	Linfinity	C1	0.22µF/600V	
L1	PQ2620/H7C1 Core	TDK	C2	0.047µF/50V	
Q1	IRFBE42, 600V	I.R.	C3	68µF/25V	
D1-D4	1N4007, Diode, 1A	Motorola	C4	0.22µF/50V	
D5	1N4935, Diode, 1A	Motorola	C5	3300pF/50V	
D6	MR856, 3A, 600V	Motorola	C6, C9	47µF/315V	
D7	HT32, DIAC	TECCOR	C7	0.1µF/50V	
R1	2.2MΩ		C8	0.1µF/50V	
R2	5.1KΩ				
R3	260KΩ, 1W				
R4	22KΩ				
R5	22KΩ				
R6	47Ω				
R7	330Ω				
R8	0.51Ω, ½W - Carbon type				
R9	2.2MΩ, 1% Res				
R10	11.3KΩ, 1% Res				
R11	1.5KΩ				
R12	300Ω				
R13					

TYPICAL APPLICATIONS

277V - Buck Boost Application

Pin numbers are for 8-pn dip package.

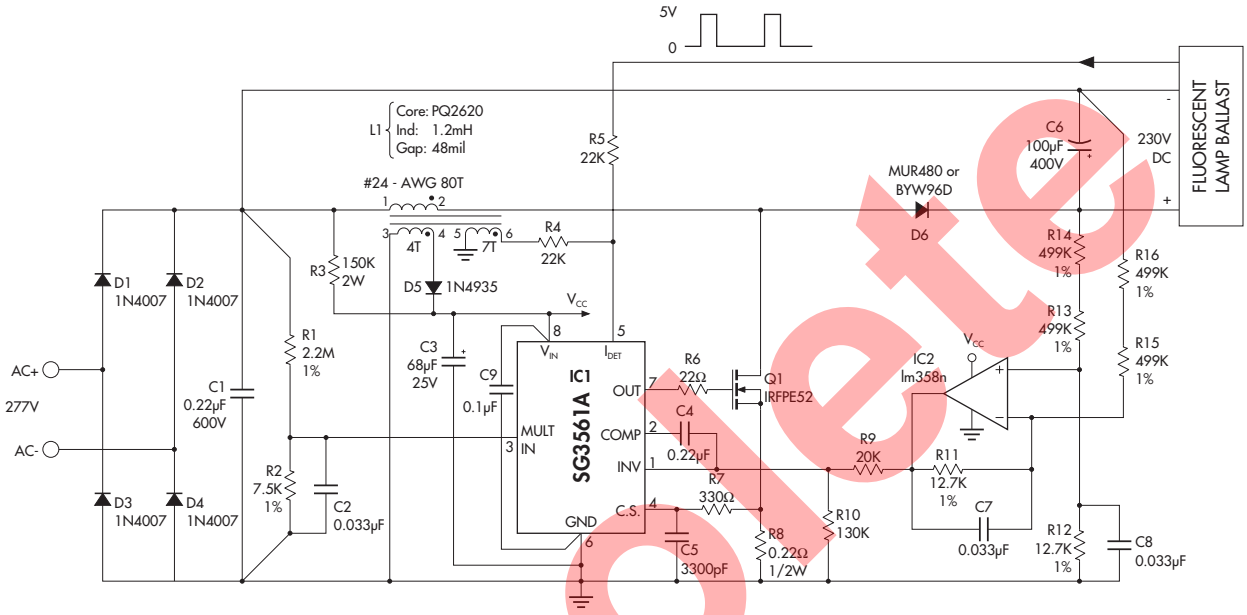


FIGURE 17 — TYPICAL APPLICATION OF THE SG3561A IN AN 80W FLUORESCENT LAMP BALLAST WITH ACTIVE POWER FACTOR CONTROL.

Electrical Specification — 90-265VAC Input — 230VDC / 80W Output

Ref.	Component	Manuf.	Ref.	Component	Manuf.
IC	SG3561A	Linfinity	C1	0.22µF/600V	
IC2	LM358N		C2	0.033µF/50V	
L1	PQ2620/H7CI Core	TDK	C3	68µF/25V	
Q1	IRFPE52, 800V	I.R.	C4	0.22µF/50V	
D1-D4	1N4007, Diode, 1A	Motorola	C5	3300pF/50V	
D5	1N4935, Diode, 1A	Motorola	C6	100µF/400V	
D6	BYW96D, 4A, 800V		C7, C8	0.033µF/50V	
R1	2.2MΩ, 1%		C9	0.1µF/50V	
R2	7.5KΩ, 1%				
R3	150K, 2W				
R4	22kΩ				
R5	22K				
R6	22Ω				
R7	330Ω				
R8	0.22Ω, ½W				
R9	20K				
R10	130K				
R11	12.7K, 1%				
R12	12.7K, 1%				
R13, 14	499K, 350V				
R15, 16	499K, 350V				

TYPICAL APPLICATIONS

90 - 265V

Pin numbers are for 8-pn dip package.

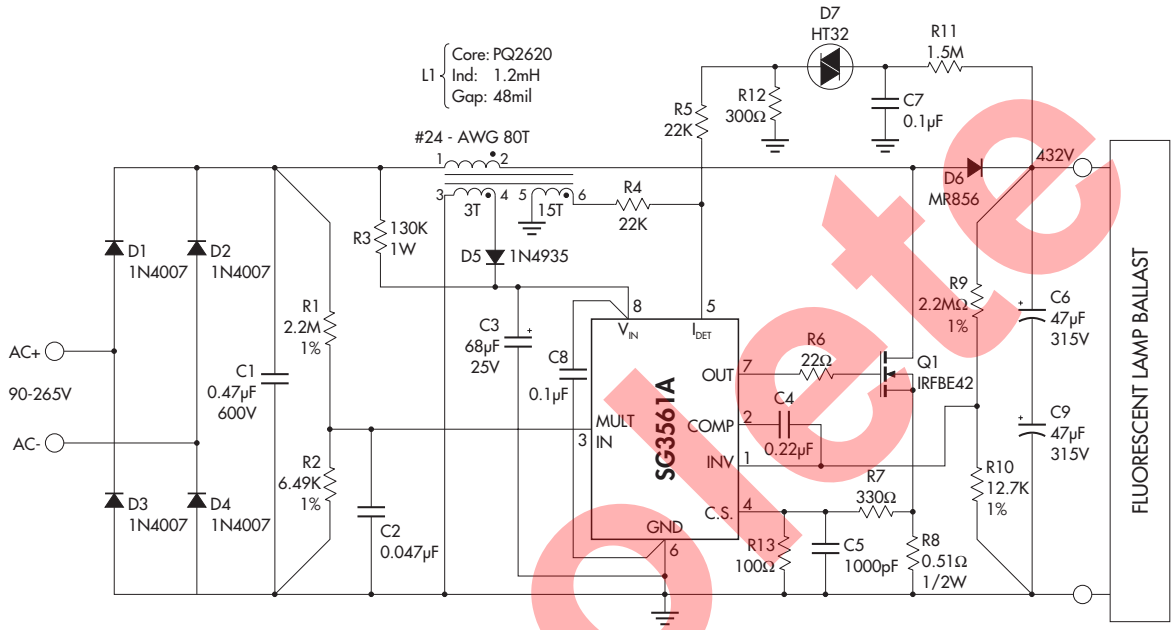


FIGURE 18 — TYPICAL APPLICATION OF THE SG3561A IN AN 80W FLUORESCENT LAMP BALLAST WITH ACTIVE POWER FACTOR CONTROL.

Electrical Specification — 90-265VAC Input — 432VDC / 80W Output

Ref.	Component	Manuf.	Ref.	Component	Manuf.
IC	SG3561A	Linfinity	C1	0.47µF/600V	
L1	PQ2620/H7C1 Core	TDK	C2	0.047µF/50V	
Q1	IRFBE42, 600V	I.R.	C3	68µF/25V	
D1-D4	1N4007, Diode, 1A	Motorola	C4	0.22µF/50V	
D5	1N4935, Diode, 1A	Motorola	C5	1000pF/50V	
D6	MR856, 3A, 600V	Motorola	C6, C9	47µF/315V	
D7	HT32, DIAC	TECCOR	C7	0.1µF/50V	
R1	2.2MΩ, 1%		C8	0.1µF/50V	
R2	6.49K, 1%				
R3	130K, 1W				
R4	22kΩ				
R5	22K				
R6	22Ω				
R7	330Ω				
R8	0.51Ω, ½W - Carbon type				
R9	2.2MΩ, 1% Res				
R10	12.7KΩ, 1% Res				
R11	1.5KΩ				
R12	300Ω				
R13	100Ω				