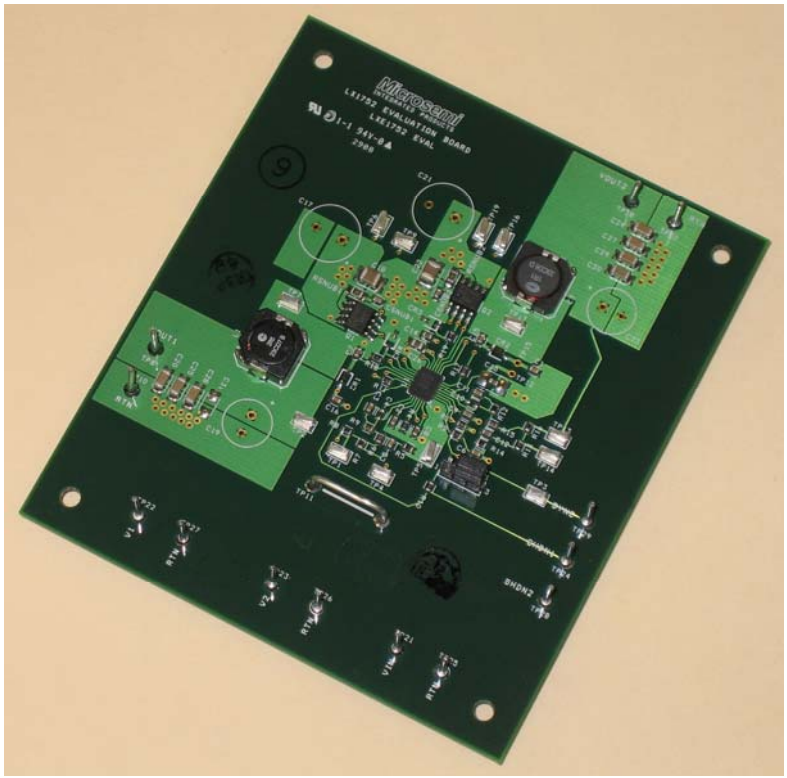
LX1752

Dual Interleaving PWM Controller

Evaluation Board



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Introduction to Product

LX1752 is a dual output, PWM controller. It is designed to generate two independent output voltages. Multiple LX1752 ICs can be synchronized to an external clock, or slaved to a single LX1752 IC operating as a master. The LX1752 Evaluation board is configured for a 1.2V and 3.3V output, however these voltages can easily be changed by a single resistor value change (1 per output). The evaluation board is capable of output currents up to 5 Amps with the components installed.

Features:

Dual Output with individual input voltages for each output.
Jumper selectable phase positioning for interleaving of 2 LX1752 ICs in synchronized operation.
Can be synchronized with external clock signal.

Operation

The LX1752 Evaluation Board has three inputs for power, and two outputs for powering external loads. The three power inputs are wired together for single supply use. A power supply capable of 9V to 15V at a minimum current of 5 Amps is required for full output load operation. The LX1752 Evaluation Board is optimized for 12V power supply input; however, power supply voltages up to 22V may be accommodated. Multiple LX1752s may be synchronized together by connecting together their respective sync signals (available at TP29 on the evaluation board). Synchronizing to an external clock is possible by connecting TP29 through an open drain switch to ground and driving the switch with a 100ns pulse at a frequency 5% higher than the set PWM frequency. Two synchronized LX1752s can be interleaved in a three output, 120°degree phase, or a four output, 90° phase configuration by changing the state of the PSET input. PSET input is determined by the jumper position on JB1 and is shown in Table 1:

Table1

LX1752 Phase Position			
JB1 Jumper Position	PSET Input	VOUT 1 Phase Position	VOUT 2 Phase Position
2 - 3	Ground	0°	180°
Open	Open	90°	270°
1 – 2	High	120°	240°

The LX1752 Evaluation board is configured to operate at 800kHz switching frequency, with outputs set at 1.2V and 3.3V. The Output Voltage can be changed by changing the value of R5 (VOUT1), and R14 (VOUT2). The value of these resistors can be determined as follows:

$$R = \frac{12.7 \times 10^3}{V_{OUT} - 0.7}$$

The Switching Frequency can be changed by changing the value of R4. R4 is found by:

$$R_{FREQ}(K\Omega) = \frac{1}{27.56E^{-9} \times F_{OSC}} - 5.156$$

Note: Changes in PWM frequency (without changing the inductor) will change inductor ripple current (ripple will increase significantly at lower frequencies), and subsequent output ripple voltage. Depending on load current, the maximum peak current rating of the inductors could easily be exceeded at lower switching frequencies. The inductors installed in the LX1752 Evaluation board have a peak current rating of 7 Amps for VOUT1, and 9 Amps

for VOUT2. The closed-loop bandwidth of the LX1752 Evaluation Board is set at 100kHz with a 12 Volt input; PWM frequencies should not be set lower than 500kHz (100kHz X 5) without changing the compensation components. See the applications information section in the LX1752 Datasheet for details.

The following tables describe the test point signals available on the LX1752 Evaluation Board.

Test points

Test Point	Description
TP1 & TP2	Measurement points for a Network Analyzer, such as AP Industries model 200. Used to generate Bode Plot for closed-loop analysis of compensation components. TP1 and TP2 are connected to each side, respectively, of a 20Ω resistor, in line with the feedback signal from VOUT1.
TP3	Sync signal I/O. Can be used to monitor internal Sync signal, or to input sync signal from an external source.
TP4	Buffered VREF output. Provides a source for 0.8V reference.
TP5	Signal Ground
TP6	HO1 gate drive signal
TP7	VOUT1 switch node signal
TP9	LO1 gate drive signal
TP11	Ground Plane connection – used for connecting scope probe grounds
TP12 & TP15	Jumper points for connecting VIN to VCCL. Connect these two points together for VIN input voltage less than 6V, or 4.5V ≤ VIN ≤ 6V. **For V_{IN} voltages greater than 6V, these test points must not be connected together.**
TP13 & TP14	Measurement points for a Network Analyzer, such as AP Industries model 200. Used to generate Bode Plot for closed-loop analysis of compensation components. TP13 and TP14 are connected to each side, respectively, of a 20Ω resistor, in line with the feedback signal from VOUT2.
TP16	HO2 gate drive signal
TP17	VOUT2 switch node signal
TP19	LO2 gate drive signal

Input and Output Connection Points

Test Point	Description
TP21 & TP25	Power and Ground connection for LX1752s VIN pin. TP21 is supply positive; TP25 is supply return. TP21 is jumpered to V1 (TP22) and V2 (TP23) on the LX1752 Evaluation Board, but may be disconnected from V1 and V2 and ran separately. Supply voltage on TP21 is limited to 22V.
TP22 & TP26	Power and Ground connection for V1. V1 is VOUT1 input voltage rail. TP22 is supply positive; TP26 is supply return. V1 (TP22) is jumpered to VIN (TP21) and V2 (TP23) on the LX1752 Evaluation Board, but may be disconnected from VIN and V2 and powered separately. Supply voltage on TP22 is limited to 22V.
TP23 & TP27	Power and Ground connection for V2. V2 is VOUT2 input voltage rail. TP23 is supply positive; TP27 is supply return. V2 (TP23) is jumpered to VIN (TP21) and V1 (TP22) on the LX1752 Evaluation Board, but may be disconnected from VIN and V1 and powered separately. Supply voltage on TP23 is limited to 22V.
TP8 & TP10	Output load connection for VOUT1. TP8 is output positive; TP10 is return. Capable of 5 Amps max. output current at 3.3V.
TP18 & TP20	Output load connection for VOUT2. TP18 is output positive; TP20 is return. Capable of 5 Amps max. output current at 1.2V.
TP24	Test Point connection for SHDN1 pin. May be used to monitor the discharge portion of hiccup

Test Point	Description
	mode during a fault condition. This signal switches low during the discharge portion of hiccup, and switches high during the recovery (soft start) portion of hiccup. Primarily used for test, but can be used as a fault monitor at the system level.
TP28	Test Point connection for SHDN2 pin. May be used to monitor the discharge portion of hiccup mode during a fault condition. This signal switches low during the discharge portion of hiccup, and switches high during the recovery (soft start) portion of hiccup. Primarily used for test, but can be used as a fault monitor at the system level.
TP29	Sync Signal. Can be connected to another LX1752 sync pin for synchronous operation. May also be connected to an external sync clock by connecting TP29 to an open drain switch to ground and driving the switch with a 100ns pulse at a frequency 10% higher than the PWM frequency set by R4. The LX1752 syncs on the falling edge of Sync signal.

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LX1752 Evaluation Board BOM

Item Number	Quantity	Part Reference	Description	Manufacturer	Manufacturer Part Number
1	REF		Assembly Drawing, LX1752 Evaluation Board	Microsemi	EVB2886X3
2	REF		Schematic, LX1752 Evaluation Board	Microsemi	ES2886X3
3	1	PCB	Printed Circuit Board, LX1752 Evaluation Board	Microsemi	SGE2886X3
4	1	C14	Capacitor, Ceramic, 1.0uF, 6.3V, 10%, 0603 Case	Panasonic	ECJ-1VB0J105K
5	5	C1,C6, C7, C15, C16	Capacitor, Ceramic, 0.1uF, 16V, 10%, X7R, 0603 Case	Panasonic	ECJ-1VB1C104K
6	1	C13	Capacitor, Ceramic, 1.0uF, 25V, 10%, 0603 Case	Panasonic	ECJ-2FB1E105K
7	2	C3, C11	Capacitor, Ceramic, 3.3nF, 50V, X7R, 0603 Case	Panasonic	ECJ-1VB1H332K
8	2	C4, C10	Not Used		
9	2	C2, C9	Capacitor, Ceramic, 0.22uF, 10V, 10%, X5R, 0603 Case	Panasonic	ECJ-1VB1A224K
10	2	C18, C22	Capacitor, Ceramic, 10uF, 25V, 20%, X5R, 1210 Case	Panasonic	ECJ-4YB1E106M
11	3	C19, C23, C31	Not Used		
12	7	C20, C24, C25, C27 - C30	Capacitor, Ceramic, 10uF, 10V, 20%, X5R, 1206 Case	TDK	3216X5R1A106M
13	1	C26	Capacitor, Ceramic, 4.7uF, 6.3V, 20%, X5R, 0805 Case	Panasonic	ECJ-GVB0J475M
14	2	C8, C12	Capacitor, Ceramic, 470pF, 50V, 0603 Case	Panasonic	ECJ-1VC1H471J
15	3	C5, Csnub1, Csnub2	Capacitor, Ceramic, 680pF, 50V, 0603 Case	Panasonic	ECJ-1VC1H681J
16	2	C17, C21	Not Used		
17	2	CR1, CR2	Diode, Schottky, 100mA, 30V, SOD-323 Case	Central Semiconductor	CMDSH-3

Item Number	Quantity	Part Reference	Description	Manufacturer	Manufacturer Part Number
18	2	CR3, CR4	Not Used		
19	1	L1	Inductor, Shielded, Power, 2.5uH, 7 Amp	Coiltronics	DR1040-2R5-R
20	1	L2	Inductor, Shielded, Power, 1.1uH, 9 Amp	Coiltronics	DR1030-1R1-R
21	2	Q1, Q2	Mosfet, Dual N Channel, FDS6910, 7.5 Amp, .017 Ohm, 30V, SO8 Case	Fairchild Semiconductor	FDS6910
22	3	R1, R2, R10	Resistor, 1.00K, 5%, 1/10W, 0603 Case	Panasonic	ERJ-3EGYJ102V
23	2	R18, R19	Resistor, 0 Ohm, 0603 Case	Panasonic	ERJ-3GEY0R00V
24	2	Rsnub1, Rsnub2	Resistor, 2.2Ω, 5%, 1/4W, 0805 Case	ROHM	ESR10EZPJ2R2
25	1	R4	Resistor, 40.2K, 1%, 1/16W, 0603 Case	Panasonic	ERJ-3EKF4022V
26	1	R5	Resistor, 4.87K, 1%, 1/16W, 0603 Case	Panasonic	ERJ-3EKF4871V
27	2	R6, R15	Resistor, 18.2K, 1/16W, 0603 Case	Panasonic	ERJ-3EKF1822V
28	1	R7	Resistor, 1.2K, 5%, 1/10W, 0603 Case	Panasonic	ERJ-3EGYJ122V
29	2	R8, R16	Resistor, 20 Ohms, 1/16W, 0603 Case	Panasonic	ERJ-3EKF20R0V
30	2	R11, R17	Resistor, 2.74K, 1/16W, 0603 Case	Panasonic	ERJ-3EKF2741V
31	1	R9	Resistor, 15K, 5%, 1/10W, 0603 Case	Panasonic	ERJ-3EGYJ153V
32	1	R14	Resistor, 24.9K, 1%, 1/16W, 0603 Case	Panasonic	ERJ-3EKF2492V
33	1	R9	Resistor, 11K, 5%, 1/10W, 0603 Case	Panasonic	ERJ-3EGYJ113V
34	1	R13	Resistor, 1.6K, 5%, 1/10W, 0603 Case	Panasonic	ERJ-3EGYJ162V
35	1	JB1	Header, 3 Position, Vertical Mount, .100 Center	3M	929647-02-36-I
36	13	TP1 - TP7, TP9, TP13, TP14, TP16, TP17, TP19	Test Point, Miniature Surface Mount	Keystone	5015

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Item Number	Quantity	Part Reference	Description	Manufacturer	Manufacturer Part Number
37	13	TP8, TP10, TP18, TP20 - TP29	Pins, Terminal, .042 diameter	Vector	K24C/M
38	AR	TP11	20AWG Buss Wire Loop	Alpha Wire	297 SV001
39	1	U1	IC, 2 Phase Buck Controller, LX1752-CLQ	Microsemi	LX1752-CLQ

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Silkscreen and Test Setup

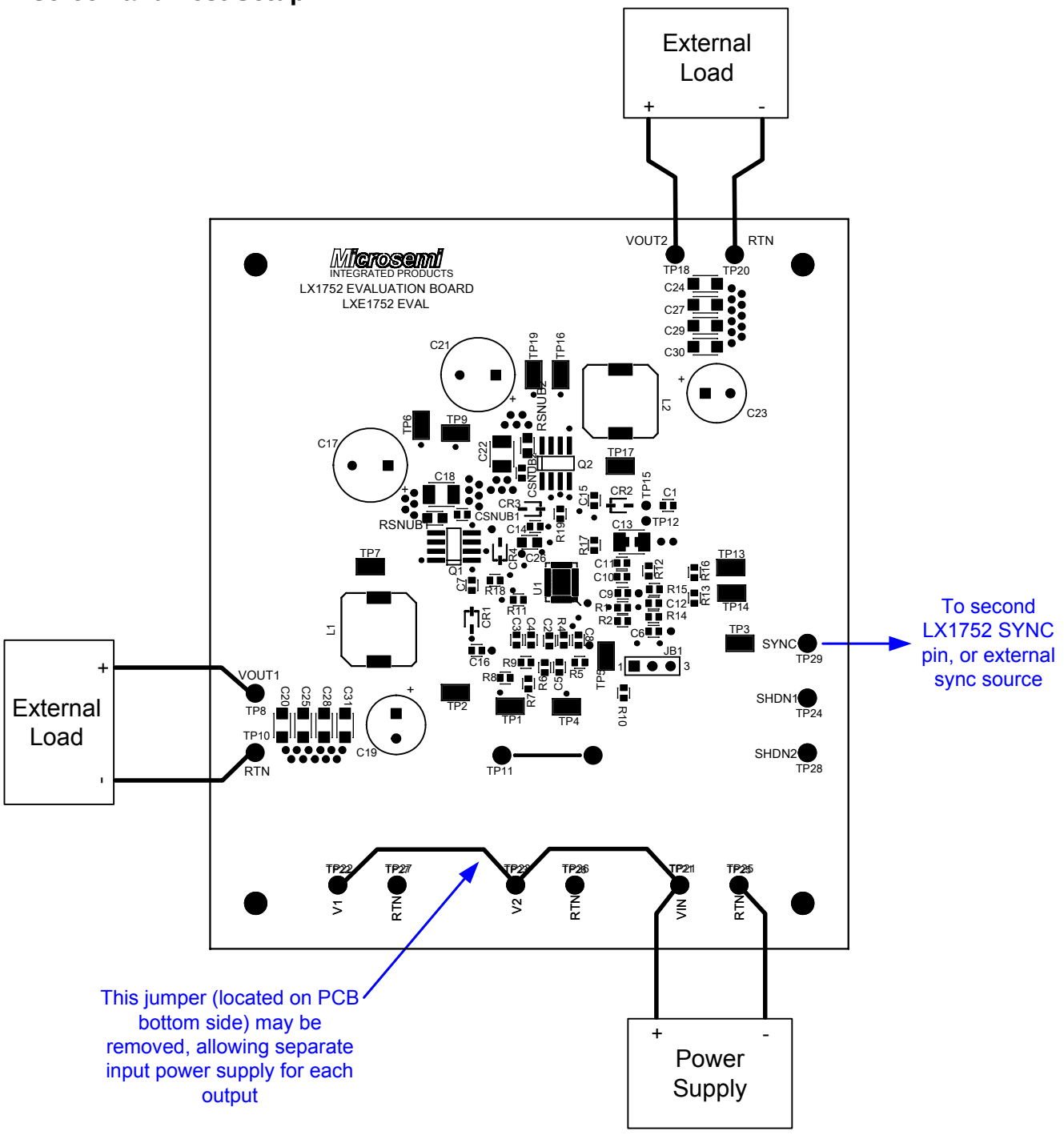


Figure 1. LX1752 Evaluation Board Test Setup

Schematic

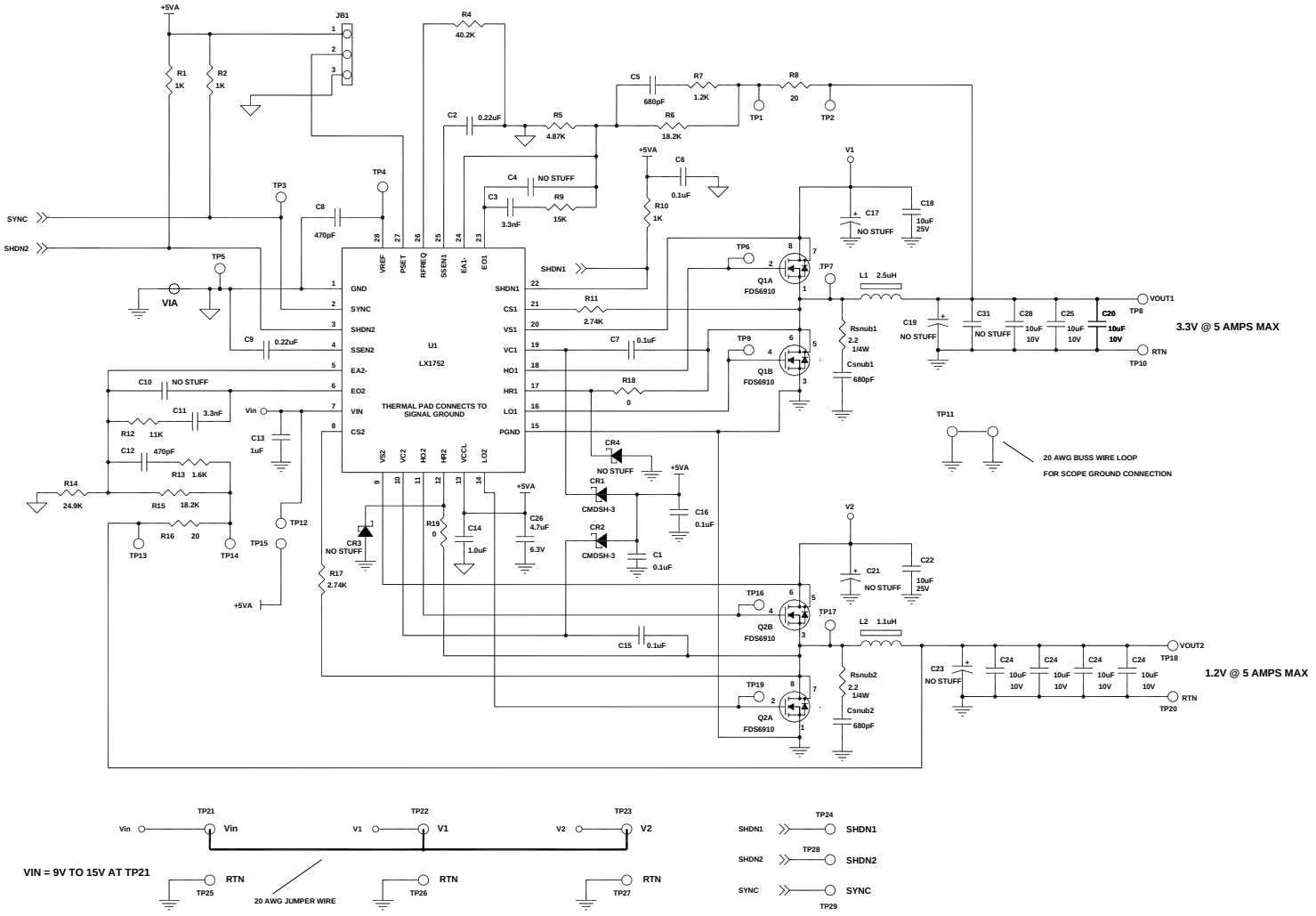


Figure 2. LX1752 Evaluation Board Schematic

Printed Circuit Board Layout Recommendations

Careful attention to PCB layout is necessary to insure proper operation with minimal noise generation. When laying out the PCB, these guidelines should be followed:

1) Keep the input capacitor, output capacitor, output inductor and output MOSFETs (upper and lower), close together, and tie all high current output returns directly to a suitable power ground plane.
2) Keep the high current ground return paths separate from the signal return paths. It is recommended that a separate signal ground plane be used, with a common tie point between the power ground plane and the signal ground plane established at the IC signal ground pin.
3) Place the input decoupling capacitor as close to the upper and lower MOSFETs as practical. Connections between this capacitor and the Upper and Lower MOSFETs Drain and Source connections, respectively, should be as short as practical. The LDO filter capacitor should be placed as close to the VCCL pin as practical.
4) PGND connection to the Source pin of the Lower MOSFET should be as short as practical, and should be established with a direct connection (using no vias) if possible.
5) VS_X Pin connections should be Kelvin connected directly at the Upper MOSFET's drain pin(s).
6) HR_X connection to the Upper MOSFET's Source pin should be as short as practical, and should be established with a direct connection (using no vias) if possible.
7) LOX and HOX should be connected to their respective MOSFET gate pins with as short a trace as practical, and should be established with a direct connection (using no vias) if possible.
8) The current sense (CS_X) resistor connection to the junction of the Upper MOSFET's Source, and the Lower MOSFET's drain should be as short as possible.
9) Place the CS_X resistor as close to the CS_X pin as possible. CSx pin is sensitive to capacitance to ground. If possible, minimize this capacitance by removing any ground plane area directly below the CSx pin pad and trace connection to the CSx resistor.
10) Place all compensation and feedback components as close to their respective error amplifier pins as practical. Keep the error amplifier input connections (EA_X-) as short as possible.
11) Place the frequency programming resistor, R_{FREQ} as close to the RFREQ and GND pins as practical.
12) For best thermal performance, the LX1752 thermal pad should be tied to signal ground, using 12 mil diameter (drill size) vias. Vias should be spaced 47mils apart in a grid array. See Figure 3 for details. Thermal vias are optional; the LX1752 will operate with reduced thermal performance without them.

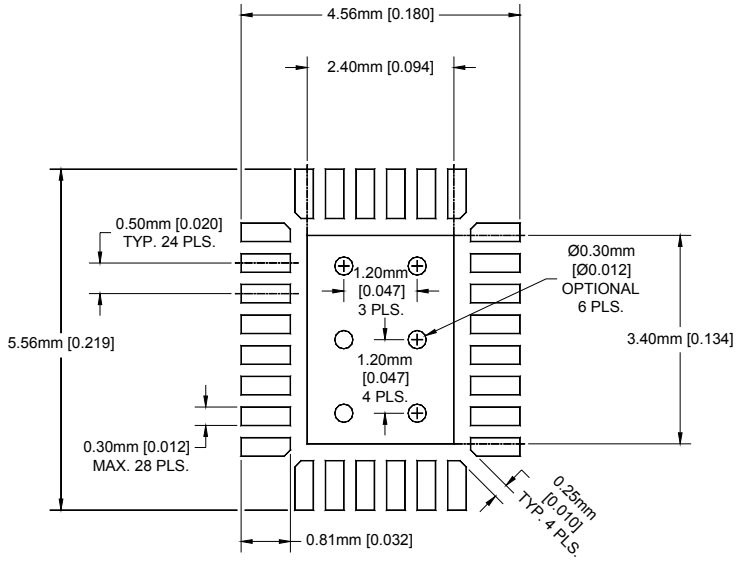
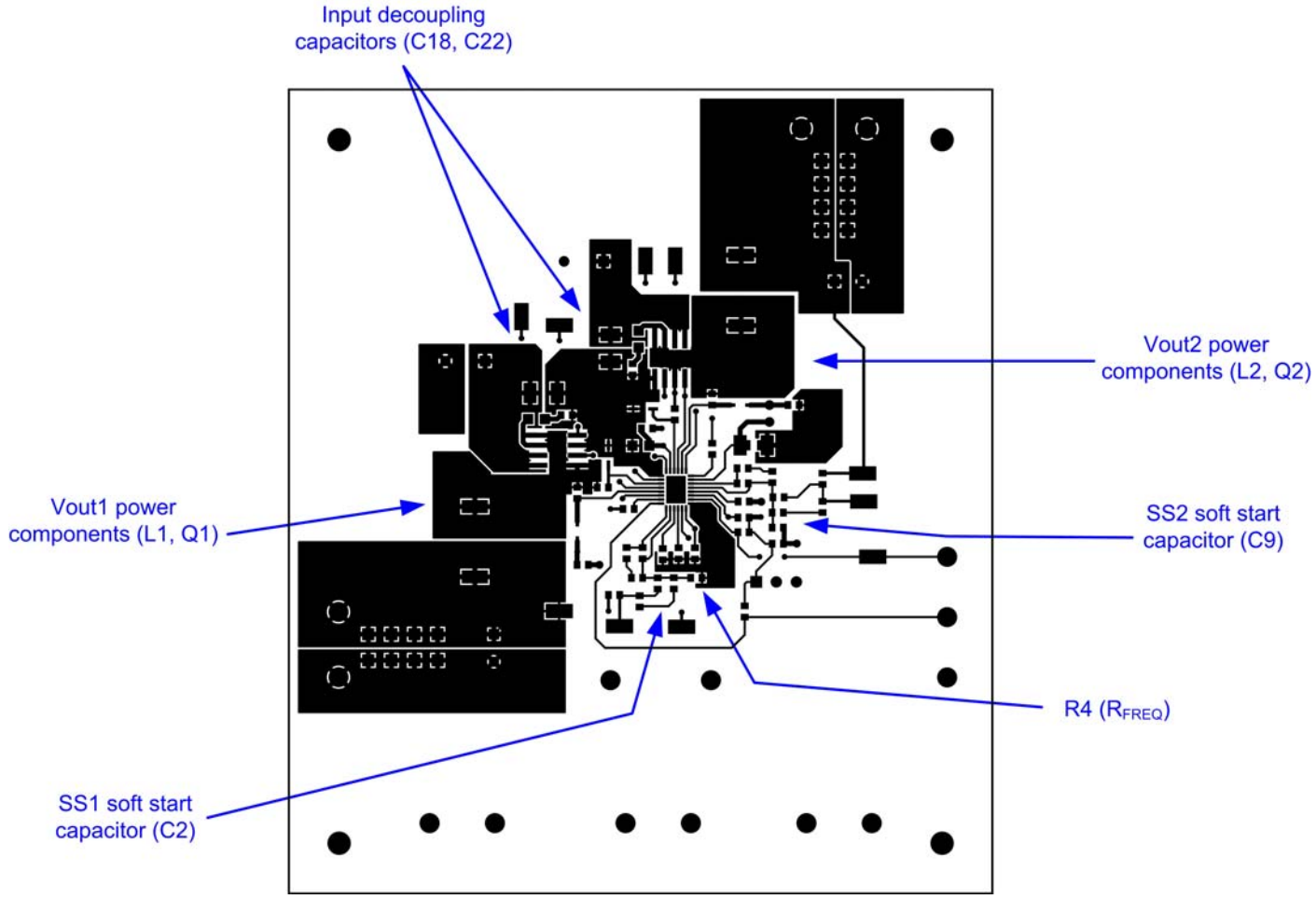


Figure 3. 4x5mm LQ package suggested PCB pad layout.

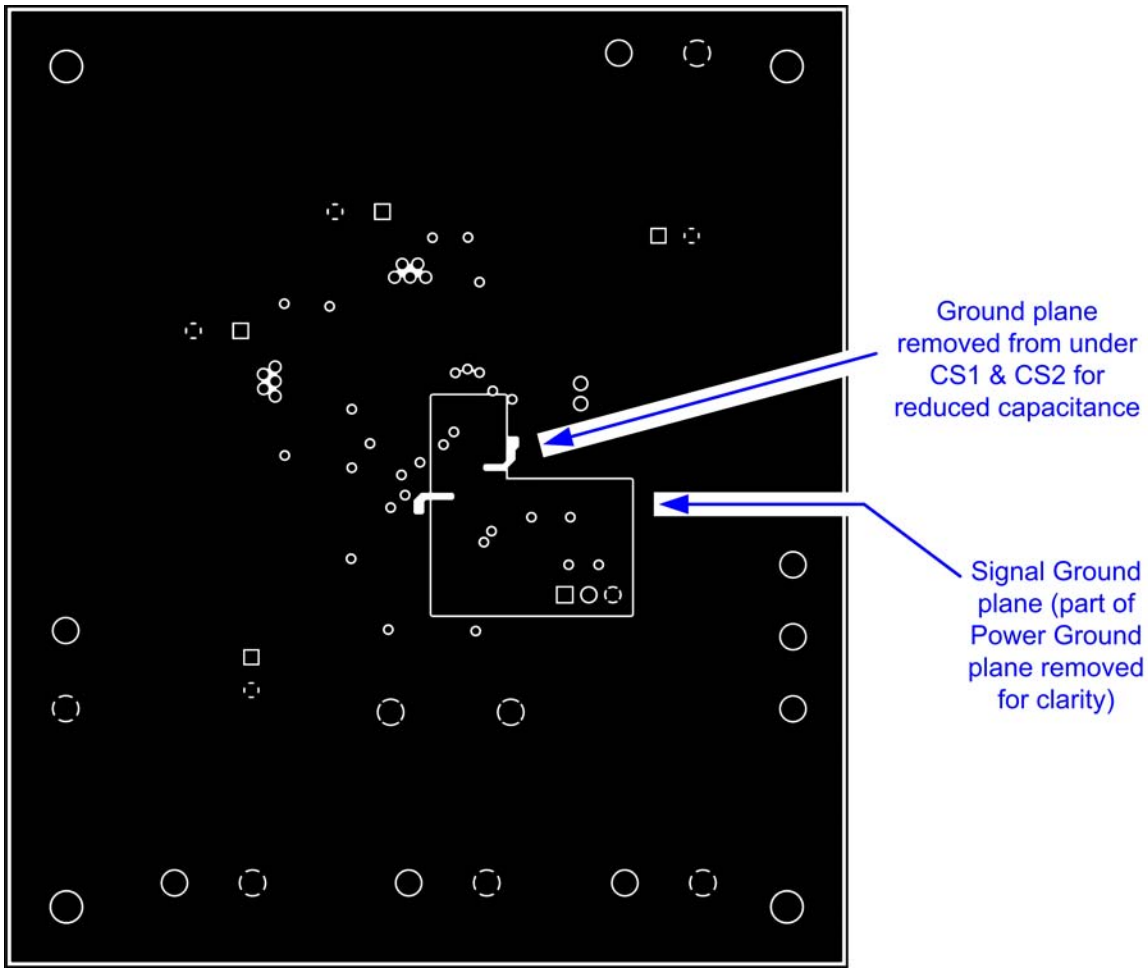
LX1752 Evaluation Board Printed Circuit Layout

PCB LAYOUT GUIDE – TOP LAYER



External PCB dimensions (W x H): 3.5 in. X 4.0 in. (88.9mm x 101.6mm)

PCB LAYOUT GUIDE – INNER LAYER 1 – POWER & SIGNAL GROUND PLANE



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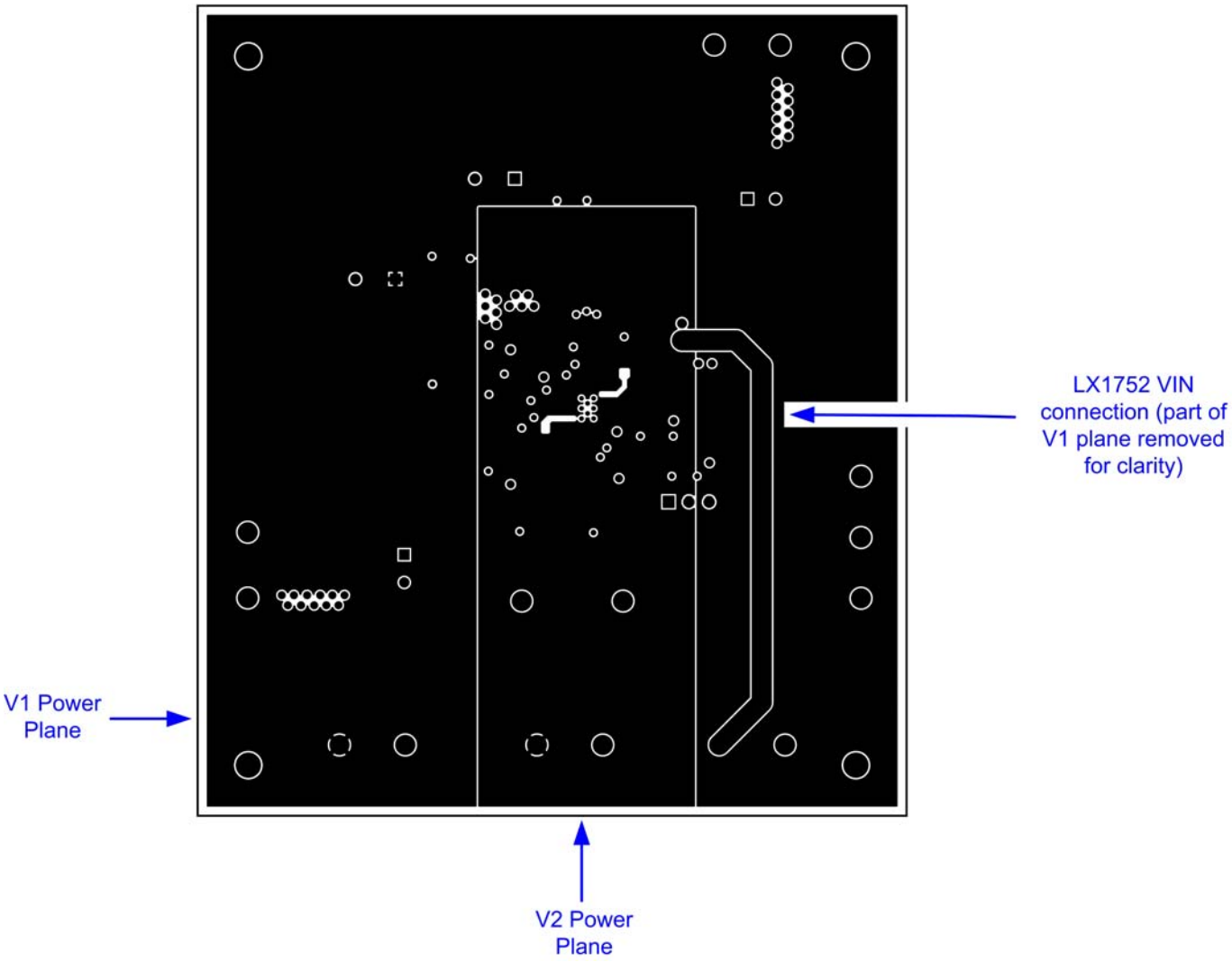
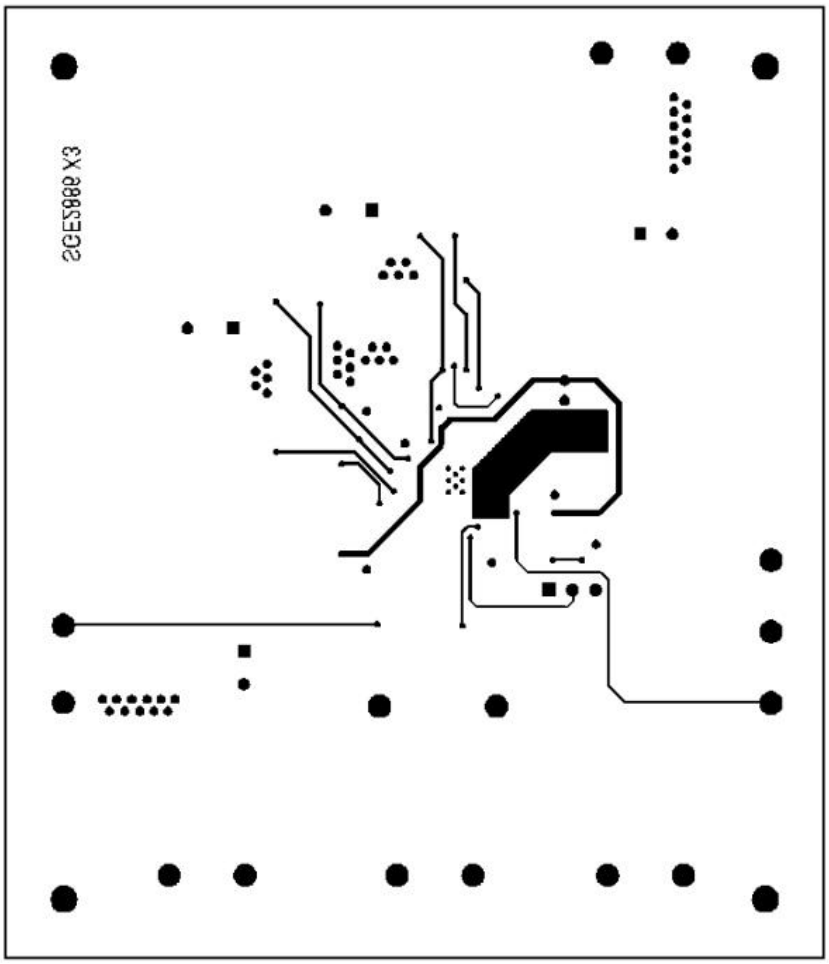
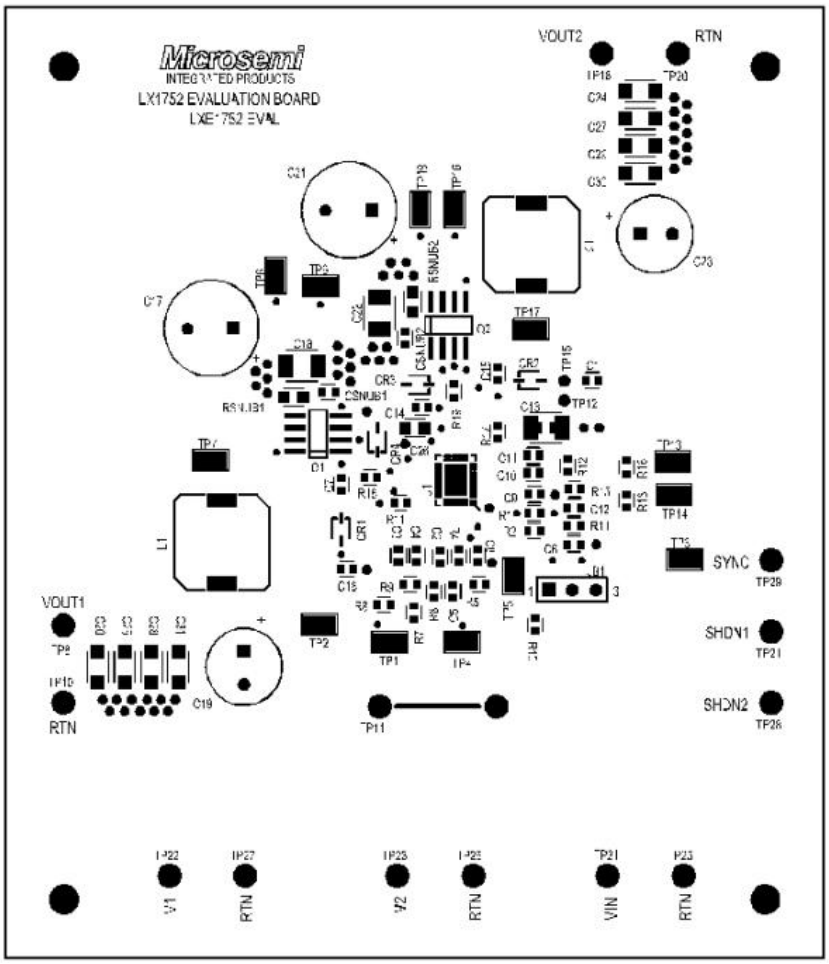
PCB LAYOUT GUIDE – INNER LAYER 2 –V1 & V2 POWER



PCB LAYOUT GUIDE – BOTTOM LAYER (TOP SIDE VIEW – MIRROR IMAGE FROM BOTTOM SIDE)



PCB LAYOUT GUIDE – TOP SILKSCREEN & SOLDER MASK



Test Hookup and Operation

The following is a demonstration scenario that can be used to evaluate the LX1752:

1) Connect a Power supply capable of 9V – 15V, 5 Amps output, to VIN and RTN (TP21 (+) and TP25 (-), respectively). Insure the supply is shut off before connecting.
2) Using an Oscilloscope, monitor test points TP7, TP17, and TP3. TP7 and TP17 are VOUT1 and VOUT2 switch nodes, respectively; TP3 is the LX1752's sync signal. Trigger on the falling edge of the signal on TP3. Probe grounds may be connected to TP11.
3) Monitor VOUT1 (TP8 (+), and TP10 (-)), and VOUT2 (TP18 (+) and TP20 (-)) with a DMM.
4) Insure the position of the jumper JB1 is as follows:
    a. JB1 = jumper in position 2-3.
5) Power on the supply, and insure current is less than 100mA. Switch node waveforms on TP7 and TP17 should be continuous pulse waveforms with peak voltage levels approximately equal to the supply voltage.
6) SYNC signal present on TP3 should be a narrow, negative-going spike, approximately 5 Volts in amplitude. Frequency will be 800kHz +/- 5%
7) VOUT1 should measure 3.3 Volts, +/- 3%; VOUT2 should measure 1.2 Volts, +/- 3%.
8) Connect suitable loads to VOUT1 and VOUT2: TP8 (+) and TP10 (-) for VOUT1; TP18 (+) and TP20 (-) for VOUT2. Loads may be resistive or electronic loads. Loads should be able to handle at least 20 Watts (VOUT1), and 10 Watts (VOUT2). If using a resistive load, 0.66 Ohms 20 Watts (or higher) on VOUT1, and 0.24 Ohms 10 Watts (or higher) on VOUT 2 will load the outputs to their full rated capacity (assumes standard configuration with 3.3V and 1.2V output on VOUT1 and VOUT2, respectively).
9) Check short circuit limit: momentarily short VOUT1 with a small, heavy gauge wire. Average input power supply current will reduce significantly, and will cycle up/down in magnitude. Verify VOUT1 switch node signal at TP7 changes from a continuous pulse stream to a pulse stream that cycles on/off, with the on period approximately 4% of the overall on/off cycle. The on time for VOUT1 will be approximately 9.5 ms with the installed 0.22uF capacitor (C2). Verify that VOUT2 is unaffected and is still regulating. Remove the short across VOUT1
10) Momentarily short VOUT2 with a small, heavy gauge wire. Average input power supply current will reduce significantly, and will cycle up/down in magnitude. Verify VOUT2 switch node signal at TP17 changes from a continuous pulse stream to a pulse stream that cycles on/off, with the on period approximately 4% of the overall on/off cycle. The on time for VOUT2 will be approximately 9.5ms with the installed 0.22uF capacitor (C9). Verify that VOUT1 is unaffected and is still regulating. Remove the short across VOUT2
11) For 4 output interleaving, synchronize two LX1752 Evaluation Boards by connecting a wire between both evaluation board's SYNC signal test points (TP29). Place jumper JB1 on one of the evaluation boards in position 2-3, and leave jumper JB1 on the other board open. Monitor test points TP7 and TP17 on both boards, verify that the switch node outputs are interleaved at approximate 90° intervals.

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