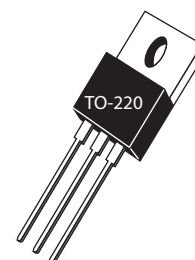


## N-Channel MOSFET


Power MOS 8™ is a high speed, high voltage N-channel switch-mode power MOSFET. A proprietary planar stripe design yields excellent reliability and manufacturability. Low switching loss is achieved with low input capacitance and ultra low  $C_{rss}$  "Miller" capacitance. The intrinsic gate resistance and capacitance of the poly-silicon gate structure help control slew rates during switching, resulting in low EMI and reliable paralleling, even when switching at very high frequency. Reliability in flyback, boost, forward, and other circuits is enhanced by the high avalanche energy capability.



**APT4M120K**  
Single die MOSFET



### FEATURES

- Fast switching with low EMI/RFI
- Low  $R_{DS(on)}$
- Ultra low  $C_{rss}$  for improved noise immunity
- Low gate charge
- Avalanche energy rated
- RoHS compliant 

### TYPICAL APPLICATIONS

- PFC and other boost converter
- Buck converter
- Two switch forward (asymmetrical bridge)
- Single switch forward
- Flyback
- Inverters

### Absolute Maximum Ratings

Symbol	Parameter	Ratings	Unit
$I_D$	Continuous Drain Current @ $T_C = 25^\circ\text{C}$	5	A
	Continuous Drain Current @ $T_C = 100^\circ\text{C}$	3	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	15	
$V_{GS}$	Gate-Source Voltage	±30	V
$E_{AS}$	Single Pulse Avalanche Energy <sup>②</sup>	310	mJ
$I_{AR}$	Avalanche Current, Repetitive or Non-Repetitive	2	A

### Thermal and Mechanical Characteristics

Symbol	Characteristic	Min	Typ	Max	Unit
$P_D$	Total Power Dissipation @ $T_C = 25^\circ\text{C}$			225	W
$R_{\theta JC}$	Junction to Case Thermal Resistance			0.56	$^\circ\text{C/W}$
$R_{\theta CS}$	Case to Sink Thermal Resistance, Flat, Greased Surface		0.11		
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55		150	$^\circ\text{C}$
$T_L$	Soldering Temperature for 10 Seconds (1.6mm from case)			300	
$W_T$	Package Weight		0.07		oz
			1.9		g
Torque	Mounting Torque ( TO-220 Package), 4-40 or M3 screw			10	in·lbf
				1.1	N·m

# Static Characteristics

$T_J = 25^\circ\text{C}$  unless otherwise specified

APT4M120K

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$V_{BR(DSS)}$	Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	1200			V
$\Delta V_{BR(DSS)}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	Reference to $25^\circ\text{C}, I_D = 250\mu A$		1.41		V/ $^\circ\text{C}$
$R_{DS(on)}$	Drain-Source On Resistance <sup>③</sup>	$V_{GS} = 10V, I_D = 2A$		3.12	3.8	$\Omega$
$V_{GS(th)}$	Gate-Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 0.5mA$	3	4	5	V
$\Delta V_{GS(th)}/\Delta T_J$	Threshold Voltage Temperature Coefficient			-10		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 1200V, T_J = 25^\circ\text{C}$ $V_{GS} = 0V, T_J = 125^\circ\text{C}$			100	$\mu A$
$I_{GSS}$	Gate-Source Leakage Current	$V_{GS} = \pm 30V$			500	nA

# Dynamic Characteristics

$T_J = 25^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$g_{fs}$	Forward Transconductance	$V_{DS} = 50V, I_D = 2A$		4.5		S
$C_{iss}$	Input Capacitance	$V_{GS} = 0V, V_{DS} = 25V$ $f = 1MHz$		1385		pF
$C_{rss}$	Reverse Transfer Capacitance			17		
$C_{oss}$	Output Capacitance			100		
$C_{o(cr)}^{④}$	Effective Output Capacitance, Charge Related	$V_{GS} = 0V, V_{DS} = 0V \text{ to } 800V$		40		
$C_{o(er)}^{⑤}$	Effective Output Capacitance, Energy Related			20		
$Q_g$	Total Gate Charge	$V_{GS} = 0 \text{ to } 10V, I_D = 2A,$ $V_{DS} = 600V$		43		nC
$Q_{gs}$	Gate-Source Charge			7		
$Q_{gd}$	Gate-Drain Charge			20		
$t_{d(on)}$	Turn-On Delay Time	<b>Resistive Switching</b> $V_{DD} = 800V, I_D = 2A$ $R_G = 4.7\Omega^{⑥}, V_{GG} = 15V$		7.4		ns
$t_r$	Current Rise Time			4.4		
$t_{d(off)}$	Turn-Off Delay Time			24		
$t_f$	Current Fall Time			6.9		

# Source-Drain Diode Characteristics

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
$I_S$	Continuous Source Current (Body Diode)	MOSFET symbol showing the integral reverse p-n junction diode (body diode)			5	A
$I_{SM}$	Pulsed Source Current (Body Diode) <sup>①</sup>				15	
$V_{SD}$	Diode Forward Voltage	$I_{SD} = 2A, T_J = 25^\circ\text{C}, V_{GS} = 0V$			1.3	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 2A, V_{DD} = 100V^{②}$ $di_{SD}/dt = 100A/\mu s, T_J = 25^\circ\text{C}$		1150		ns
$Q_{rr}$	Reverse Recovery Charge			16		$\mu C$
$dv/dt$	Peak Recovery dv/dt	$I_{SD} \leq 2A, di/dt \leq 1000A/\mu s, V_{DD} = 800V,$ $T_J = 125^\circ\text{C}$			10	V/ns

① Repetitive Rating: Pulse width and case temperature limited by maximum junction temperature.

② Starting at  $T_J = 25^\circ\text{C}, L = 155.0mH, R_G = 25\Omega, I_{AS} = 2A$ .

③ Pulse test: Pulse Width < 380 $\mu s$ , duty cycle < 2%.

④  $C_{o(cr)}$  is defined as a fixed capacitance with the same stored charge as  $C_{OSS}$  with  $V_{DS} = 67\%$  of  $V_{(BR)DSS}$ .

⑤  $C_{o(er)}$  is defined as a fixed capacitance with the same stored energy as  $C_{OSS}$  with  $V_{DS} = 67\%$  of  $V_{(BR)DSS}$ . To calculate  $C_{o(er)}$  for any value of  $V_{DS}$  less than  $V_{(BR)DSS}$ , use this equation:  $C_{o(er)} = -6.30E-8/V_{DS}^2 + 7.65E-9/V_{DS} + 1.09E-11$ .

⑥  $R_G$  is external gate resistance, not including internal gate resistance or gate driver impedance. (MIC4452)

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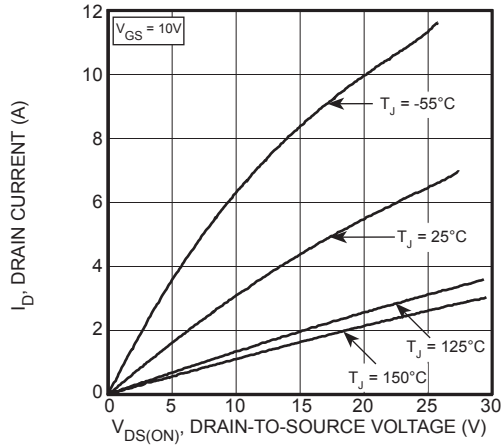


Figure 1, Output Characteristics

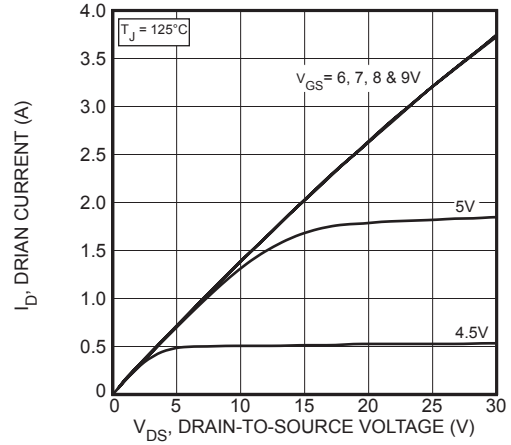


Figure 2, Output Characteristics

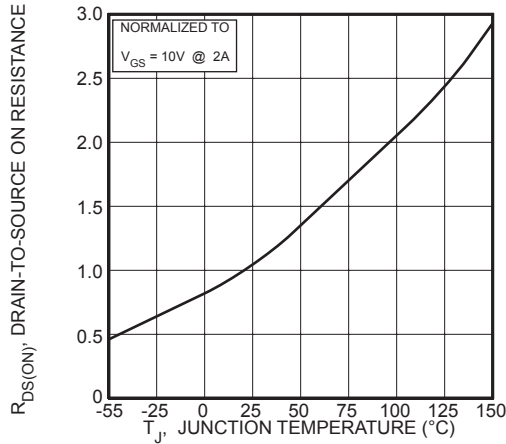


Figure 3,  $R_{DS(ON)}$  vs Junction Temperature

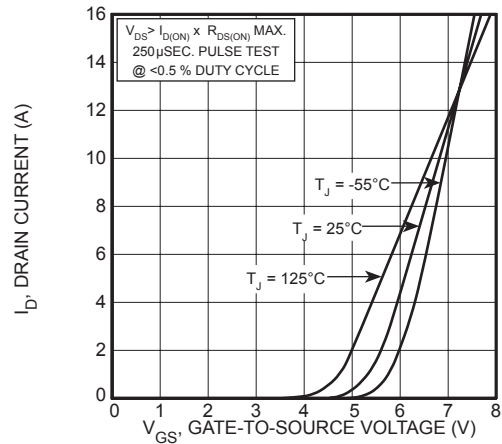


Figure 4, Transfer Characteristics

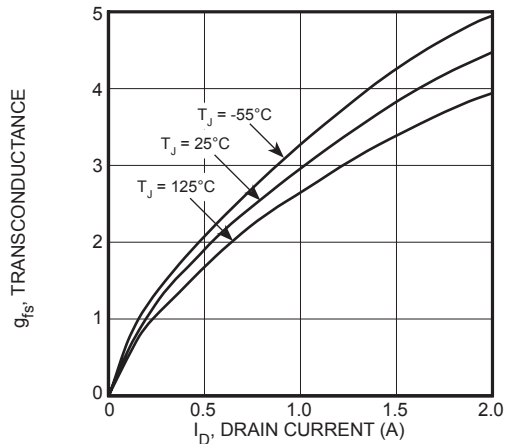


Figure 5, Gain vs Drain Current

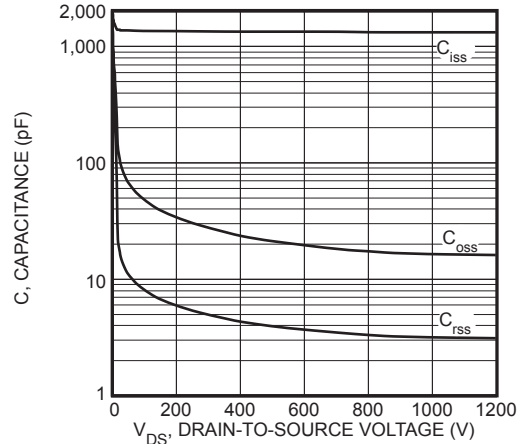


Figure 6, Capacitance vs Drain-to-Source Voltage

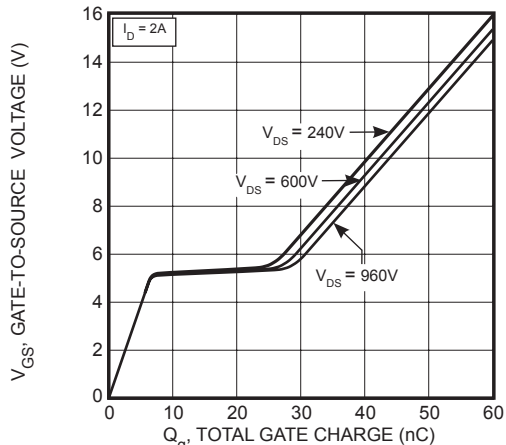


Figure 7, Gate Charge vs Gate-to-Source Voltage

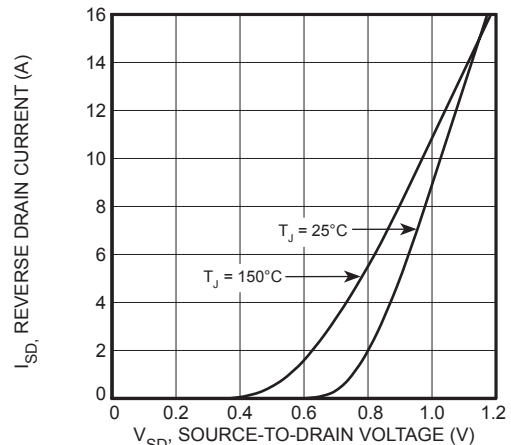
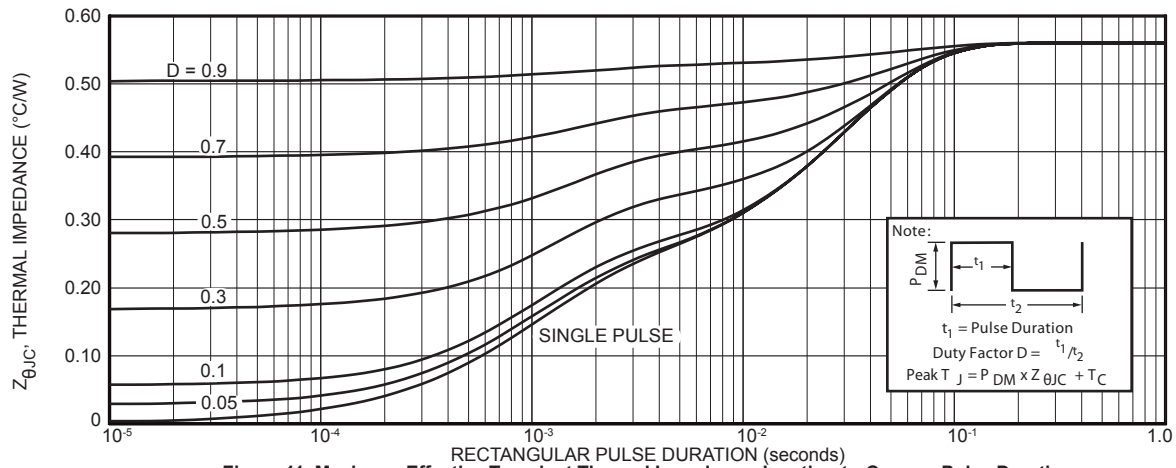
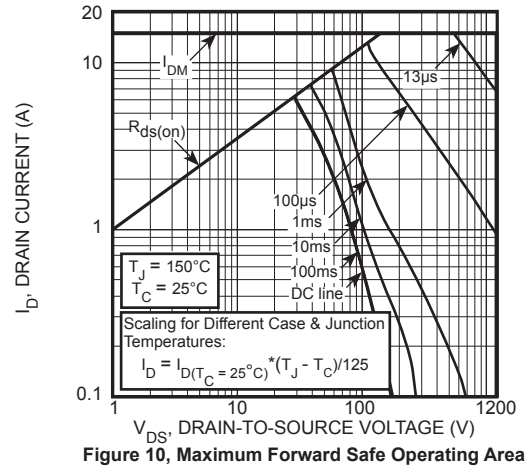
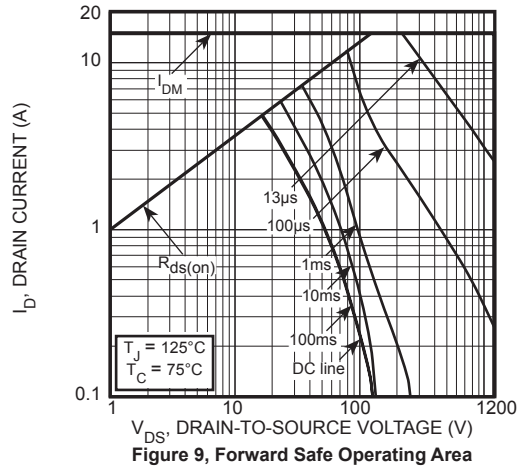
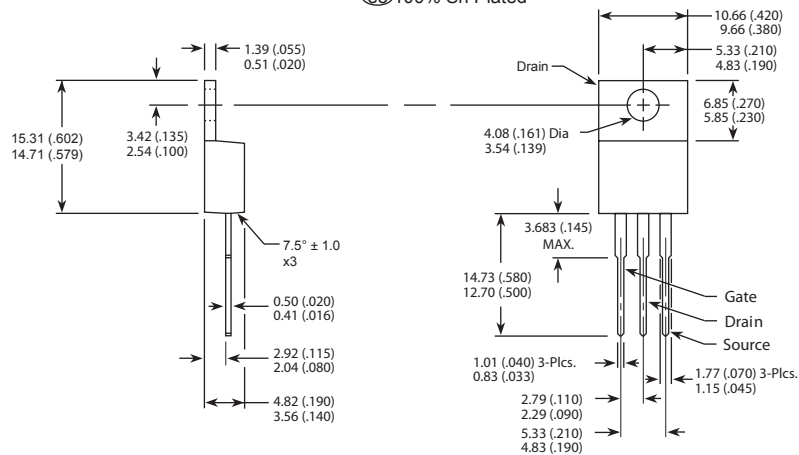


Figure 8, Reverse Drain Current vs Source-to-Drain Voltage



### TO-220 (K) Package Outline

Ⓢ100% Sn Plated



Dimensions in Millimeters and (Inches)

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