Power MOS 7® is a new generation of low loss, high voltage, N-Channel enhancement mode power MOSFETS. Both conduction and switching losses are addressed with Power MOS 7® by significantly lowering $R_{DS(ON)}$ and $Q_g$. Power MOS 7® combines lower conduction and switching losses along with exceptionally fast switching speeds inherent with Microsemi’s patented metal gate structure.

- Lower Input Capacitance
- Increased Power Dissipation
- Lower Miller Capacitance
- Easier To Drive
- Lower Gate Charge, $Q_g$
- TO-247 or Surface Mount D³PAK Package

MAXIMUM RATINGS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Parameter</th>
<th>APT1201R4B_SFLL</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{DSS}$</td>
<td>Drain-Source Voltage</td>
<td>1200</td>
<td>Volts</td>
</tr>
<tr>
<td>$I_D$</td>
<td>Continuous Drain Current @ $T_C = 25°C$</td>
<td>9</td>
<td>Amps</td>
</tr>
<tr>
<td>$I_{DM}$</td>
<td>Pulsed Drain Current (1)</td>
<td>36</td>
<td></td>
</tr>
<tr>
<td>$V_{GS}$</td>
<td>Gate-Source Voltage Continuous</td>
<td>±30</td>
<td>Volts</td>
</tr>
<tr>
<td>$V_{GSM}$</td>
<td>Gate-Source Voltage Transient</td>
<td>±40</td>
<td></td>
</tr>
<tr>
<td>$P_D$</td>
<td>Total Power Dissipation @ $T_C = 25°C$</td>
<td>300</td>
<td>Watts</td>
</tr>
<tr>
<td>$T_J,T_{STG}$</td>
<td>Operating and Storage Junction Temperature Range</td>
<td>-55 to 150</td>
<td>°C</td>
</tr>
<tr>
<td>$T_L$</td>
<td>Lead Temperature: 0.063&quot; from Case for 10 Sec.</td>
<td>300</td>
<td>Amps</td>
</tr>
<tr>
<td>$I_{AR}$</td>
<td>Avalanche Current (1) (Repetitive and Non-Repetitive)</td>
<td>9</td>
<td>mJ</td>
</tr>
<tr>
<td>$E_{AR}$</td>
<td>Repetitive Avalanche Energy (1)</td>
<td>30</td>
<td></td>
</tr>
<tr>
<td>$E_{AS}$</td>
<td>Single Pulse Avalanche Energy (1)</td>
<td>1210</td>
<td></td>
</tr>
</tbody>
</table>

STATIC ELECTRICAL CHARACTERISTICS

<table>
<thead>
<tr>
<th>Symbol</th>
<th>Characteristic / Test Conditions</th>
<th>MIN</th>
<th>TYP</th>
<th>MAX</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>$BVDSS$</td>
<td>Drain-Source Breakdown Voltage ($V_{GS} = 0V$, $I_D = 250\mu A$)</td>
<td>1200</td>
<td></td>
<td></td>
<td>Volts</td>
</tr>
<tr>
<td>$R_{DS(on)}$</td>
<td>Drain-Source On-State Resistance (2) ($V_{GS} = 10V$, $I_D = 4.5A$)</td>
<td>1.50</td>
<td></td>
<td></td>
<td>Ohms</td>
</tr>
<tr>
<td>$I_{DSS}$</td>
<td>Zero Gate Voltage Drain Current ($V_{DS} = 1200V$, $V_{GS} = 0V$)</td>
<td>250</td>
<td></td>
<td></td>
<td>µA</td>
</tr>
<tr>
<td></td>
<td>Zero Gate Voltage Drain Current ($V_{DS} = 960V$, $V_{GS} = 0V$, $T_C = 125°C$)</td>
<td>1000</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>$I_{GSS}$</td>
<td>Gate-Source Leakage Current ($V_{GS} = ±30V$, $V_{DS} = 0V$)</td>
<td>±100</td>
<td></td>
<td></td>
<td>nA</td>
</tr>
<tr>
<td>$V_{GS(th)}$</td>
<td>Gate Threshold Voltage ($V_{DS} = V_{GS}$, $I_D = 1mA$)</td>
<td>3</td>
<td>5</td>
<td></td>
<td>Volts</td>
</tr>
</tbody>
</table>

⚠️ CAUTION: These Devices are Sensitive to Electrostatic Discharge. Proper Handling Procedures Should Be Followed.
### Dynamic Characteristics

#### Symbol | Characteristic | Test Conditions | MIN | TYP | MAX | UNIT
---|---|---|---|---|---|---
C Iss | Input Capacitance | \( V_{GS} = 0V \)
Coss | Output Capacitance | \( V_{DS} = 25V \)
C rss | Reverse Transfer Capacitance | \( f = 1 \text{ MHz} \)
Q g | Total Gate Charge \(\theta\) | \( V_{GS} = 10V \)
Q gs | Gate-Source Charge | \( V_{DD} = 600V \)
Q gdd | Gate-Drain ("Miller") Charge | \( I_D = 9A @ 25°C \)
t(on) | Turn-on Delay Time | \( V_{GS} = 15V \)
t | Rise Time | \( V_{DD} = 600V \)
t(off) | Turn-off Delay Time | \( I_D = 9A @ 25°C \)
tf | Fall Time | \( R_g = 1.62\Omega \)
E on | Turn-on Switching Energy \(\theta\) \( V_{DD} = 800V, V_{GS} = 15V \)
E off | Turn-off Switching Energy | \( \text{XX} \)
E on | Turn-on Switching Energy \(\theta\) \( V_{DD} = 800V, V_{GS} = 15V \)
E off | Turn-off Switching Energy | \( 18 \)

#### Source-Drain Diode Ratings and Characteristics

#### Symbol | Characteristic | Test Conditions | MIN | TYP | MAX | UNIT
---|---|---|---|---|---|---
l_s | Continuous Source Current (Body Diode) | | 9 | | | Amps
l_sm | Pulsed Source Current \(\theta\) (Body Diode) | | 36 | | | Amps
V SD | Diode Forward Voltage \(\theta\) \( V_{GS} = 0V, I_S = -I_D 9A \) | | 1.3 | | | Volts
dv/dt | Peak Diode Recovery \(dv/dt\) \(\theta\) | | 18 | | | V/ns
t_rr | Reverse Recovery Time \( I_S = -I_D 9A, dv/dt = 100A/\mu s \) | \( T_J = 25°C \)
| | | | 210 | | ns
| | | Reverse Recovery Charge \( I_S = -I_D 9A, dv/dt = 100A/\mu s \) | \( T_J = 125°C \)
| | | | 710 | | \mu C
I RMS | Peak Recovery Current \( I_S = -I_D 9A, dv/dt = 100A/\mu s \) | \( T_J = 25°C \)
| | | | 10 | | Amps

#### Thermal Characteristics

#### Symbol | Characteristic | MIN | TYP | MAX | UNIT
---|---|---|---|---|---
R JUC | Junction to Case | | 0.42 | | \degree C/W
R JUA | Junction to Ambient | | | 40 | \degree C/W

---

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Pulse Test: Pulse width < 380 \( \mu \)s, Duty Cycle < 2%
3. See MIL-STD-750 Method 3471
4. Starting \( T_J = 25°C, L = 29.9mH, R_g = 25\Omega \), Peak \( I_L = 9A \)
5. \( dv/dt \) numbers reflect the limitations of the test circuit rather than the device itself. \( I_S \leq -I_D 9A, dv/dt \leq 700A/\mu s \), \( V_R \leq 1200 \text{ V}, T_J \leq 150°C \)
6. Eon includes diode reverse recovery. See figures 18, 20.

Microsemi reserves the right to change, without notice, the specifications and information contained herein.
Typical Performance Curves

**FIGURE 2, TRANSIENT THERMAL IMPEDANCE MODEL**

$R_{GS} > I_D (ON) \times R_{DS(ON)} \text{MAX.}$

250μSEC. PULSE TEST

@ <0.5 % DUTY CYCLE

**FIGURE 3, LOW VOLTAGE OUTPUT CHARACTERISTICS**

**FIGURE 4, TRANSFER CHARACTERISTICS**

**FIGURE 5, $R_{DS(ON)}$ vs DRAIN CURRENT**

$V_{GS} = 10V$

$V_{GS} = 20V$

$V_{GS} = 15, 10 & 8V$

**FIGURE 6, MAXIMUM DRAIN CURRENT vs CASE TEMPERATURE**

**FIGURE 7, BREAKDOWN VOLTAGE vs TEMPERATURE**

**FIGURE 8, ON-RESISTANCE vs TEMPERATURE**

**FIGURE 9, THRESHOLD VOLTAGE vs TEMPERATURE**

$T_J = +125°C$

$T_J = +25°C$

$T_J = -55°C$

$V_{DS} > I_D (ON) \times R_{DS(ON) \text{MAX.}} 250μSEC. \text{ PULSE TEST} \ @ <0.5 \% \text{ DUTY CYCLE}$
FIGURE 10, MAXIMUM SAFE OPERATING AREA

FIGURE 11, CAPACITANCE vs DRAIN-TO-SOURCE VOLTAGE

FIGURE 12, GATE CHARGES vs GATE-TO-SOURCE VOLTAGE

FIGURE 13, SOURCE-DRAIN DIODE FORWARD VOLTAGE

FIGURE 14, DELAY TIMES vs CURRENT

FIGURE 15, RISE AND FALL TIMES vs CURRENT

FIGURE 16, SWITCHING ENERGY vs CURRENT

FIGURE 17, SWITCHING ENERGY vs. GATE RESISTANCE