ARF300 – ARF301
In
N-N and N-P Half Bridge RF Generators
with Pulse and Sine Drive

George J. Krausse
Microsemi Corp. RF Power Products Group
405 SW Columbia St.
Bend, OR 97702 USA
gkrausse@microsemi.com

and

Richard Frey, P.E. K4XU
Applications Engineering
Microsemi Corp. RF Power Products Group
405 SW Columbia St.
Bend, Oregon 97702 USA
dfrey@microsemi.com

Introduction

The following Application Note is a SPICE Model Tutorial on Half Bridge (HB) Topologies and their relative performance with matched and reactive loads. It is based on new Large Signal RF Spice Models developed at Microsemi PPG. The circuits include all significant strays. This format allows us to explore operational elements that are exceedingly difficult, if not impossible, to measure accurately on a Bench Prototype Circuit. In addition, it provides a valuable tool for the understanding of Circuit Operation under varying load conditions.

Circuit Parameters, for each configuration, have been adjusted for the highest efficiency and highest power output while limiting the MOSFETs junction temperature to a maximum of ≈ 100°C and limiting the Drain to Source Margin to a positive number or zero. These are defined as the boundary conditions. This term will be referenced repeatedly in the text.

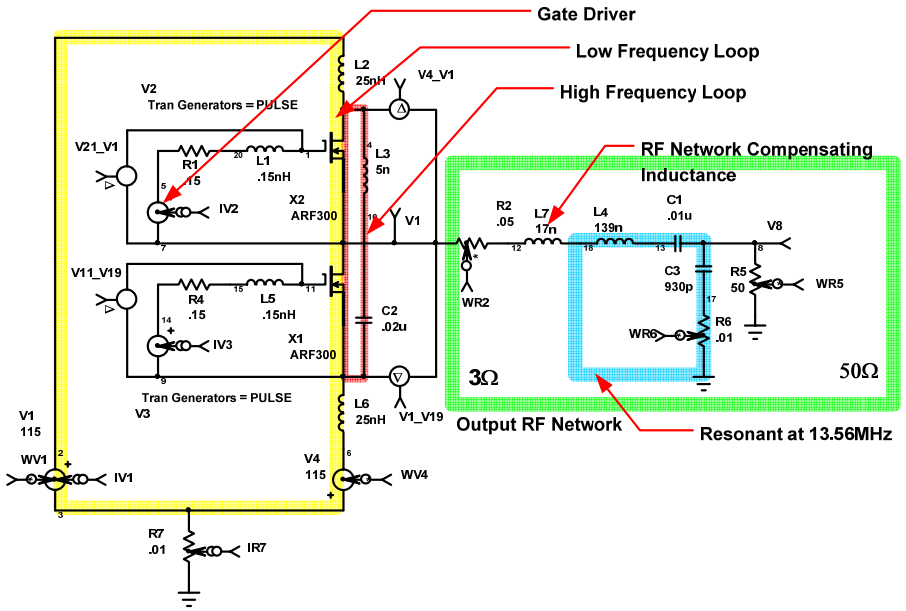
The Circuit Parameters that we will adjust are Load Matching MOSFET Drain to Load, Pulse Width for Pulse Drive, Amplitude and DC Offset for Sine Drive and the RF Network Compensating Inductance. Using this process we will cover circuit performance for N-N Channel, N-P Channel Half-Bridges with both Square Wave Drive and Sine Wave Drive.

It should be noted that, for clarity, each configuration section is self contained. This results in the duplication of material, however it also facilitates the presentation of information.

N Channel–N Channel Half Bridge

Figure 1 illustrates a classical N Channel-N Channel Half Bridge RF Generator. The High Side Switch X2 and the Low Side Switch X1 form the two active devices in the Half Bridge. X1 and X2 commutate in an alternating fashion providing a pseudo Square Wave drive to the input of the RF network, at V1. The RF network provides an impedance match from the Drain Impedance of X1, X2 of about 3Ω to the 50Ω load. This L Match network is also resonant at 13.56MHz so that the output is a Sine Wave.

This is a resonant network and only performs the translation at the design frequency. The common design formulas account only for a resistive source and load. Since the output devices have parasitic capacitance, after the network is designed, the series L must be adjusted to account for this capacitance. A value of L ≈ 10% to 25% higher than the calculated is typically required to bring the network to full efficiency, illustrated in Figure 1 as L7.



Circuit Performance	
Vsupply	±150V
Pout	2238W
Pin	2499W
PLoss	261W
Eff	89.4%
Pulse Gate Drive	PW=22ns
Ths	45°C
Tj X2	100°C
TjX1	100°C
Vds Margin	270V
Drain Z=3Ω	Out Z=50Ω

Figure 1 N-N Channel Half Bridge

Figure 1 illustrates an N-N Channel Half Bridge circuit topology. The circuit contains two current loops. A low frequency loop is highlighted in yellow. The high frequency loop is highlighted in red. These loops are illustrated with near-minimum stray inductance. Great care should be taken to achieve inductance values near the illustrated values. If we allow L2 and L6 to reach 100nH or greater, performance will be degraded. The inductance of the inner loop, L3, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics.

At 13.56MHz the period is 73.75ns and a one-half cycle time is 36.87ns. However, we have set the Gate Pulse Width at 26ns. This allows for two design considerations. The first of these is a timing margin to prevent cross conduction in X1 and X2. Cross conduction would be damaging to the devices and greatly reduce efficiency. The second consideration is to allow the charge and discharge of L7 which increases efficiency, as discussed for Figure 1.

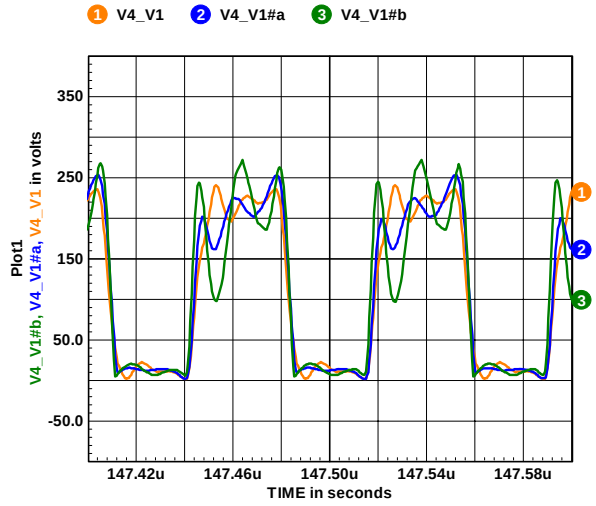


Figure 2 Variations in L3

The inductance of the inner loop, L3, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics. Figure 2 illustrates this variation with L2 and L6 held at 25nH. In Trace (1) L3 is 5nH, the ring frequency is 79.3MHz. In Trace (2) L3 is 25nH, the ring frequency is 74.6MHz. In Trace (3) L3 is 50nH and the ring frequency is 55.5MHz. The higher the ring frequency and the lower the amplitude, the easier it will be to suppress this harmonic. Trace (3) is a problem.

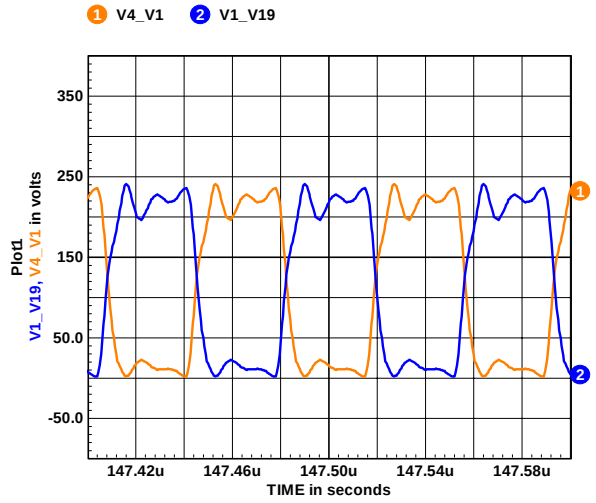


Figure 3 Drain Wave Forms N-N HB

Figure 3 illustrates the two drain wave forms in the N-N Half Bridge. Trace (1) is a plot of the Source to Drain wave form on X2. Trace (2) is a plot of the Source to Drain wave form on X1. From this plot we see a low ring amplitude with a peak-to-peak frequency of about 80.0MHz. No cross conduction is present. If the devices were cross conducting, the first positive going ring would be more pronounced and the damping would be less.

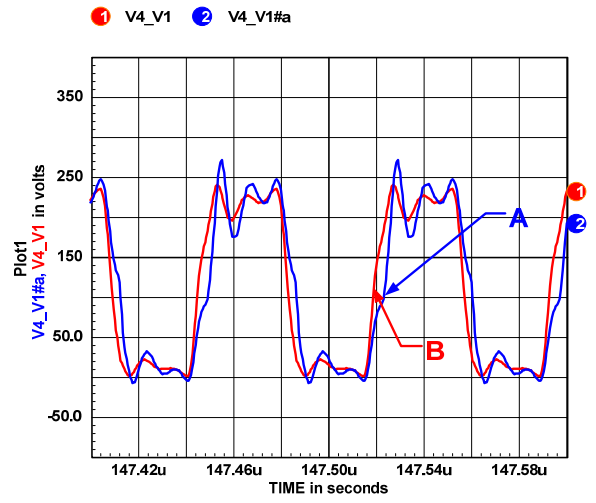


Figure 4 Improved Efficiency due to L7

In Figure 4 we see an overlay of the Drain Waveform for X2 with the inductor L7 (17nH) in place (B) and with L7 removed (A).The difference in Markers A and B illustrate the energy saved by the addition of L7, this accounts for about 3% improvement in efficiency, 35°C reduction in junction temperature, and a more damped drain wave form.

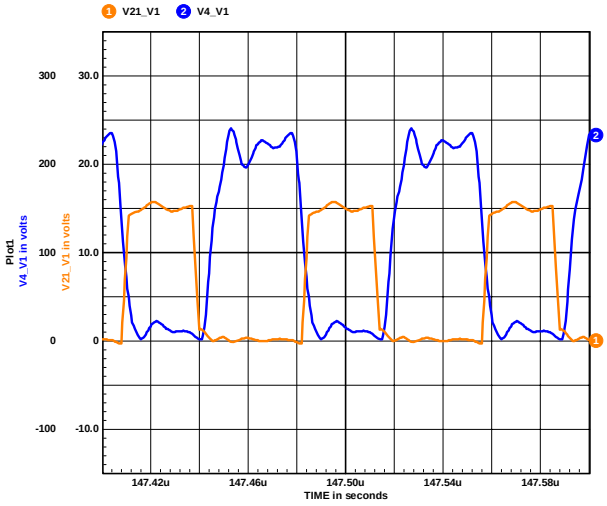


Figure 5 Drain and Gate Wave Forms N-N HB

Figure 5 illustrates Trace (1), the X2 Gate Drive wave form in the N-N Half Bridge. Trace (2) is a plot of the Drain wave form on X2. The Gate Drive wave form has been adjusted for highest efficiency and highest power while limiting the MOSFETs junction to a maximum of ≈ 100°C, and not exceeding the boundary conditions. Circuit settings and performance are shown in the table to the right of Figure 1.

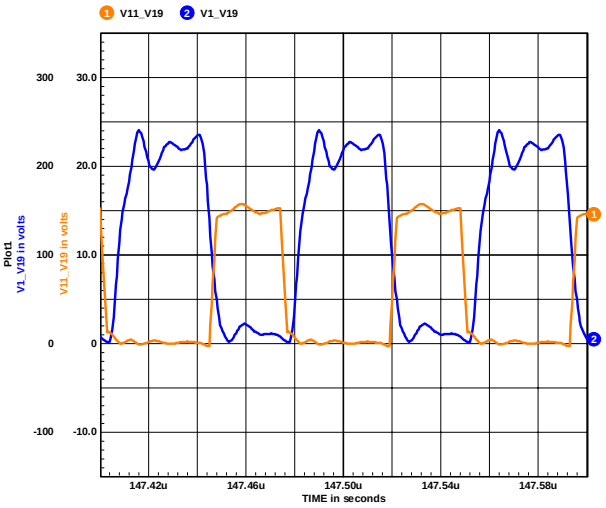


Figure 6 Drain and Gate Wave Forms N-N HB

Figure 6 illustrates Trace (1), the X1 Gate Drive wave form in the N-N Half Bridge. Trace (2) is a plot of the Drain wave form on X1. The Gate Drive wave form has been adjusted for highest efficiency and highest power while not exceeding the boundary conditions.

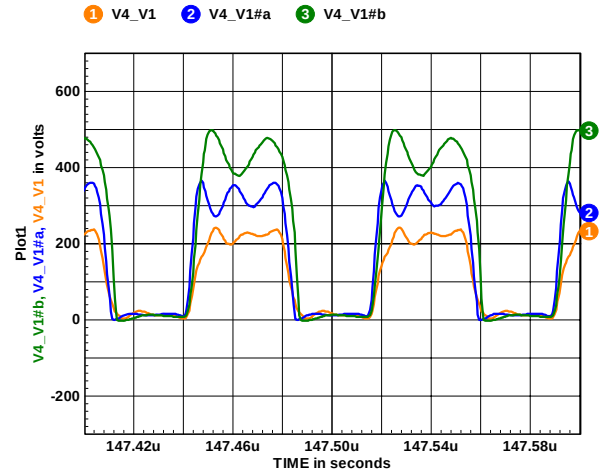


Figure 7 Drain Wave Forms with L2, L3 and L6 Variations

In Figure 7, Trace 1 is the Drain Wave Form of the preferred configuration, also shown in column 2 of Table 1. As we increase the values of the Stray Inductive Terms L2, L3 and L6, we decrease power output and efficiency. Vds Margin is only slightly affected. Trace 2 performance is shown in Table 1 column 3, and Trace 3 performance is shown in Table 1 column 4.

Shown in Table 1 are a set of values for variations in the three stray inductive terms, L2, L3 and L6 and the impact on circuit performance. If we allow L2 and L6 to reach 100nH or greater, performance will be degraded. Power output capability and efficiency are reduced significantly. The inductance of the inner loop, L3, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics.

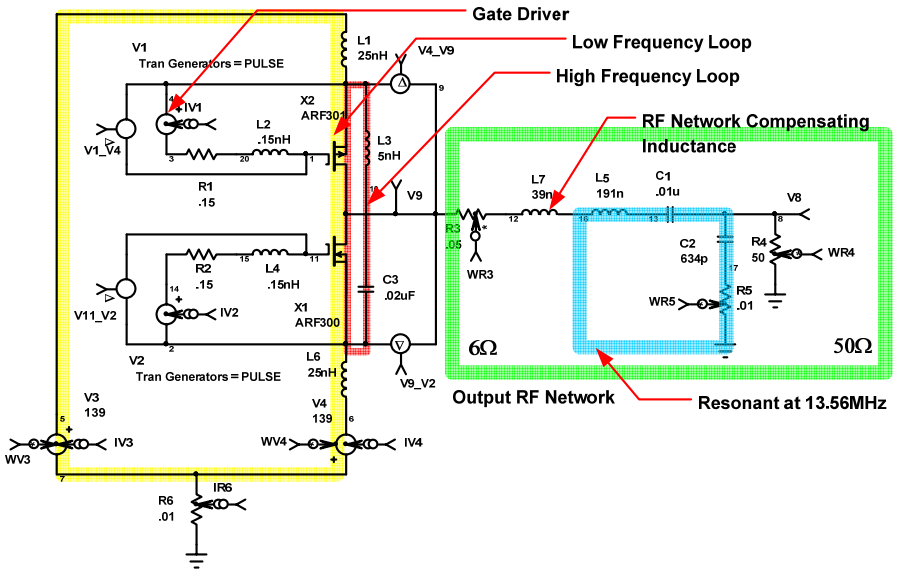
Table 1 L2, L3, L6 Variations

L2, L3, L6	L2=25nH L3=5nH L6=25nH	L2=100nH L3=20nH L6=100nH	L2=250nH L3=50nH L6=250nH
Vsupply	± 115V	± 173V	± 235V
Pout	2238W	1856W	816W
Pin	2499W	2116W	1060W
PLoss	261W	260W	244W
Eff	89.4%	87.7%	77.0%
Pw	26ns	26ns	26ns
Ths	45°C	45°C	45°C
Tj X2	100°C	100°C	96°C
TjX1	100°C	100°C	96°C
Vds Margin	270V	139V	5V

For Columns 2, 3 and 4, Circuit Parameters have been adjusted for the highest efficiency and highest power output while not exceeding the boundary conditions as stated in the Introduction.

N Channel–P Channel Half Bridge

Figure 8 illustrates a classical N Channel-P Channel Half Bridge RF Generator. The Positive Supply Switch X2 and the Negative Supply Switch X1 form the two key active devices in the Half Bridge. As in Figure 1, X1 and X2 commutate in an alternating fashion providing a pseudo Square Wave drive to the input of the RF network, V9. The RF network provides an impedance match from the Drain Impedance of X1, X2 of about 6Ω to 50Ω of the load. This L Match network is also resonate at 13.56MHz so that the output is a Sine Wave.



Circuit Performance	
Vsupply	±139V
Pout	1506W
Pin	1679W
PLoss	173W
Eff	89.8%
PW	22ns
Ths	45°C
Tj X2	100°C
TjX1	62°C
Vds Margin	222V
Drain Z=6Ω	Out Z=50Ω

Figure 8 N-P Channel Half Bridge

In Figure 8, a low frequency loop is highlighted in yellow. This loop is illustrated with near minimum stray inductance achievable. Great care should be taken to achieve these values. If we allow L2 and L6 to reach 100nH or greater, performance will be degraded. The inductance of the inner loop, L3, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics.

At 13.56MHz, the period is 73.75ns and a one half cycle time is 36.87ns. However, we have set the Gate Pulse Width at 22ns. This allows for two design considerations. The first of these is a margin to prevent cross conduction in X1 and X2. The second consideration is to allow the charge and discharge of L7 which will increase efficiency. Recall that the Gate Drive Pulse Width for the N-N Channel Half Bridge was 26ns vs. 22ns for the N-P Channel. The difference in the Gate Drive Pulse Width is due to the elevated tank impedance of the 6Ω reflected to the drain, this also requires that the L7 inductor be increased is size to 39nH.

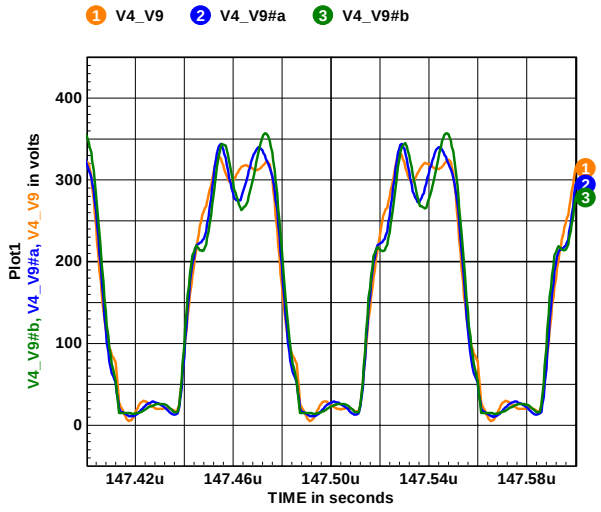


Figure 9 Variations in L3

The inductance of the inner loop, L3, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics. Figure 9 illustrates this variation with L1 and L6 held at 25nH. In Trace (1) L3 is 5nH and the ring frequency is 94.3MHz. In Trace (2) L3 is 25nH and the ring frequency is 64.1MHz. In Trace (3) L3 is 50nH and the ring frequency is 57.5MHz. The higher the ring frequency and the lower the amplitude, the easier it will be to suppress. Traces (2 and 3) are a problem. As the frequency approaches the fundamental, the purity of the output wave form will be compromised.

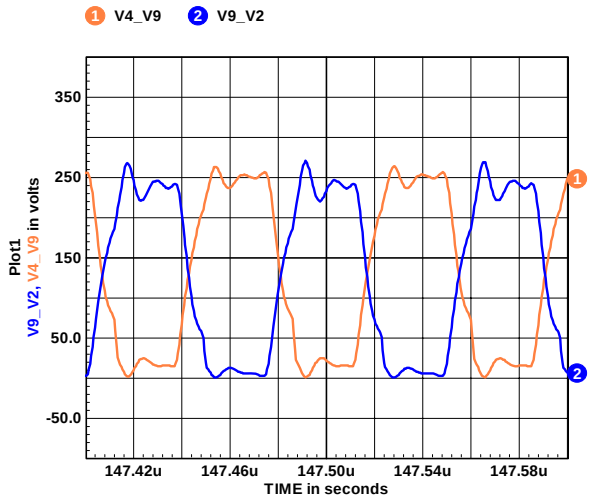


Figure 10 Drain Wave Forms N-N HB

Figure 10 illustrates the two Drain wave forms in the N-N Half Bridge. Trace (1) is a plot of the Source to Drain wave form on X2, (2) is a plot of the Source to Drain wave form on X1. From this plot we see a low ring amplitude with a peak-to-peak frequency of about 90MHz. No cross conduction is present. If the devices were cross conducting, the first positive going ring would be more pronounced and the dampening would be less.

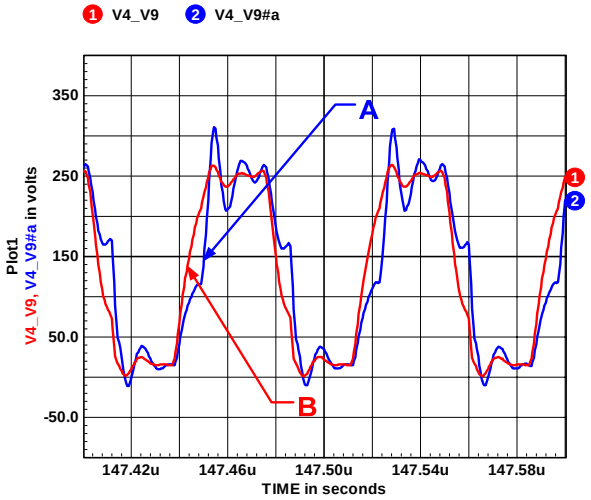


Figure 11 Improved Efficiency due to L7

In Figure 11 we see an overlay of the Drain Waveform for X2 with the inductor L7 (39nH) in place (B) and with L7 removed (A). No other circuit changes were made to the simulation. The difference in Markers A and B illustrate the energy saved by the addition of L7. This accounts for about 7% improvement in efficiency, 45°C reduction in junction temperature, and a more dampened drain wave form.

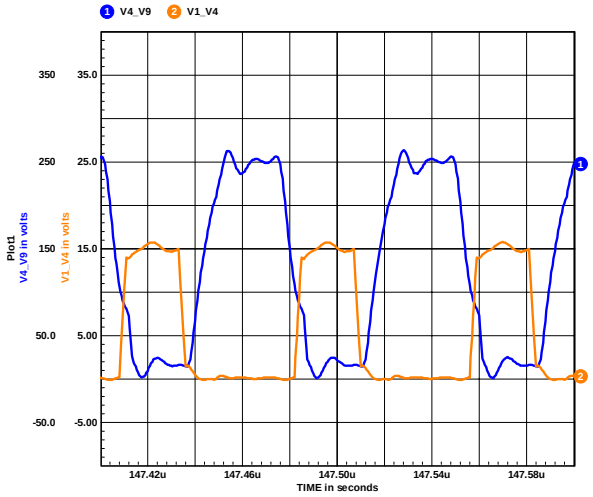


Figure 12 Drain and Gate Wave Forms N-P HB

Figure 12 illustrates Trace (1), the X1 Drain wave form in the N-P Half Bridge. Trace (2) is a plot of the Gate Drive wave form on the Gate of X1. The Pulse wave form has been adjusted for highest efficiency and highest power while not exceeding the boundary conditions, PW= 22ns.

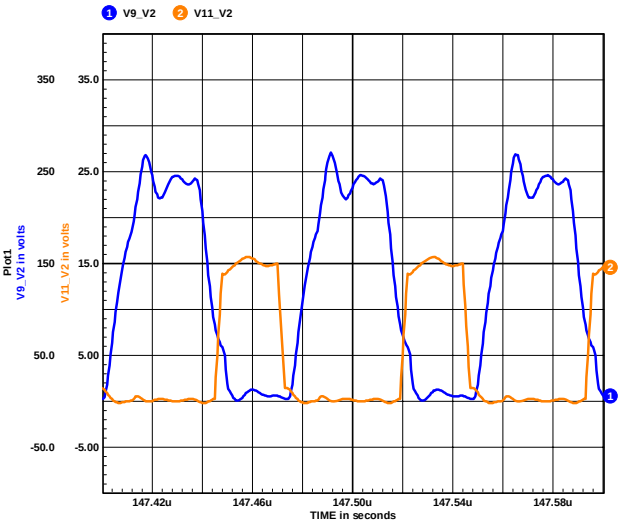


Figure 13 Drain Wave Forms N-P Low Side

Figure 13 illustrates Trace (2), the X1 Drain wave form in the N-P Half Bridge. Trace (1) is a plot of the Gate Drive wave form on the Gate of X1. The Pulse wave form has been adjusted for highest efficiency and highest power while not exceeding the boundary conditions, PW= 22ns.

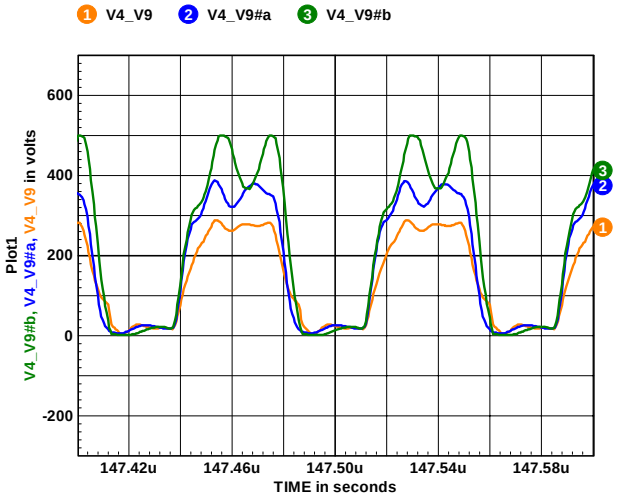


Figure 14 Drain Wave Forms with L1, L3, L6 Variations

In Figure 14, Trace 1 is the Drain Wave Form of the preferred configuration of Figure 8, also shown in column 2 of Table 2. As we increase the values of the Stray Inductive Terms L2, L3 and L6, we see an overall decrease in power output and Vds margin. efficiency is only slightly affected. Trace 2 performance is shown in Table 2 column 3 and Trace 3 performance is shown in Table 2 column 4. Trace (3) is a problem; Drain Voltage peak is at 500V. As the frequency approaches the fundamental, the purity of the output wave form will be compromised.

Shown in Table 2 are a set of values for variations in the three Stray Inductive terms, L1, L3 and L6 and the impact on circuit performance. If we allow L1 and L6 to reach 100nH or greater, performance will be degraded. Vds margin is reduced significantly. The inductance of the inner loop, L3, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics. Trace (2 and 3) are a problem.

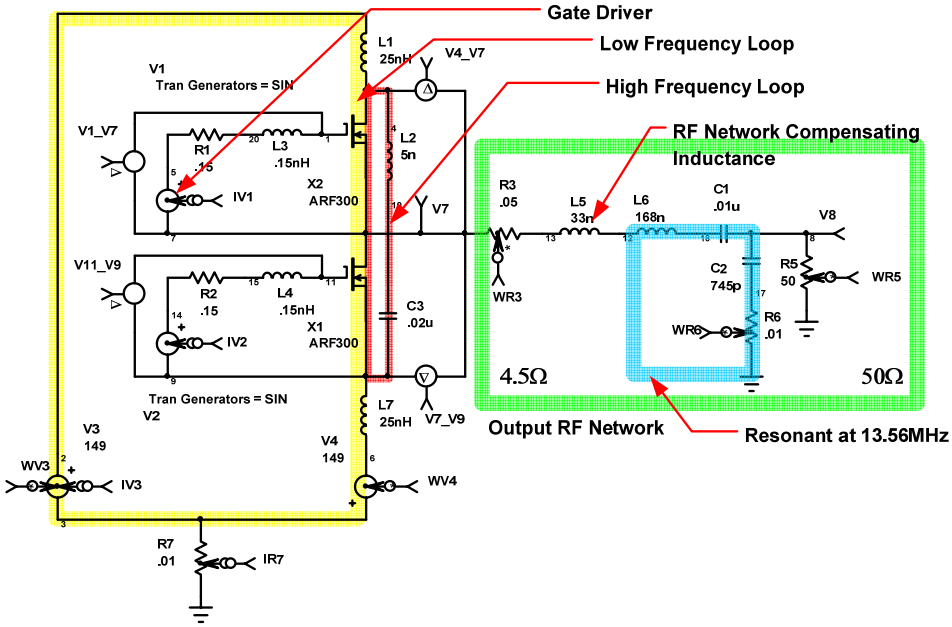
Table 2 L1, L3, L6 Variations

L2, L3, L6	L1=25nH L3=5nH L6=25nH	L1=100nH L3=20nH L6=100nH	L2=250nH L3=50nH L6=250nH
Vsupply	±139V	±184V	±230V
Pout	1506W	1672W	1008W
Pin	1679W	1843W	1131W
PLoss	173W	171W	123W
Eff	89.8%	90.7%	89.1%
Pw	22ns	22ns	22ns
Ths	45°C	45°C	45°C
Tj X2	100°C	100°C	84°C
TjX1	62°C	62°C	57°C
Vds Margin	215V	116V	3V

For Columns 2, 3 and 4 Circuit Parameters have been adjusted for the highest efficiency and highest power output while limiting the MOSFETs junction to a maximum of ≈ 100°C and limiting the Drain Supply voltage to a positive number or zero. These are defined in the Introduction as the boundary conditions.

N Channel–N Channel Half Bridge with Sine Wave Drive

Figure 15 illustrates a classical N-N Channel Half Bridge RF Generator. The Positive Supply Switch X2 and the Negative Supply Switch X1 form the two key active devices in the Half Bridge. X1 and X2 commutate in an alternating fashion providing a Sine Wave drive to the input of the RF network, V7. The RF network provides an impedance match from the Drain Impedance of X1, X2 of about 4.5Ω to 50Ω of the load. This L Match network is also resonate at 13.56MHz so that the output is a Sine Wave.



Circuit Performance	
Vsupply	±149V
Pout	2089W
Pin	2351W
PLoss	262W
Eff	88.8%
Sine Drive	Os=-5V Pk= 20V
Ths	45°C
Tj X2	100°C
TjX1	100°C
Vds Margin	202V
Drain Z=4.5Ω	Out Z=50Ω

Figure 15 N-N Channel Half Bridge

In Figure 15 a low frequency loop is highlighted in yellow. This loop is illustrated with near minimum stray inductance achievable. Great care should be taken to achieve these values. If we allow L1 and L7 to reach 100nH or greater, performance will be degraded. The inductance of the inner loop, L2, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics, see Figure 16 and text inset.

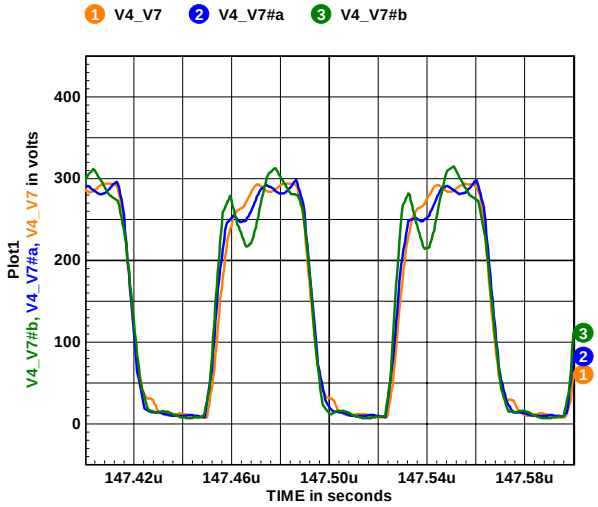


Figure 16 Variations in L2

The inductance of the inner loop, L2, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics. Figure 16 illustrates this variation with L1 and L6 held at 25nH. In Trace (1) L3 is 5nH and the ring frequency is 81.9MHz. In Trace (2) L3 is 25nH and the ring frequency is 76.9MHz. In Trace (3) L3 is 50nH and the ring frequency is 54.9MHz. The higher the ring frequency and the lower the amplitude the easier it will be to suppress. Trace (3) is a problem.

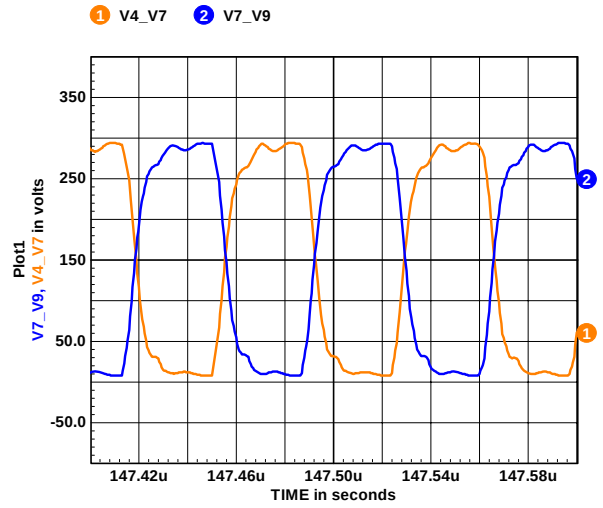


Figure 17 Drain Wave Forms N-N HB

Figure 17 illustrates the two Drain wave forms in the N-N Half Bridge, with Sine Wave Drive. Trace (1) is a plot of the Source to Drain wave form on X2. Trace (2) is a plot of the Source to Drain wave form on X1. From this plot we see a very low ring amplitude with a peak-to-peak frequency of about 113.6MHz. No cross conduction is present. If the devices were cross conducting the first positive going ring would be increasingly more pronounced.

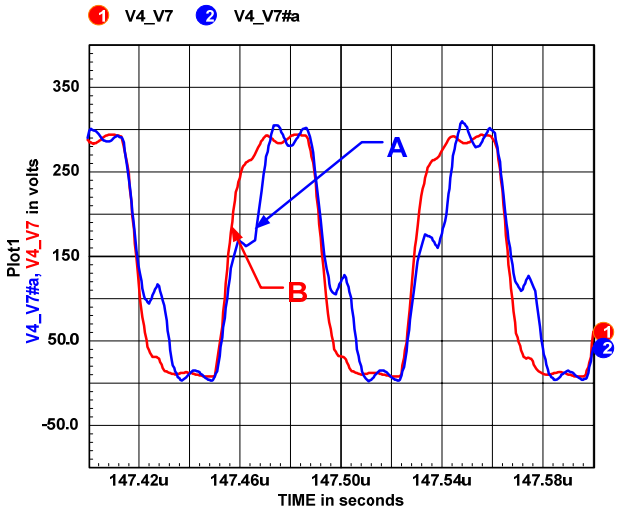


Figure 18 Improved Efficiency due to L5

In Figure 18 we see an overlay of the Drain Waveform for X2 Trace (1) with the inductor L7 (33nH) in place. In Trace (2) with L5 removed. The difference in Markers A and B illustrates the energy saved by the addition of L5. This accounts for about 7% improvement in efficiency, 45°C reduction in junction temperature, and a more dampened drain wave form.

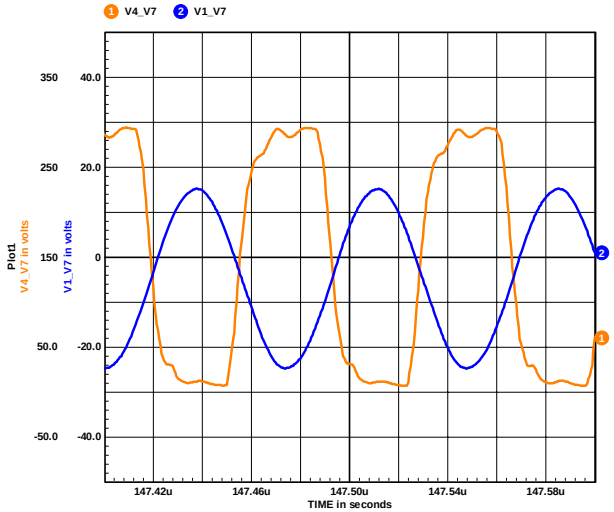


Figure 19 Drain and Gate Wave Forms N-N HB

Figure 19 illustrates Trace (1), the X2 Drain wave form in the N-N Half Bridge. Trace (2) is a plot of the Gate Drive wave form on the Gate of X2. The Sine Wave form has been adjusted for highest efficiency and highest power while not exceeding the boundary conditions, Sine 20Vpk, -5V offset.

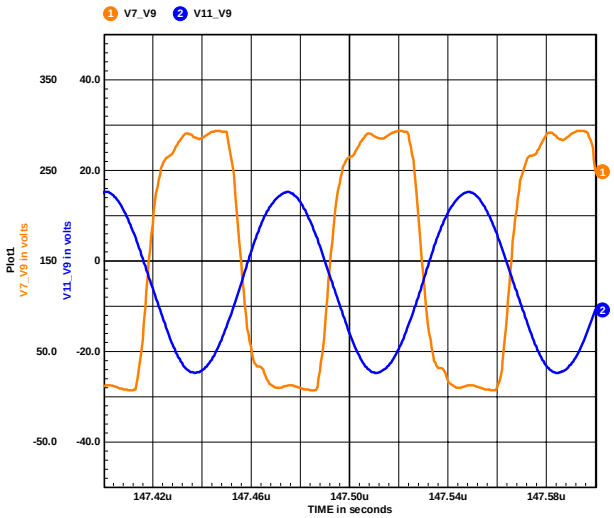


Figure 20 Drain Wave Forms N-N Low Side

Figure 20 illustrates Trace (2), the X1 Drain wave form in the N-N Half Bridge. Trace (1) is a plot of the Gate Drive wave form on the Gate of X1. The Sine wave form has been adjusted for highest efficiency and highest power while not exceeding the boundary conditions, Sine 20Vpk, -5V offset.

At 13.56MHz, the period is 73.746ns and one half cycle time is 36.873ns. However we have set the Gate Sine wave drive at -5V offset. This allows for two design considerations. The first of these is a margin to prevent cross conduction in X1 and X2. Cross conduction would be damaging to the devices and greatly reduce efficiency. The second consideration is to allow the charge and discharge of L5 which will increases efficiency, recall Figure 18.

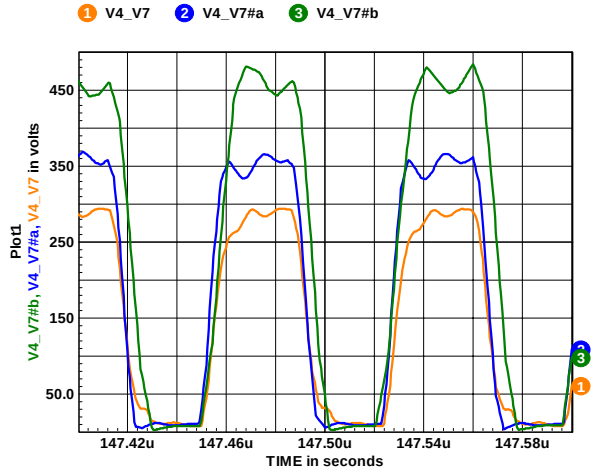


Figure 21 Drain Wave Forms with L1, L2, L7 Variations

In Figure 21 Trace 1 is the Drain Wave Form of the preferred configuration, also shown in column 2 of Table 2. As we increase the values of the Stray Inductive Terms L1, L2 and L7 we reduce power output, efficiency and Vds margin. Trace 2 performance is shown in Table 2 column 3 and Trace 3 performance is shown in Table 1 column 4. Note that Trace 3 in very near 500V.

Shown in Table 3 are a set of values for variations in the three Stray Inductive Terms, L1, L2 and L7 and the impact on circuit performance. If we allow L1 and L2 to reach 100nH or greater, performance will be degraded. Consequently the Drain Peak voltage will approach 500V and the circuit will have less voltage margin. In addition, power output capability will be reduced. The inductance of the inner loop, L2, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics.

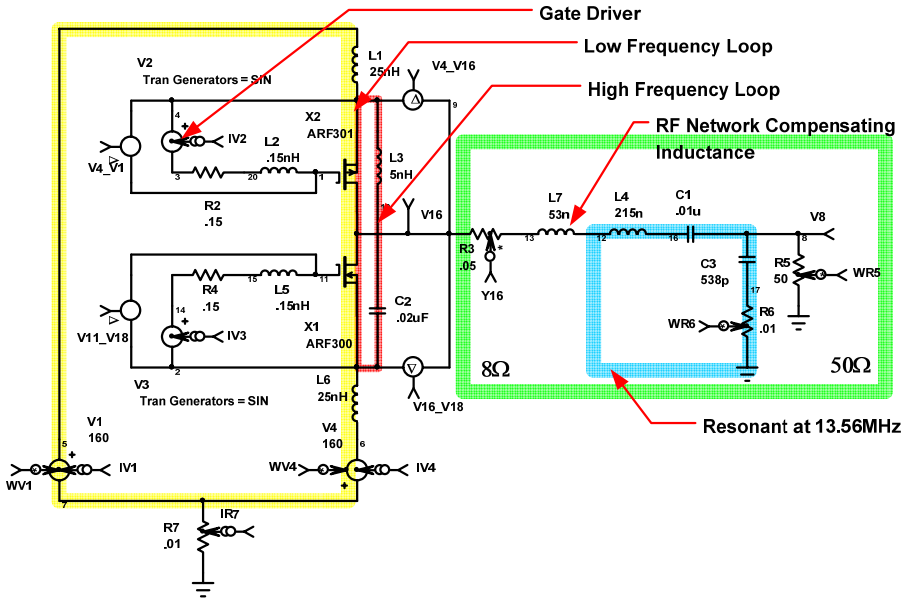
Table 3 L1, L2, L7 Variations

L2, L3, L6	L1=25nH L2=5nH L7=25nH	L1=100nH L2=20nH L7=100nH	L1=250nH L2=50nH L7=250nH
Vsupply	±149V	±187V	±249V
Pout	2089W	1578W	725W
Pin	2351W	1842W	988W
PLoss	262W	264W	263W
Eff	88.9%	85.6%	73.4%
Sine	20VPk -5V Os	20VPk -5V Os	20VPk -5V Os
Ths	45°C	45°C	45°C
Tj X2	100°C	100°C	100°C
TjX1	100°C	100°C	100°C
Vds Margin	208V	136V	19V

For Columns 2, 3 and 4 Circuit Parameters have been adjusted for the highest efficiency and highest power output while not exceeding the boundary conditions.

N Channel–P Channel Half Bridge with Sine Wave Drive

Figure 22 illustrates a classical N Channel-P Channel Half Bridge RF Generator. The Positive Supply Switch X2 and the Negative Supply Switch X1 form the two key active devices in the Half Bridge. X1 and X2 commutate in an alternating fashion providing a pseudo Square Wave drive to the input of the RF network. The RF network provides an impedance match from the Drain Impedance of X1, X2 of about 6Ω to 50Ω of the load. This L Match network is also resonating at 13.56MHz so that the output is a Sine Wave.



Circuit Performance	
Vsupply	±160V
Pout	1385W
Pin	1557W
PLoss	172W
Eff	88.9%
Sine Drive	Os=-5V Pk= 20V
Ths	45°C
Tj X2	100°C
TjX1	62°C
Vds Margin	202V
Drain Z=8Ω	Out Z=50Ω

Figure 22 N-P Channel Half Bridge

In Figure 22 a low frequency loop is highlighted in yellow. This loop is illustrated with near minimum stray inductance achievable. Great care should be taken to achieve these values. If we allow L1 and L6 to reach 100nH or greater, performance will be degraded. The inductance of the inner loop, L3, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics.

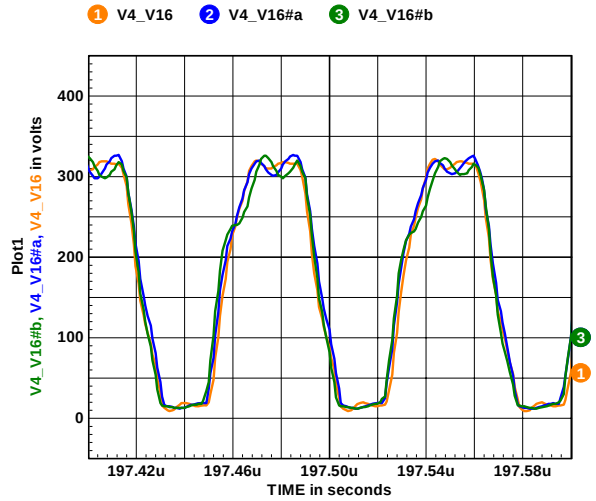


Figure 23 Variations in L3

The inductance of the inner loop, L3, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics. Figure 23 illustrates this variation with L1 and L6 held at 25nH. In Trace (1) L3 is 5nH and the ring frequency is 96.1MHz. In Trace (2) L3 is 25nH and the ring frequency is 70.4MHz. In Trace (3) L3 is 50nH and the ring frequency is 73.3MHz. The higher the ring frequency and the lower the amplitude the easier it will be to suppress. As shown in Figure 23 with Sine Wave drive the problem is mitigated.

It should be noted that comparing the previous configurations, Figures 2, 9 and 16 we see that Figure 23 shows the least effect of the L3 inductance variation.

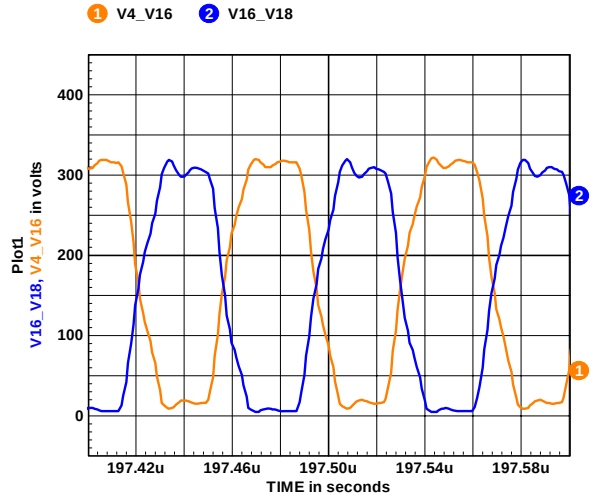


Figure 24 Drain Wave Forms N-P HB

Figure 24 illustrates the two Drain wave forms in the N-P Half Bridge with Sine Drive. Trace (1) is a plot of the Source to Drain wave form on X2. Trace (2) is a plot of the Source to Drain wave form on X1. From this plot we see a low ring amplitude with a peak-to-peak frequency of about 90.9MHz. No cross conduction is present. If the devices were cross conducting, the first positive going ring would be increasingly more pronounced.

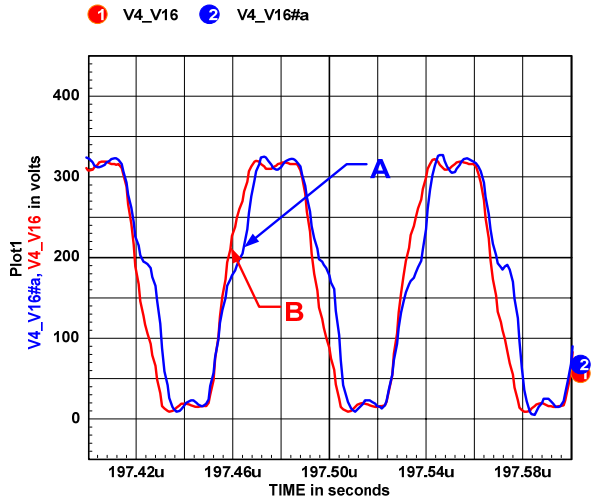


Figure 25 Improved Efficiency due to L7

In Figure 25 we see an overlay of the Drain Waveform for X1 Trace (1) with the inductor L7 (53nH) in place. In Trace (2) with L7 removed. The difference in markers A and B illustrates the energy saved by the addition of L7. This accounts for about 9% improvement in efficiency, 80°C reduction in junction temperature and a more dampened drain wave form.

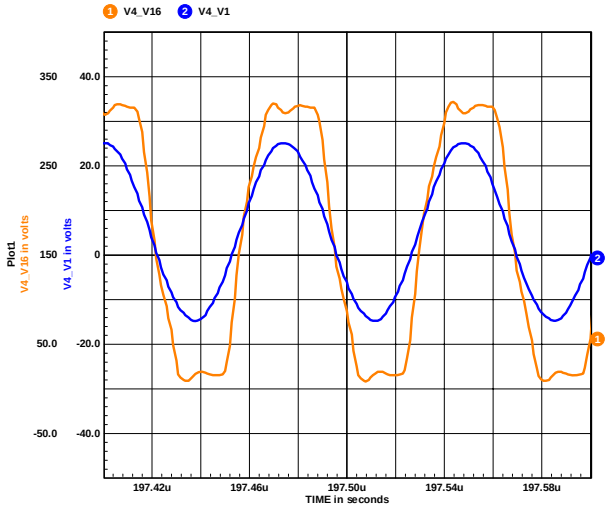


Figure 26 Drain and Gate Wave Forms N-P HB

Figure 26 illustrates Trace (1), the X2 Drain wave form in the N-P Half Bridge. Trace (2) is a plot of the Gate Drive wave form on the Gate of X2. The Sine wave form has been adjusted for highest efficiency and highest power while not exceeding the boundary conditions, Sine 20VPk, -5V Os.

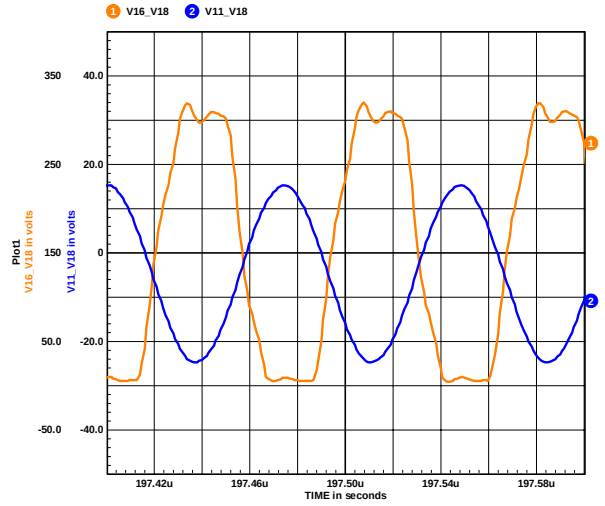


Figure 27 Drain Wave Forms N-N Low Side

Figure 27 illustrates Trace (1), the X2 Drain wave form in the Half Bridge. Trace (2) is a plot of the Gate Drive wave form on the Gate of X2. The Sine wave form has been adjusted for highest efficiency and highest power while limiting the MOSFETs junction to a maximum of ≈ 100°C, Sine 20VPk, -5V Os.

At 13.56MHz, the period is 73.75ns and one half cycle time is 36.87ns. However we have set the Gate Sine wave drive at -5V offset. This allows for two design considerations. The first of these is a margin to prevent cross conduction in X1 and X2. Cross conduction would be damaging to the devices and greatly reduce efficiency. The second consideration is to allow the charge and discharge of L7 which will increase efficiency.

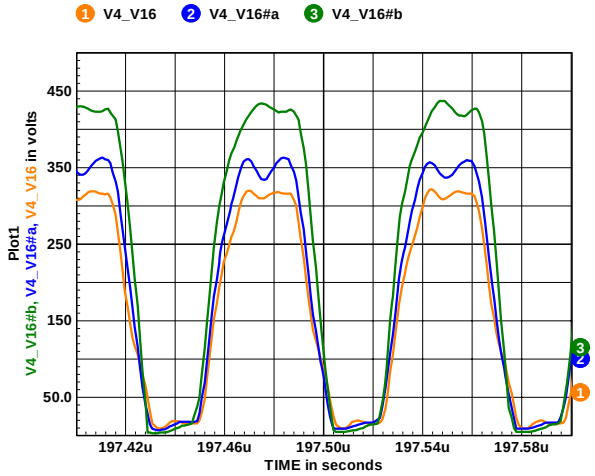


Figure 28 Drain Wave Forms with L1, L3, L6 Variations

In Figure 28 Trace 1 is the Drain Wave Form of the preferred configuration, also shown in column 2 of Table 4. As we increase the values of the Stray Inductive Terms L1, L3 and L6 we vary power output, efficiency and Vds margin. Trace 2 performance is shown in Table 4 column 3 and Trace 3 performance is shown in Table 4 column 4.

Shown in Table 4 are a set of values for variations in the three Stray Inductive Terms, L1, L3 and L6 and the impact on circuit performance. If we allow L1 and L6 to reach 100nH or greater, performance will be degraded. Consequently the Drain Peak voltage will approach 500V and the circuit will have less voltage margin. In addition, power output capability and efficiency will be reduced. The inductance of the inner loop, L3, is a very critical stray component. Values greater than a few nH can cause stability problems and excessive harmonics.

Table 4 L1, L3, L6 Variations

L2, L3, L6	L1=25nH L3=5nH L6=25nH	L1=100nH L3=20nH L6=100nH	L1=250nH L3=50nH L6=250nH
Vsupply	±160	±180V	±223V
Pout	1385W	1135W	796W
Pin	1557W	1307W	967W
PLoss	172W	172W	171W
Eff	88.9%	86.8%	82.3%
Sine	20VPk -5V Os	20VPk -5V Os	20VPk -5V Os
Ths	45°C	45°C	45°C
Tj X2	100°C	100°C	100°C
TjX1	62°C	62°C	62°C
Vds Margin	182V	139V	62V

For Columns 2 through 4 the Circuit Parameters have been adjusted for the highest efficiency and highest power output, while not exceeding the boundary conditions.

Performance vs. Load Characteristics

In this section we will examine the four optimized circuit combinations, N-N Pulse Drive, N-N Sine Drive, N-P Pulse Drive and N-P Sine Drive, under varying load conditions. We will not make any adjustments to the circuits to compensate for this change in load. This exercise will demonstrate important aspects of the topologies that we have not addressed overvoltage on the drain and excessive power dissipation.

N-N Channel HB with Pulse Drive Load 1-4

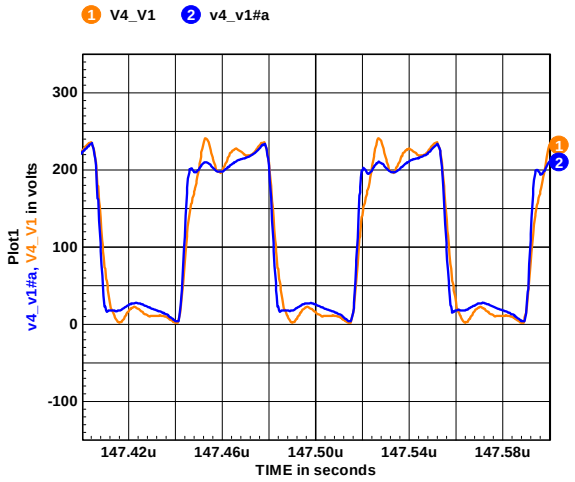


Figure 29 Load 1 vs. Base Line

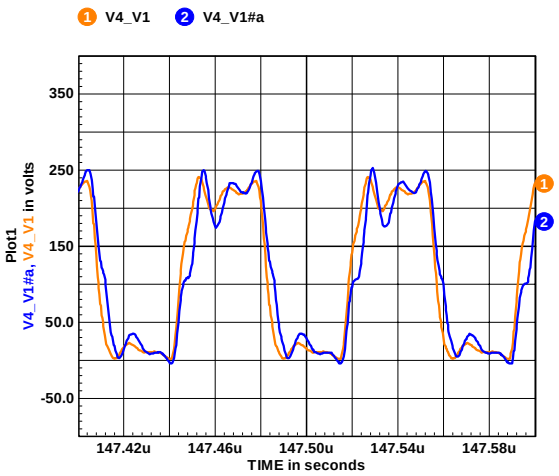


Figure 30 Load 2 vs. Base Line

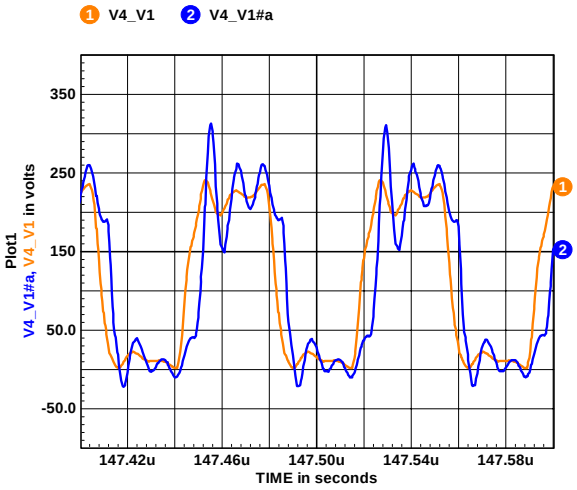


Figure 31 Load 3 vs. Base Line

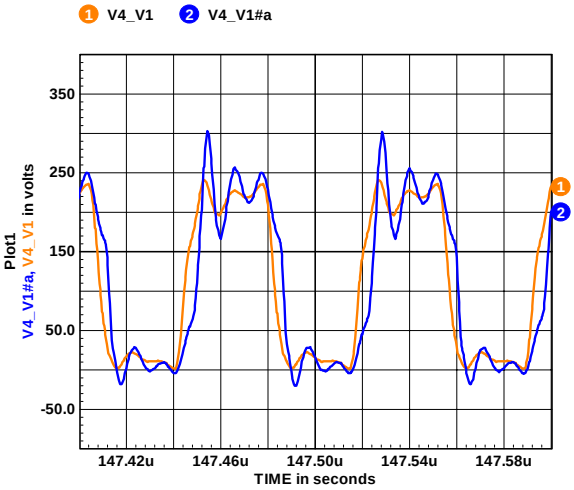


Figure 32 Load 4 vs. Base Line

Table 5 N-N Channel Pulse Drive

Load Number	Rs	Xs	jXs	Power out	Power In	Efficiency %	Junction Temp.
Base Line	50	0	0	2238	2499	89	100
1	**100**	**0**	**0**	**2238**	**2500**	**89**	**100**
2	**69.5**	**431nH**	**36.7**	**3585**	**4312**	**83**	**197**
3	**40**	**352.6nH**	**30**	**2495**	**3094**	**81**	**170**
4	**28.1**	**174.5nH**	**14.9**	**1646**	**1926**	**85**	**104**

In Table 5 we see that there are two load configurations (2-3) that present a thermal over load to the two devices, X1 and X2 of Figure 1 (Base Line). If this condition is not addressed, the two devices will be damaged. Loads 1 through 4 do not represent an over voltage risk to X1 and X2.

N-N Channel HB with Pulse Drive Load 5-8

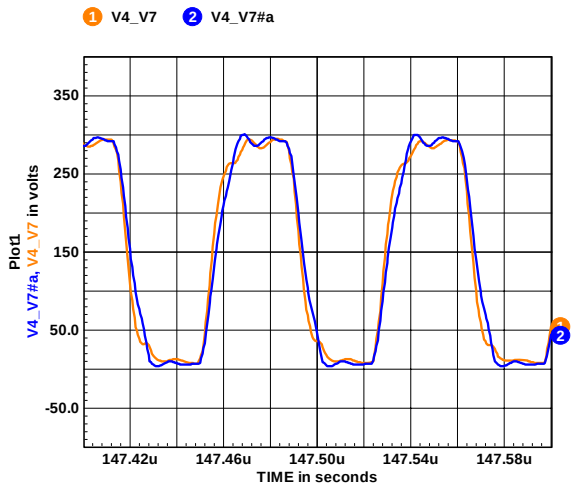


Figure 33 Load 5 vs. Base Line

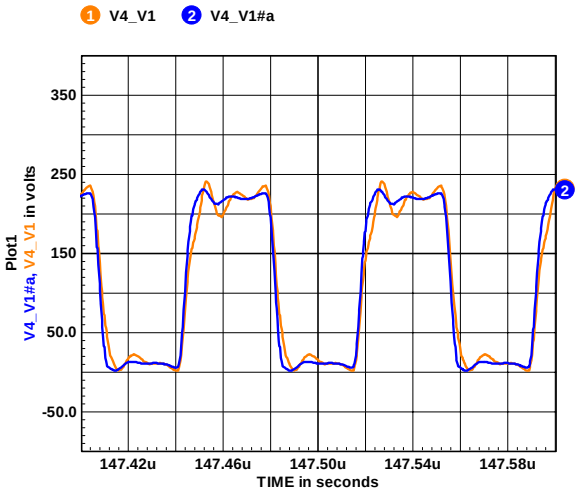


Figure 34 Load 6 vs. Base Line

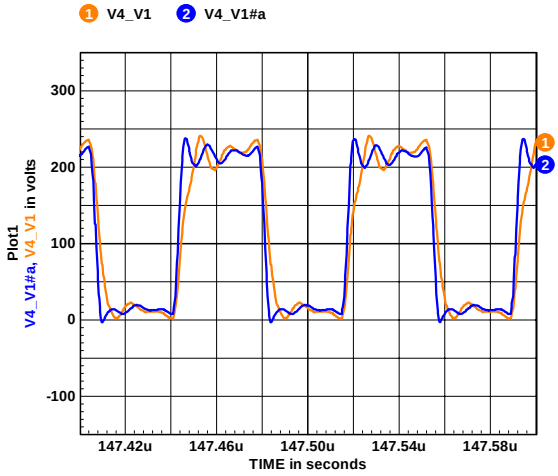


Figure 35 Load 7 vs. Base Line

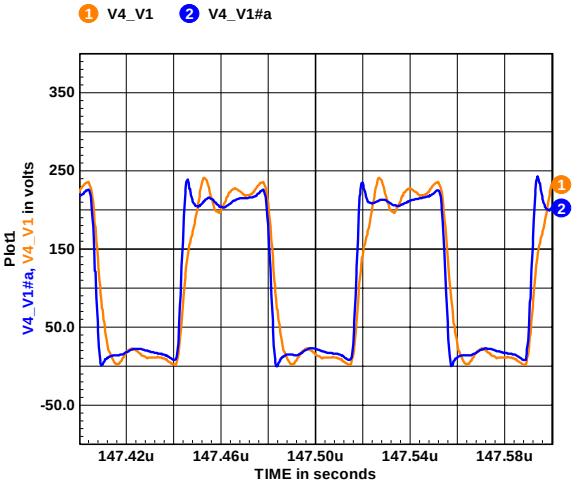


Figure 36 Load 8 vs. Base Line

Table 6 N-N Channel Pulse Drive

Load Number	Rs	Xs	jXs	Power out	Power In	Efficiency %	Junction Temp.
Base Line	50	0	0	2238	2499	89	100
5	**25**	**0**	**0**	**1284**	**1398**	**92**	**67**
6	**28.1**	**709pF**	**-14.9**	**1234**	**1388**	**89**	**77**
7	**40**	**390pF**	**-30**	**1416**	**1815**	**78**	**129**
8	**69.5**	**317pF**	**-36.7**	**2157**	**2815**	**77**	**183**

In Table 6 we see that there are two load configurations (7-8) that present a thermal over load to the two devices, X1 and X2 of Figure 1 (Base Line). If this condition is not addressed, the two devices will be damaged. Loads 5 through 8 do not represent an over voltage risk to X1 and X2.

N-N Channel HB with Sine Drive Load 1-4

In this section we will examine the four optimized N-N Channel circuit combinations with Sine Drive, under varying load conditions. We will not make any adjustments to the circuits to compensate for this change in load. This exercise will demonstrate important aspects of the topologies that we have not addressed overvoltage on the drain and excessive power dissipation.

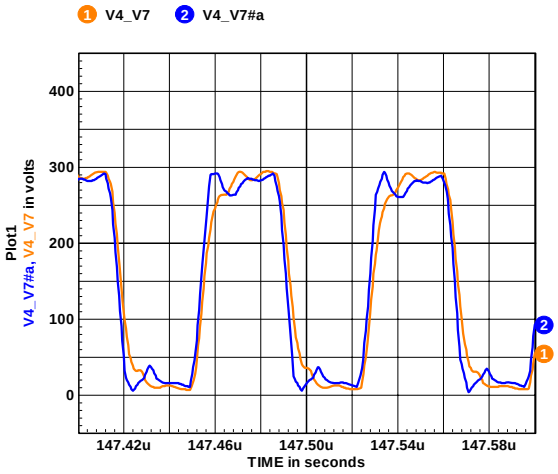


Figure 37 Load 1 vs. Base Line

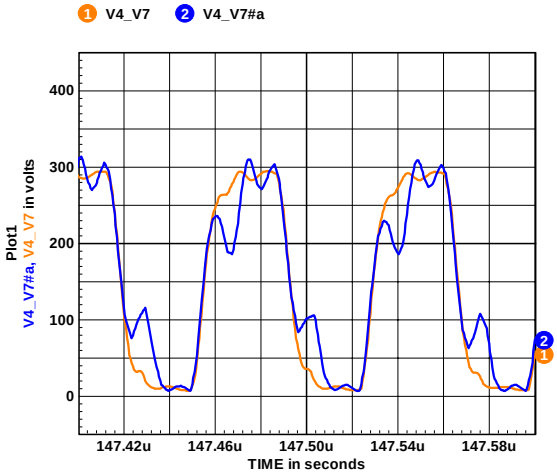


Figure 38 Load 2 vs. Base Line

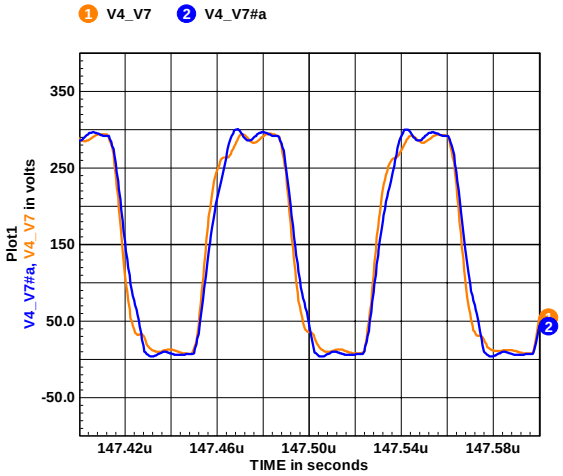


Figure 39 Load 3 vs. Base Line

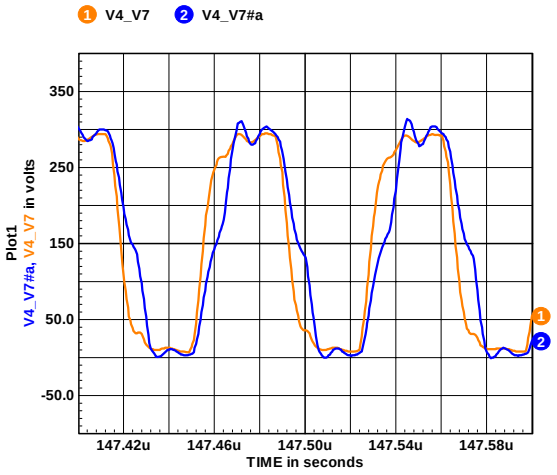


Figure 40 Load 4 vs. Base Line

Table 7 N-N Channel Sine Drive

Load Number	Rs	Xs	jXs	Power out	Power In	Efficiency %	Junction Temp.
Base Line	50	0	0	2089	2351	89	100
1	**100**	**0**	**0**	**2800**	**3669**	**76**	**227**
2	**69.5**	**431nH**	**36.7**	**2738**	**3539**	**77**	**213**
3	**40**	**352.6nH**	**30**	**2057**	**2587**	**79**	**155**
4	**28.1**	**174.5nH**	**14.9**	**1462**	**1686**	**87**	**92**

In Table 7 we see that there are three load configurations (1, 2 and 3) that present a thermal over load to the two devices, X1 and X2 of Figure 15 (Base Line). If this condition is not addressed, the two devices will be damaged. Load 1 through 4 do not represent an over voltage risk to X1 and X2.

N-N Channel HB with Sine Drive Load 5-8

In this section we will examine the four optimized N-N Channel circuit combinations with Sine Drive, under varying load conditions. We will not make any adjustments to the circuits to compensate for this change in load. This exercise will demonstrate important aspects of the topologies that we have not addressed overvoltage on the drain and excessive power dissipation.

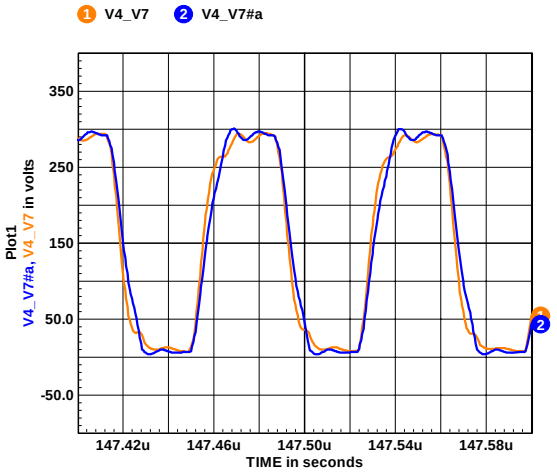


Figure 41 Load 5 vs. Base Line

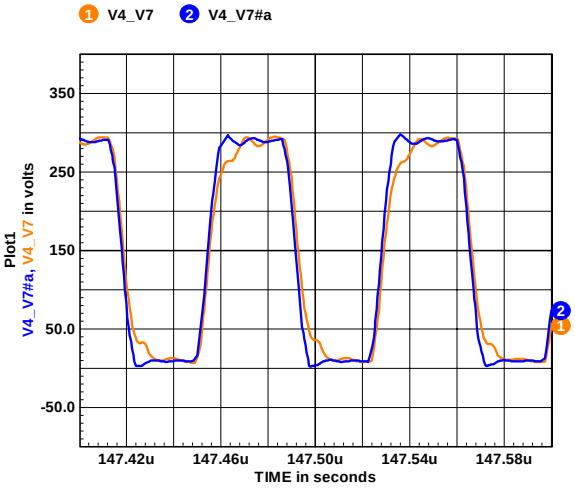


Figure 42 Load 6 vs. Base Line

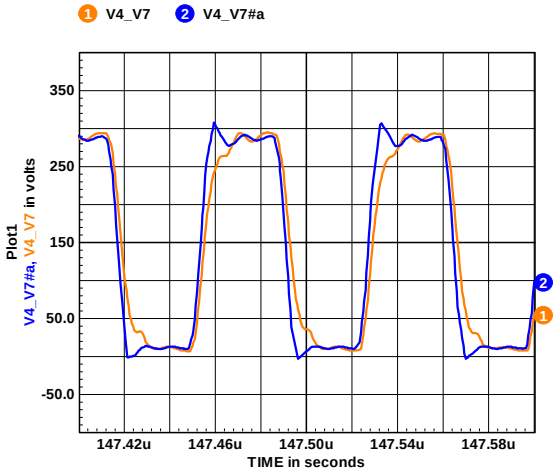


Figure 43 Load 7 vs. Base Line

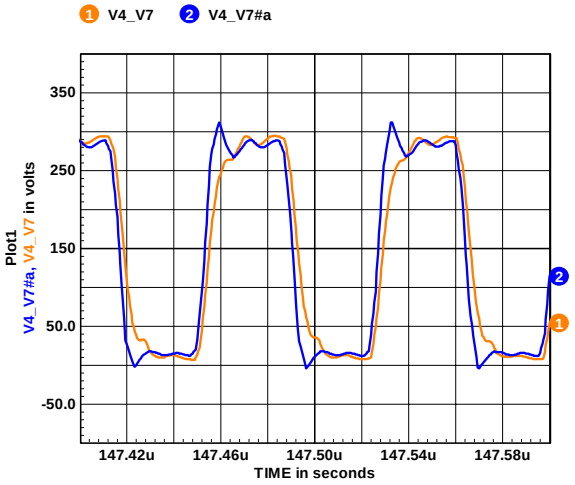


Figure 44 Load 8 vs. Base Line

Table 8 N-N Channel Sine Drive

Load Number	Rs	Xs	jXs	Power out	Power In	Efficiency %	Junction Temp.
Base Line	50	0	0	2238	2499	89	100
5	**25**	**0**	**0**	**1167**	**1265**	**92**	**65**
6	**28.1**	**709pF**	**-14.9**	**1099**	**1281**	**86**	**83**
7	**40**	**390pF**	**-30**	**1285**	**1605**	**80**	**112**
8	**69.5**	**317pF**	**-36.7**	**1735**	**2355**	**73**	**175**

In Table 8 we see that there is only one load configuration (8) that presents a thermal over load to the two devices, X1 and X2 of Figure 15 (Base Line). If this condition is not addressed, the two devices will be damaged. Loads 5 through 8 do not represent an over voltage risk to X1 and X2.

N-P Channel HB with Pulse Drive, Load 1-4

In this section we will examine the four optimized N-P Channel circuit combinations with Pulse and Sine Drive, under varying load conditions. We will not make any adjustments to the circuits to compensate for this change in load. This exercise will demonstrate important aspects of the topologies that we have not addressed overvoltage on the drain and excessive power dissipation.

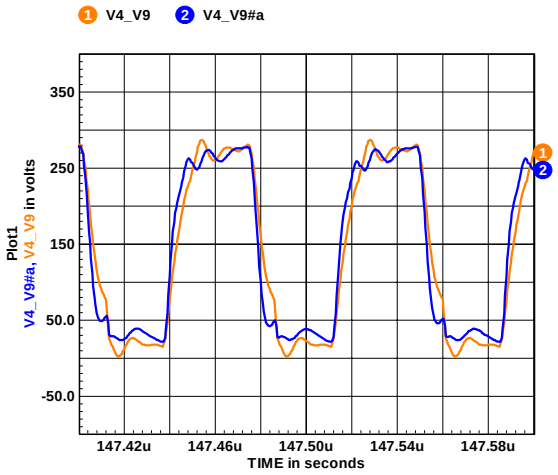


Figure 45 Load 1 vs. Base Line

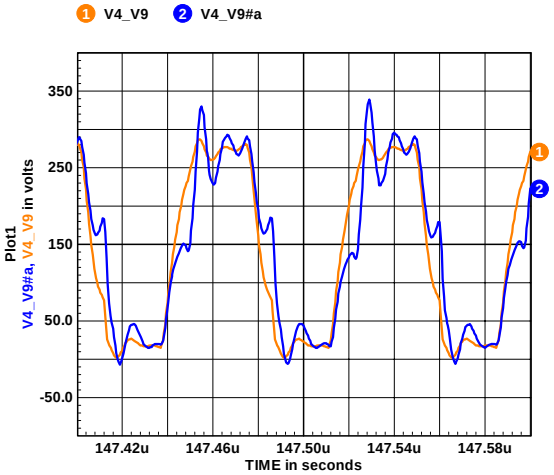


Figure 46 Load 2 vs. Base Line

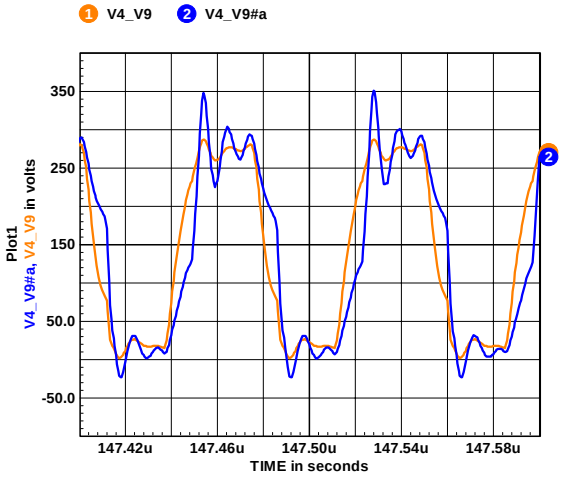


Figure 47 Load 3 vs. Base Line

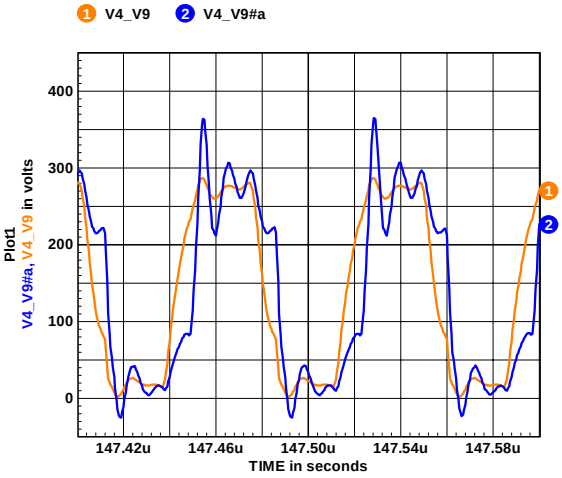


Figure 48 Load 4 vs. Base Line

Table 9 N-P Channel Pulse Drive

Load Number	Rs	Xs	jXs	Power out	Power In	Efficiency %	Junction Temp.
Base Line	50	0	0	1506	1679	90	100
1	**100**	**0**	**0**	**2507**	**2987**	**84**	**146**
2	**69.5**	**431nH**	**36.7**	**2227**	**2748**	**81**	**154**
3	**40**	**352.6nH**	**30**	**1519**	**1951**	**78**	**136**
4	**28.1**	**174.5nH**	**14.9**	**1024**	**1248**	**82**	**92**

In Table 9 we see that there are three load configurations (1, 2 and 3) that present a thermal over load to the two devices, X1 and X2 of Figure 8 (Base Line). If this condition is not addressed, the X2 device will be damaged. It should be noted that that the P-Channel device, X2, will have about three times the power dissipation of the N-Channel X1 device. Loads 1 through 4 do not represent an over voltage risk to X1 and X2.

N-P Channel HB with Pulse Drive, Load 5-8

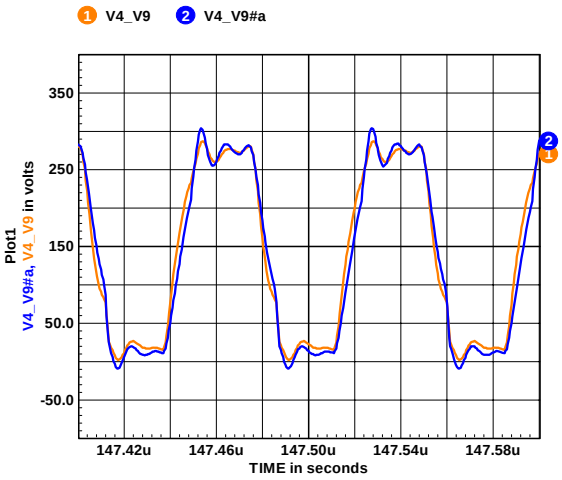


Figure 49 Load 5 vs. Base Line

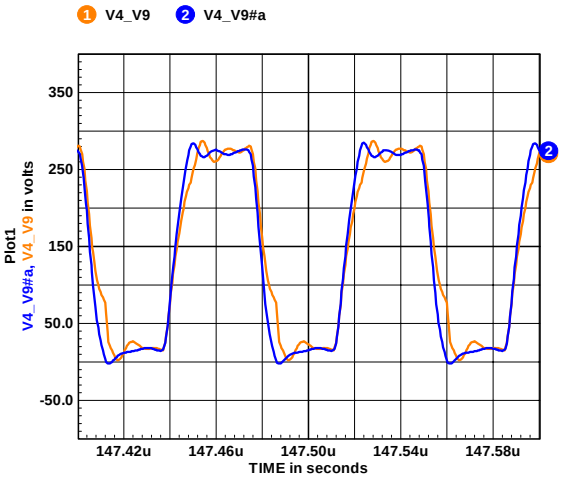


Figure 50 Load 6 vs. Base Line

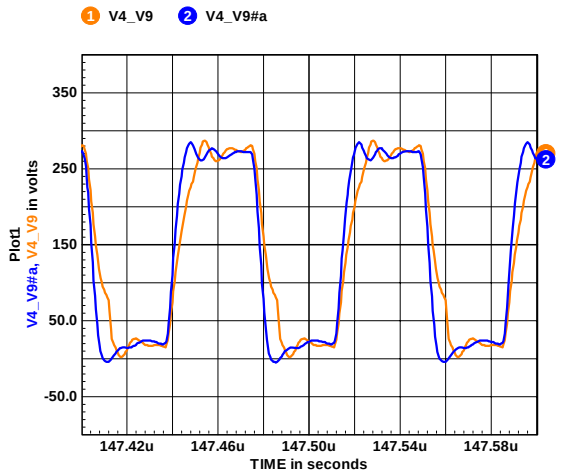


Figure 51 Load 7 vs. Base Line

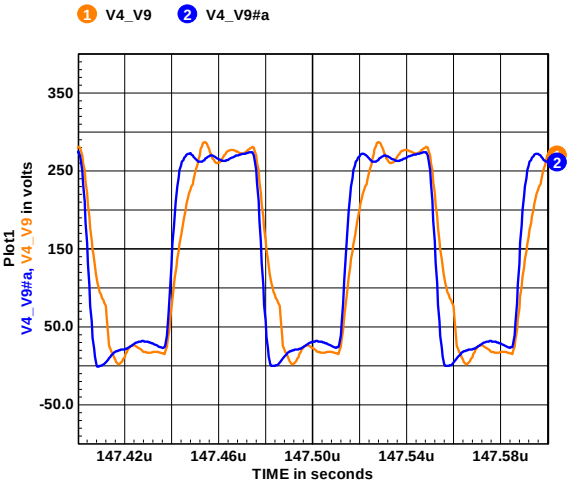


Figure 52 Load 8 vs. Base Line

Table 10 N-P Channel Pulse Drive

Load Number	Rs	Xs	jXs	Power out	Power In	Efficiency %	Junction Temp.
Base Line	50	0	0				
5	**25**	**0**	**0**	**834**	**926**	**90**	**64**
6	**28.1**	**709pF**	**-14.9**	**870**	**973**	**89**	**67**
7	**40**	**390pF**	**-30**	**1126**	**1318**	**85**	**85**
8	**69.5**	**317pF**	**-36.7**	**1708**	**2056**	**83**	**118**

In Table 10 we see that there is one load configuration (8) that presents a thermal over load to the two devices, X1 and X2 of Figure 8 (Base Line). If this condition is not addressed, the X2 device will be damaged. It should be noted that the P-Channel device, X2, will have about three times the power dissipation of the N-Channel X1 device. Loads 1 through 4 do not represent an over voltage risk to X1 and X2.

N-P Channel HB with Sine Drive, Load 1-4

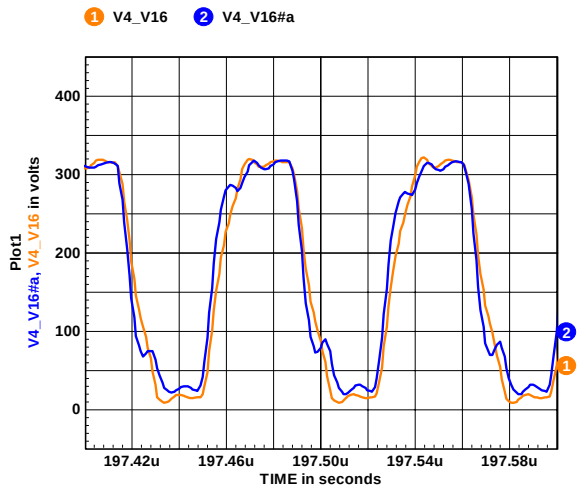


Figure 53 Load 1 vs. Base Line

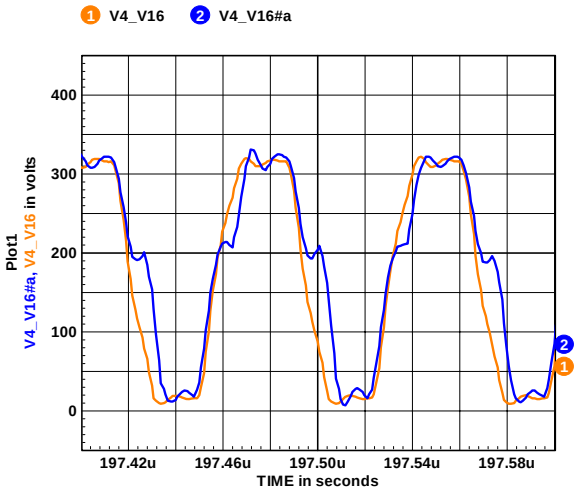


Figure 54 Load 2 vs. Base Line

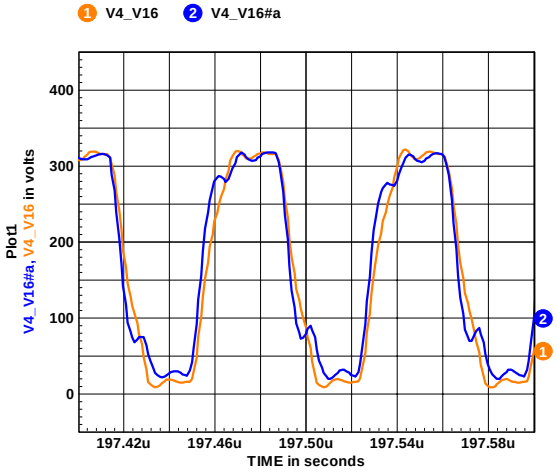


Figure 55 Load 3 vs. Base Line

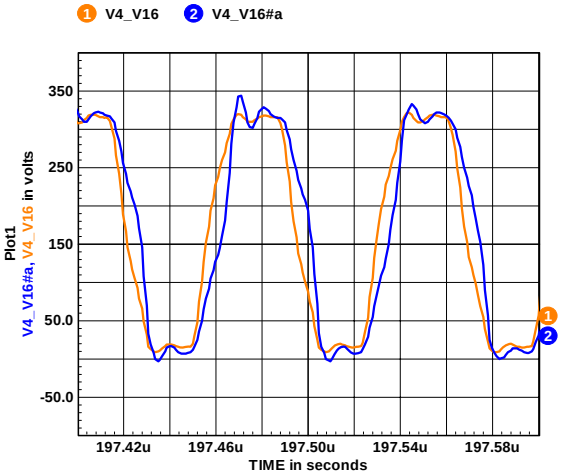


Figure 56 Load 4 vs. Base Line

Table 11 N-P Channel Sine Drive

Load Number	Rs	Xs	jXs	Power out	Power In	Efficiency %	Junction Temp.
Base Line	50	0	0	1385	1557	90	100
1	**100**	**0**	**0**	**2234**	**2720**	**82**	**147**
2	**69.5**	**431nH**	**36.7**	**1776**	**2326**	**76**	**160**
3	**40**	**352.6nH**	**30**	**1256**	**1702**	**74**	**138**
4	**28.1**	**174.5nH**	**14.9**	**892**	**1148**	**78**	**98**

In Table 11 we see that there are three load configurations (1-3) that present a thermal over load to the two devices, X1 and X2 of Figure 22 (Base Line). If this condition is not addressed, the X2 device will be damaged. It should be noted that the P-Channel device, X2, will have about three times the power dissipation of the N-Channel X1 device. Loads 1 through 4 do not represent an over voltage risk to X1 and X2.

N-P Channel HB with Sine Drive Load 5-8

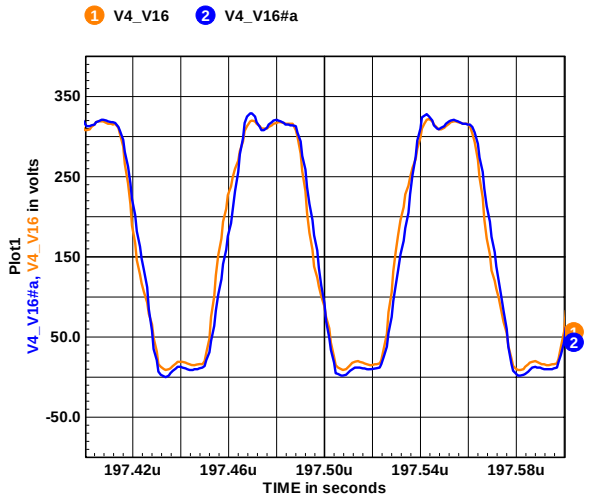


Figure 57 Load 5 vs. Base Line

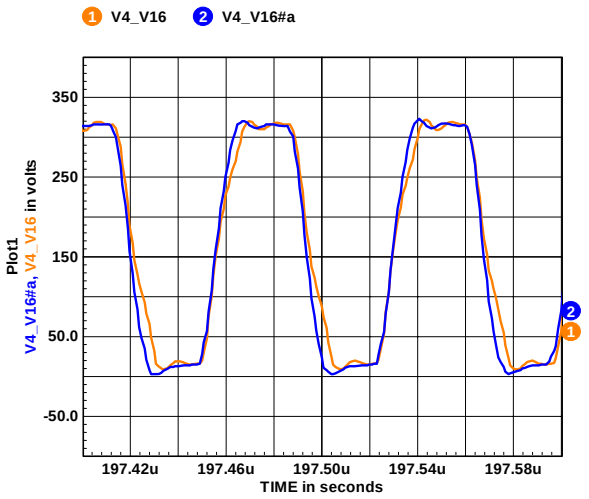


Figure 58 Load 6 vs. Base Line

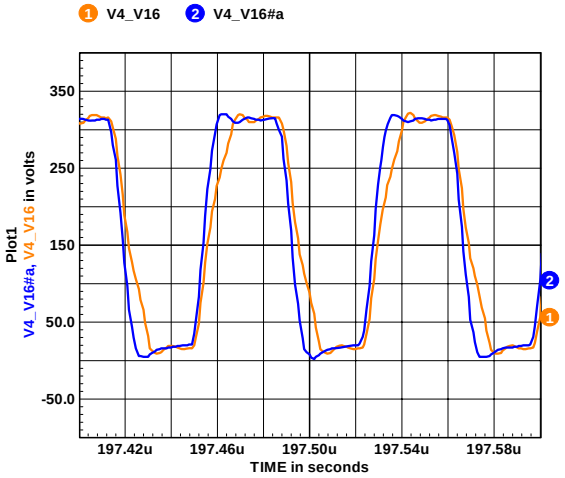


Figure 59 Load 7 vs. Base Line

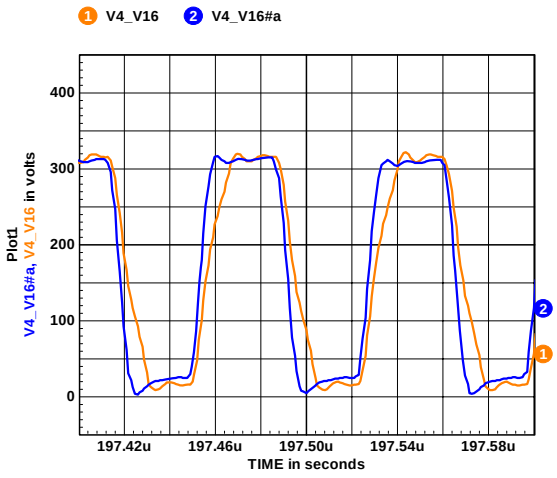


Figure 60 Load 8 vs. Base Line

Table 12 N-P Channel Sine Drive

Load Number	Rs	Xs	jXs	Power out	Power In	Efficiency %	Junction Temp.
Base Line	50	0	0	1385	1557	90	100
5	**25**	**0**	**0**	**757**	**869**	**87**	**68**
6	**28.1**	**709pF**	**-14.9**	**753**	**865**	**87**	**68**
7	**40**	**390pF**	**-30**	**1017**	**1220**	**83**	**87**
8	**69.5**	**317pF**	**-36.7**	**1601**	**1975**	**81**	**123**

In Table 12 we see that there is one load configuration (8) that presents a thermal over load to the two devices, X1 and X2 of Figure 8 (Base Line). If this condition is not addressed, the X2 device will be damaged. It should be noted that the P-Channel device, X2, will have about three times the power dissipation of the N-Channel X1 device. Loads 1 through 4 do not represent an over voltage risk to X1 and X2.

Conclusion

Recall that in the Introduction the Parameter Adjustment Process and the boundary conditions were defined.

N-N and N-P Power Output Comparison Pulse Gate Drive and Sine Gate Drive

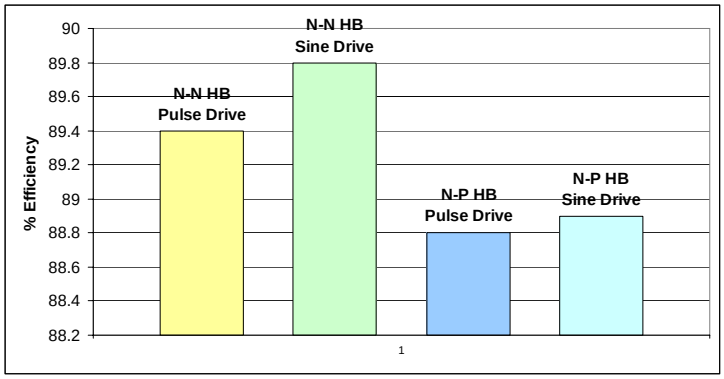


Figure 61 Power Output vs. Configuration

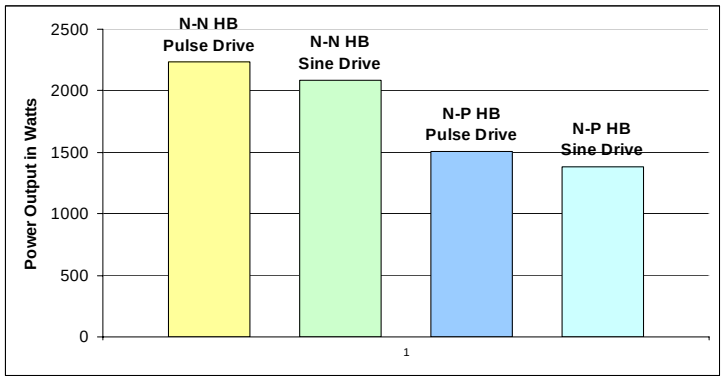


Figure 62 Efficiency vs. Configuration

Figure 61 illustrates the variation in power output and circuit configuration. Figure 62 illustrates the variation in efficiency vs. configuration. Before we discuss these figures, recall the boundary conditions from the introduction. Circuit Parameters have been adjusted for the highest efficiency and highest power.

In Figure 61 we see that the highest power output is achieved with the N-N Half Bridge with Pulse Drive and in Figure 62 we see that the best efficiency is delivered by the N-N Half Bridge Sine Gate Drive, however the improvement is only 0.4%. In Figure 62 we also see that the N-P Pulse Drive and the N-P Sine Drive produce notably lower power output than the either of the two N-N or N-P configurations with Pulse Drive. We also see that of all the configurations the N-P configurations yield the lowest power output and the lowest efficiencies. In addition, it should be noted that the Rds(on) of P-Channel device is approximately 0.9Ω that of the N-Channel device. Therefore X2 will have about three times the power dissipation of the N-Channel, X1 device. Loads 1 through 4 do not represent an over voltage risk to X1 and X2.

Low Frequency Loop, High Frequency Loop and Stray Inductance

Stray Inductance in most cases is detrimental to circuit performance. For the four HB circuit configurations we included a table with three sets of stray inductances. The preferred is Set (1), 25nH, 5nH, 25nH. Set (2), 100nH, 20nH, 100nH is usable but not advised, and Set (3), 250nH, 50nH, 250nH is not acceptable.

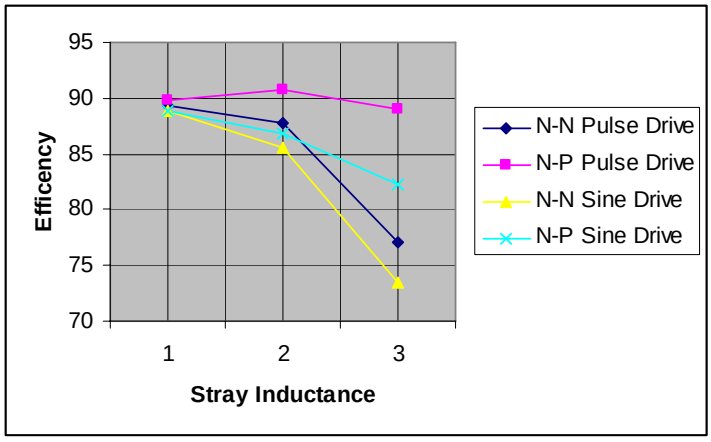


Figure 63 Efficiency vs. Stray Inductance

Figure 63 illustrates efficiency vs. stray inductance. For Sets 2 and 3 we see that the efficiency is reduced.

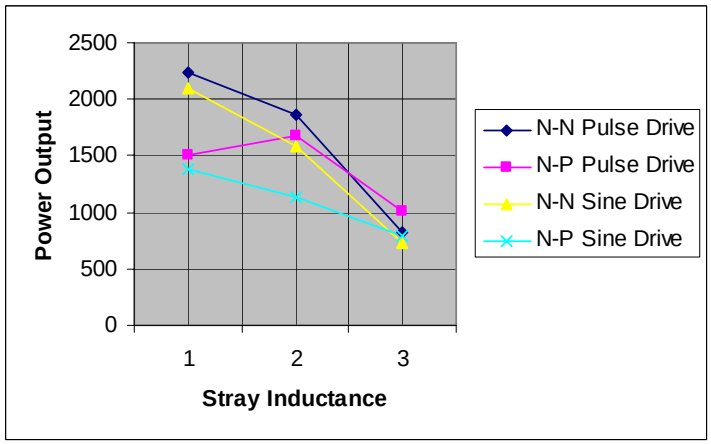


Figure 64 Efficiency vs. Stray Inductance

Figure 64 illustrates power output vs. stray inductance. For Sets 1, 2 and 3 we see that the power output is reduced.

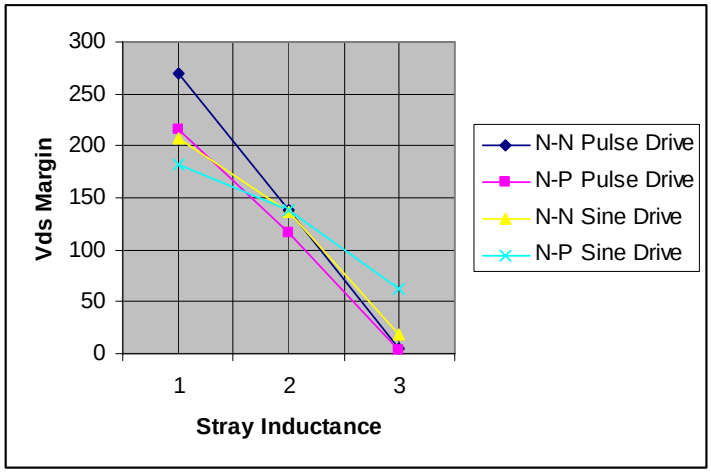
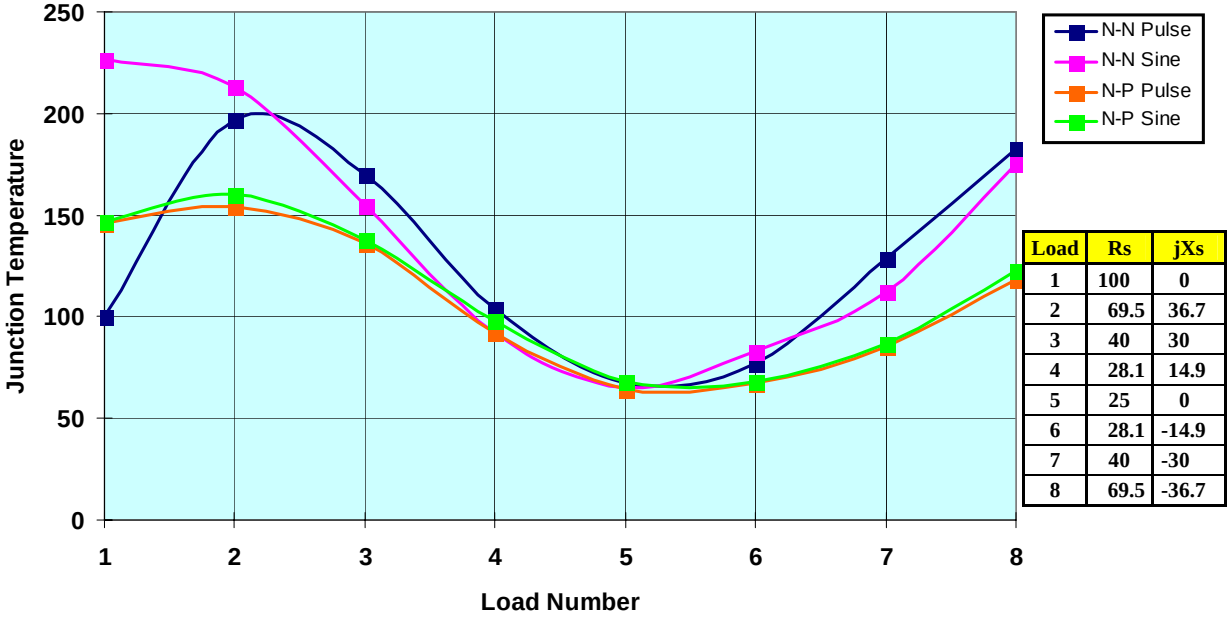


Figure 65 Efficiency vs. Stray Inductance

Figure 65 illustrates Vds margin vs. stray inductance. For Sets 2 and 3 we see that the Vds margin is reduced.

Figures 63, 64 and 65 illustrate the value of taking great care in the minimization of the stray inductance in the low frequency and the high frequency loops.

Non reactive and Reactive loads



Load	Rs	jXs
1	100	0
2	69.5	36.7
3	40	30
4	28.1	14.9
5	25	0
6	28.1	-14.9
7	40	-30
8	69.5	-36.7

Figure 66 Loads vs. Configuration

Each of these eight loads illustrated in Figure 66 presents a 2:1 VSWR mismatch to 50Ω. They are equally spaced every 45° around a 2:1 VSWR load circle. In each of the circuits, the 50Ω load is transformed through the output matching network (i.e., L5+L6 and C2 in Figure 1) to approximately 3Ω at the junction of transistors X1 and X2. A load other than 50Ω is "mismatched" and its effect on the circuit is quite different.

An output load impedance lower than 50Ω will be transformed to a higher impedance load at the devices. The transistors can more easily supply the full output voltage to this higher impedance and consequently the output power is less and the junction temperature is lower. A load impedance greater than 50Ω on the output is transformed though the matching network to an impedance lower than 3Ω at the transistor junction. This causes the devices to be overloaded and mistuned. They put the full voltage on this lower impedance creating more output power at lower efficiency which in turn causes the rise in junction temperature. Figure 66 clearly demonstrates the importance of maintaining a proper load on the output of the RF Generator.

Topology

Figures 61 through 65 provide an understanding of which topology is best matched to the application requirements. For example, for a 2KW design an N-N HB is a good choice, high power and high efficiency. Combining two Half Bridges then forms a 4KW Full Bridge. Pulse Gate Drive allows complex modulation programs. Phase, pulse width and amplitude may all be used in a computer controlled modulation program to, in some configurations, reduce the size of the DC filter Capacitors or AM modulate the RF Carrier. See Gate Drive below.

Gate Drive

Figure 61 and 62 illustrate that Gate Drive is not exclusive to a particular topology. Pulse and Sine types of Gate Drive each have their advantages and disadvantages. The choice of which type is best suited to the topology is complicated by the topology which has been selected.

N-N HB Pulse Gate Drive

For this topology, the Figure 1 X2 device, Gate Drive is the most difficult to implement. On a 1-10 scale of difficulty, it would be a 9. However, the versatility would be the highest.

N-N HB Sine Gate Drive
For this topology, the Figure 15 X2 device, Gate Drive is of moderate difficulty to implement. On a 1-10 scale of difficulty, it would be a 5. The versatility would be moderate to low.

N-P HB Pulse Gate Drive
For this topology, the Figure 8 X2 device, Gate Drive is easy to implement. On a 1-10 scale of difficulty, it would be a 6. The versatility would be high to highest.

N-P HB Sine Gate Drive
For this topology, the Figure 22 X2 device, Gate Drive is the least difficult to implement. On a 1-10 scale of difficulty, it would be a 3. The versatility would be moderate.

MOSFET Drain Impedance to Output Load Impedance Match
Setting the value of the Drain load Impedance to reflect from the Output Load should start with the Rds(on) of the MOSFET. For example if the MOSFET Rds(on) is 0.3Ω and the goal is to reach ≈ 90% efficiency, then set the reflected impedance at 3Ω. However this is only an approximate value. Lowering this value will increase the power output, however the efficiency will be reduced. Conversely, increasing the reflected impedance will increase the efficiency but will require the Drain Supply voltage to be increased to maintain the same output power. This presumes that no other circuit changes are made at the same time.

RF Network Compensating Inductance
Since the optimum Drain Impedance for the Half Bridge is not 50Ω, an L-network is used to make the impedance transformation. This is a resonant network and only performs the translation at the design frequency. The common design formulas account only for a resistive source and load. Since the output devices have parasitic capacitance, after the network is designed the series L must be adjusted to account for this capacitance. A value of L ≈ 10% to 25% higher than the calculated is typically required to bring the network to full efficiency, illustrated in Figure 1 as L7.

Circuit Performance vs. Load Conditions
Mismatched loads are often encountered in typical operation. Though their individual effects are different, they all must be accounted for by the control system to prevent various problems they cause: low output power, poor efficiency, over-current, and/or high junction temperature. A practical half or full bridge generator will typically use a variable power supply to control the output power. An obvious method to protect the generator would be to sense the load mismatch with a directional coupler and reduce the operating supply voltage until the load mismatch is corrected. In a pulse-modulated system, the output power can be reduced by decreasing the duty cycle until the load mismatch is corrected.

Correcting the load mismatch usually requires some form of adjustable matching network at the output of the RF generator that is tuned so the mismatch is corrected.