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By: Kenneth Dierberger

APPLICATION NOTE

Simple and Inexpensive High-Efficiency Power Amplifier Using New APT MOSFETs

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Simple and Inexpensive High-Efficiency Power Amplifier Using New APT MOSFETs

Kenneth Dierberger
Applications Engineering Manager
Advanced Power Technology Inc.
405 SW Columbia St.
Bend, Oregon 97702 USA

Frederick H. Raab, Ph.D.
Green Mountain Radio Research Co.
50 Vermont Ave., Fort Ethan Allan
Colchester, Vermont 05446

Lee Max
Independent Consultant
6284 Squiredell Dr.
San Jose, California 95129

ABSTRACT

This note describes a simple and inexpensive high-efficiency RF power amplifier based upon the new Advanced Power Technology (APT) RF-power MOSFETs. Its key features are a transformerless driver, low-cost RF-power MOSFETs, a simple output transformer, and Class-D operation. The PA and driver operate from +12 and +50V and require an RF input of only 10mW. They produce an output of 250W or more at frequencies from 1.8 to 13.56MHz.

1. INTRODUCTION

This note describes a simple and inexpensive high-efficiency RF power amplifier based upon the new APT RF-power MOSFETs. Its key features are:

- A transformerless driver,
- Low-cost RF-power MOSFETs,
- Simple output transformer, and
- Class-D operation.

The PA and driver operate from +12 and +50V and require an RF input of only 10mW. They produce an output of 250W or more at frequencies from 1.8 to 13.56MHz.

The basic concept ensures an amplifier that is inherently inexpensive and easy to manufacture. In the prototype described here, however, no attempt has been made to minimize the number of components and every attempt has been made to ensure good RF grounds and bypasses.

2. BASIC DESIGN CONSIDERATIONS

Class-D power amplifiers employ two transistors in a push-pull configuration. The transistors are driven to act as switches and generate a square-wave voltage. The fundamental-frequency component of the square wave is passed to the load through a filter. Power output is controlled by varying the supply voltage.

A class-D PA is ideally 100-percent efficient at all amplitudes and in spite of load reactance. In practice, it is significantly more efficient than a similar class-B PA, especially for lower amplitudes and reactive loads.

Drain-Load Line and Turns Ratio

The power output of a class-D PA [1] [2] is:

$$P_O = \frac{8}{\pi^2}\frac{v_{\text{eff}}^{\ 2}}{2R} \qquad (1)$$

where the effective supply voltage (for MOSFETs) is:

$$V_{\text{eff}} = V_{DD}\frac{R}{R + R_{\text{ON}}} \qquad (2)$$

Above, R is the drain-load line (seen by one drain with the other open) and R_{ON} is the on-state drain-source resistance. For the ARF440 and ARF441, $R_{\text{ON}} \approx 0.8\Omega$. To obtain a 250W output with a 50V supply thus requires $R \leq 6.4\Omega$.

For a simple transformer, the drain-load line is related to the load R_0 by:

$$R = \left(m/n\right)^2 R_o \qquad (3)$$

where m and n are the numbers of turns in the primary and secondary windings, respectively. For an RF transformer, *m* and *n* must be small integers. For a 50Ω load, a bit of iteration yields *m*=1, *n*=3, and *R*=5.56Ω.

Ignoring transformer, switching, and capacitance losses, the efficiency of the PA is:

$$\eta = \frac{V_{\text{eff}}}{V_{DD}} = 0.874 \qquad (4)$$

The effects of switching and drain capacitance can be predicted by the equations given in [2]. These calculations yield a 76.2 percent efficiency for operation at 13.56MHz, excluding losses in the transformer and output filter. With typical losses in those components, an efficiency of 70 percent is expected.

Gate Voltage and Current

The peak drain current [1] [2] is:

$$i_{\text{Dmax}} = \frac{4}{\pi}\frac{v_{\text{eff}}}{R} = 10.01\text{A} \qquad (5)$$

which corresponds to I_{dc}=6.37A. The data sheets for the ARF440/ARF441 show that a gate-source voltage of 9 to 10V should be sufficient for minimum R_{ON} at i_{Dmax}=10A. Since the threshold voltage is about 3.5V, the RF drive voltage must be about 6.5V or slightly more.

The data sheets give typical small-signal active-region gate-source and gate-drain capacitances of 700 and 55pF, respectively. The input capacitance is, however, the sum of small-signal capacitances only while the MOSFET is in the cut-off region. As the MOSFET enters the active (velocity-saturation) region, the gate-drain capacitance is Miller-multiplied by the voltage gain (plus one). Finally, as the MOSFET enters the linear region (resistive region), the gate-drain capacitance inflates by a factor of five or so. As a result, the effective gate-drain capacitance is close to 2600pF during the switching process [3].

The total gate charge is 37nC at 10V. Transitioning the gate voltage in one tenth of the RF period (73.7ns at 13.56MHz) thus requires an average of 5A of gate current. A low driving resistance and low inductance are clearly required.

3. CIRCUIT

The circuit of the power amplifier and driver is shown in Figure 1; parts are identified in Tables 1 and 2. All stages are ac-coupled. Consequently, the unexpected absence of an input signal results only in an inactive circuit with minimal current flow and power consumption.

The total cost of all of the parts in the prototype breadboard is about $190, based upon quantities ranging from 1 to 100.

Pre driver

The pre driver uses a pair of low-cost ICs (U1 and U2 in Figure 1) rather than the conventional RF transformer to provide out-of-phase driving signals for the two final MOSFETs. It also provides hard limiting (sine-wave to square-wave conversion) of the input signal.

The Elantec EL7144C is intended for use as a gate driver. The internal Schmitt trigger allows it to serve as hard limiter, and the presence of both inverting and non-inverting inputs allows a pair to serve as a phase splitter.

The RF input is ac-coupled to the non-inverting input of U1 and the inverting input of U2. Adjustment of the biases via R6 and R8 allows the transition points to be selected to produce the desired duty ratio.

For operation at the lower frequencies (≤4MHz), the duty ratio can be set to 50:50. In this case, the phase error between the two EL7144s is about 0.5ns.

At higher frequencies (≥10MHz), the difference in the turn-on and turn-off delay times of the ARF440 and ARF441 can cause both to be on at the same time (Appendix A). The associated increase in current consumption is eliminated by adjusting the duty ratios of U1 and U2 so that the final MOSFETs operate with 50:50 duty ratios. This requires adjusting R6 and R8 so that the low-state pulse width is about 12ns shorter than the high-state pulse width. Some phasing error (up to 25°) is unfortunately introduced by this adjustment.

The EL7144s have high input impedances, so R5 provides a 50Ω input impedance for the signal source. Input signals in the range of 10 to 100mW are satisfactory, allowing this PA to be driven directly from a laboratory signal generator.

The best switching speed is obtained with V_{DD1}=12V.

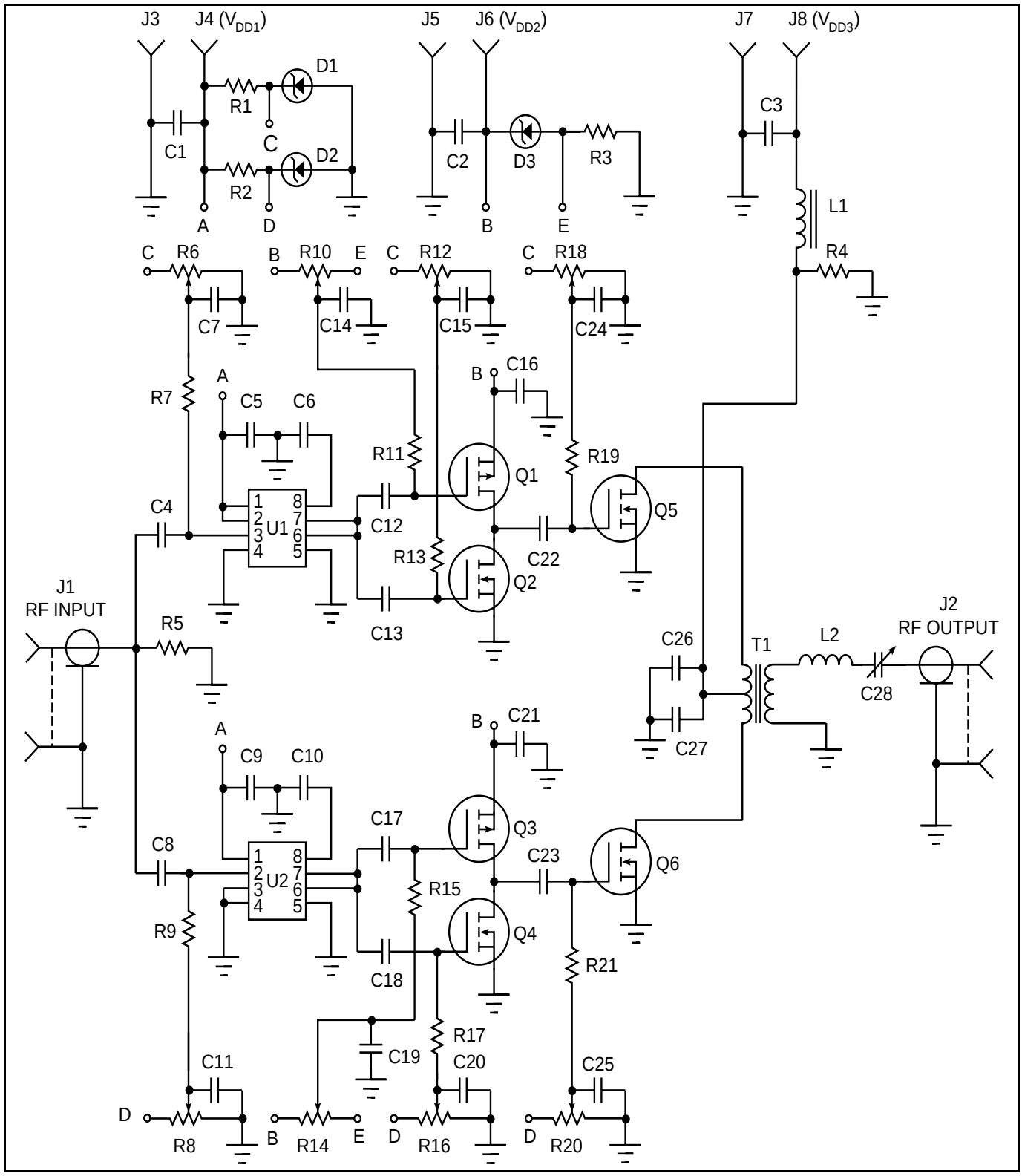

Figure 1. Circuit of power Amplifier and driver

REFERENCE DESIGNATOR	PART DESCRIPTION
C1,C2	33μF, 50V electrolytic, Mallory SKR330M1HE11V
C3	20μF, 250V electrolytic, Mallory TT250M20A
C4-C27	0.1μF, 50WV chip, ATC 200B104NP50X
C28	See Table 2.
D1,D2,D3	5.1V, 0.25W Zener, 1N751A
J1,J2	BNC female bulkhead Recommended: Amphenol 31-5538 Used: RF Industries RFB-1116S/UG
J3-J8	European-style binding post, Johnson 111-0104
L1	3.5μH, 7 turns #24 enameled wire on Ferroxcube 768XT188 4C4 toroid
L2	See Table 2.
Q1,Q3	p-channel MOSFET, Siliconix 2N7016
Q2,Q4	n-channel MOSFET, Siliconix 2N7012
Q5	n-channel MOSFET, APT ARF440
Q6	n-channel MOSFET, APT ARF441
R1,R2	330Ω RC07
R3	220Ω RC07
R4	10KΩ RC07
R5	51Ω RC07
R6,R8,R10,R12,R14,R16,R18,R20	1KΩ trimpot, Bournes 3299X-1-102
R7,R9,R11,R13,R15,R17,R19,R21	4.7kΩ RC07
T1	One Ceramic Magnetics 3000-4-CMD5005 block of CMD5005 ferrite wired per Figure 3
U1,U2	Schmitt trigger/limiter, Elantec EL7144C
Heat sink for DIP IC	Aavid 5802 clip-on
Heat sink for Q5 and Q6	Aavid 61475, 6.5-in wide by 4-in long
IC socket, 8-pin DIP (4)	Augat 208-AG190C
PC board	Approximately 6.5-in wide by 8-in long
Plastic bracket for L2	Cut from plastic L
Plastic bracket for C28	Cut from plastic L
Feet (6)	Aluminum threaded spacer, 4-40 x 2 in (Keystone 2205)

Table 1. Components other than tuning.

1.8MHz	L2:	22μH, Micrometals T200-6 toroid (2-in O.D.) with 52 turns of 24-AWG enameled wire
	C28:	354pF, 2.5kV padder, FW Capacitors AP091HV
3.5MHz	L2:	11.4μH, Micrometals T200-6 toroid (2-in O.D.) with 32 turns of 24-AWG enameled wire
	C28:	180pF, 2.5-kV padder, FW Capacitors AP051HV
7MHz	L2:	5.7μH, Micrometals T200-2 toroid (2-in O.D.) with 20 turns of 24-AWG enameled wire
	C28:	90pF, 2.5kV padder, FW Capacitors AP031HV
10MHz	L2:	2.93μH, Micrometals T200-2 toroid (2-in O.D.) with 14 turns of 20-AWG enameled wire
	C28:	86pF, 2.5kV padder, FW Capacitors AP031HV
12MHz	L2:	2.93μH, Micrometals T200-2 toroid (2-in O.D.) with 14 turns of 20-AWG enameled wire
	C28:	60pF, 2.5kV padder, FW Capacitors AP031HV
13.56MHz	L2:	2.93μH, Micrometals T200-2 toroid (2-in O.D.) with 14 turns of 20-AWG enameled wire
	C28:	47pF, 2.5kV padder, FW Capacitors AP031HV

Table 2. Tuning components.

Driver

The EL7144Cs provide sufficient drive for the ARF440 and ARF441 at frequencies up to 4MHz. Operation at higher frequencies requires a driver with a higher current rating and lower resistance.

The driver consists of two complementary pairs (Q1-Q2 and Q3-Q4 in Figure 1). The prototype uses Siliconix 2N7016 and 2N7012, which are in quarter-size DIP packages. A variety of similar complementary MOSFETs can also be used (e.g., IRFD110, IRFD9120).

The prototype provides adjustable bias for each MOSFET. The objective of the bias voltage is to place the gate voltage just below the threshold. Thus R12 is adjusted to set the gate of Q2 at 3V, while R10 is adjusted to set the gate of Q1 at V_{DD2}-3V. Adjustment is not critical and these potentiometers can be replaced by fixed dividers.

A supply voltage of V_{DD2}=12V provides sufficient drive for the final amplifier. This voltage is conveniently the same as V_{DD1}.

Final Amplifier

The final amplifier is based upon the ARF440 and ARF441 symmetric-pair MOSFETs. The quiescent currents are individually adjustable via R18 and R20 and should be set to about 0.1A each (i.e., just on the verge of conduction). This results in gate bias of about 3.5 to 3.8V.

The variable gate biases provide a convenient means of checking final MOSFETs Q5 and Q6 during development. The ac coupling also provides some isolation of the driver MOSFETs in case of a short-circuit failure of the final MOSFETs. It is, however, possible to simplify the circuit by direct-coupling the output of the driver to the gate of the final. If this is done, the bias on Q2 and Q4 should be increased slightly to ensure that Q5 and Q6 are cut-off in the absence of an input signal.

Output transformer T1 is constructed by winding #22 insulated wire through one block of CMD5005

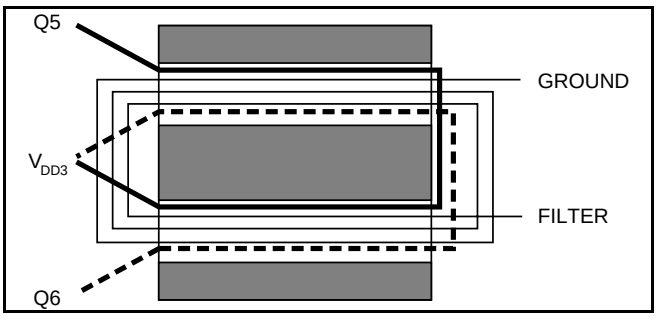

Figure 2. Construction of Output Transformer T1.

ferrite as shown in Figure 2. The use of different colors facilitates identification of the leads. The VSWR and overrating factor are less than 1.9 and 1.5, respectively, from 1 to 14MHz. Capacitors C26 and C27 ensure a good RF ground at the center of the primary winding. Inductor L1 keeps RF out of the power-supply line; its value is not critical.

The prototype uses simple series-tuned circuits (Table 2) with *Q* =5 at the frequency of operation (except that the 13.56MHz inductor is used at 10 and 12MHz). Tuning is accomplished by adjusting padder C28 for maximum output power or maximum dc-input current. Other output filters or matching networks can be used provided they include a series inductor on the transformer side to prevent current from flowing at the harmonic frequencies.

4. LAYOUT

The general layout of the principal components is shown in Figure 3. MOSFETs Q5 and Q6 are separated by about 0.8 inchs so that their drain leads are aligned with the leads from T1. The drivers and pre-drivers are installed roughly in line with the leads from Q5 and Q6.

The prototype breadboard is constructed on a 6.5 inchs by 8 inchs piece of PC board. All wiring is done on or above the surface to simulate a PC board with traces on one side and a continuous ground plane on the other.

For convenience in experimentation, U1, U2, Q1, Q2, Q3, and Q4 are socketed. Socketing is not, however, recommended for a final layout as it adds inductance between active devices.

The input to U1 and U2 is high-impedance and therefore not especially critical. Chip capacitors C5, C6, C9, and C10 are installed as close as possible to the power-supply leads. A clip-on heat sink is placed over each IC to provide adequate heat dissipation.

The pre driver outputs are connected to the driver inputs through short, wide (low-inductance) traces. Chip capacitors C16 and C21 are again installed as close as possible to the drain leads from Q1 and Q3. The outputs of the drivers are connected to the gates of Q5 and Q6 through short, wide traces. A clip-on heat sink is placed over each pair to provide adequate heat dissipation.

The heat sink is mounted flush with the bottom of the PC board. Holes are cut for Q5 and Q6, but the integrity of the ground plane is otherwise not interrupted. Connection pads are cut near the gates and drains. The leads of Q5 and Q6 are trimmed at the point they narrow and then bent downward slightly to contact the PC board.

Output transformer T1 lies flat on the PC board and is held in place adequately by its leads. Tuning elements L2 and C28 are supported on plastic L brackets.

5. PERFORMANCE

Tuned Output

A tuned output is used for transmitters and

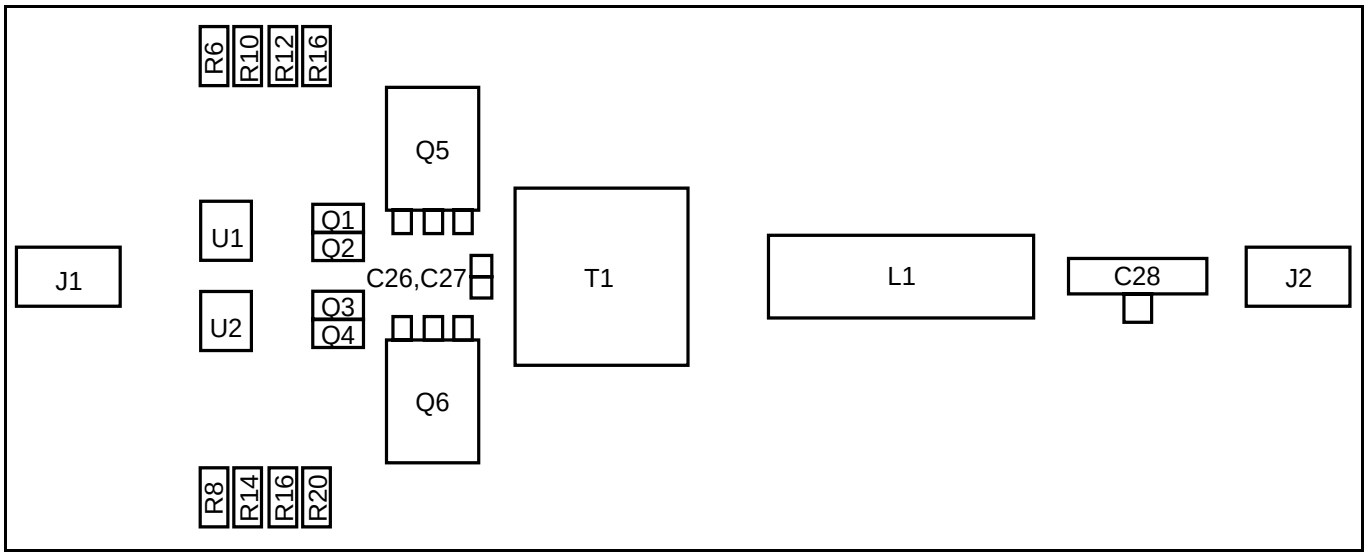

Figure 3. General Layout of Amplifier (not to scale)

resonant loads. The series-tuned output reduces the levels of the harmonics so that they contribute negligibly to the output power, which is measured by a Bird 4421 wattmeter.

The waveforms at 1.8, 7, and 13.56MHz are shown in Figures 4, 5, and 6. The waveforms include the predriver output v_{EL}, final gate v_{GS}, final drain v_{DS}, transformer output v_S and filter output v_O. All waveforms except v_S are obtained with V_{DD}=40V; v_S is obtained with V_{DD}=20V to avoid clipping by the oscilloscope.

Turn-on begins shortly after the gate voltage begins to rise and flattens the driving waveform because of the Miller effect and inflation of the gate-drain capacitance. The transients in v_{EL} and v_{GS} are probably due to the length of wire connecting the driver and gate, and/or the voltage developed across the internal inductances of the MOSFETs.

The transients in the drain voltage are the normal consequence of the MOSFET switching faster than the rise time of the transformer. The transient frequency of 56MHz corresponds roughly to the resonance of the 155pF typical drain capacitance and the measured 40nH of transformer inductance. The peak voltage remains well within the ratings of the ARF440 and ARF441. The transient is prevented from reaching the load by the output filter.

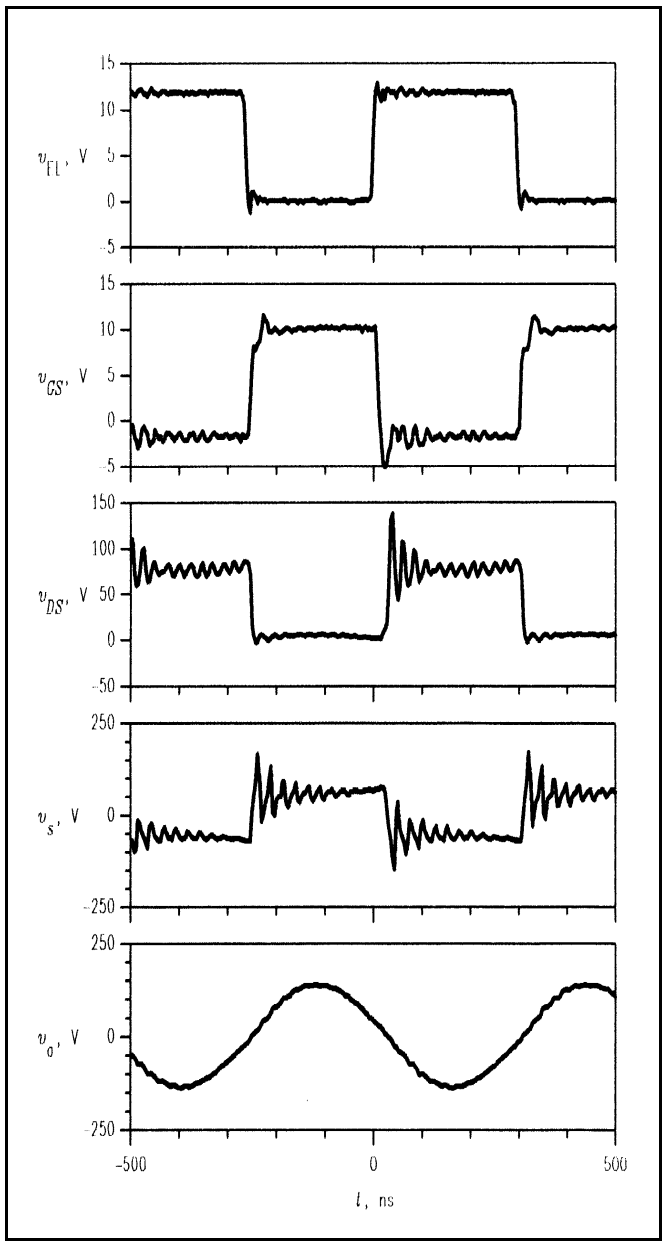

Figure 4. Waveform for Tuned Load at 1.8MHz

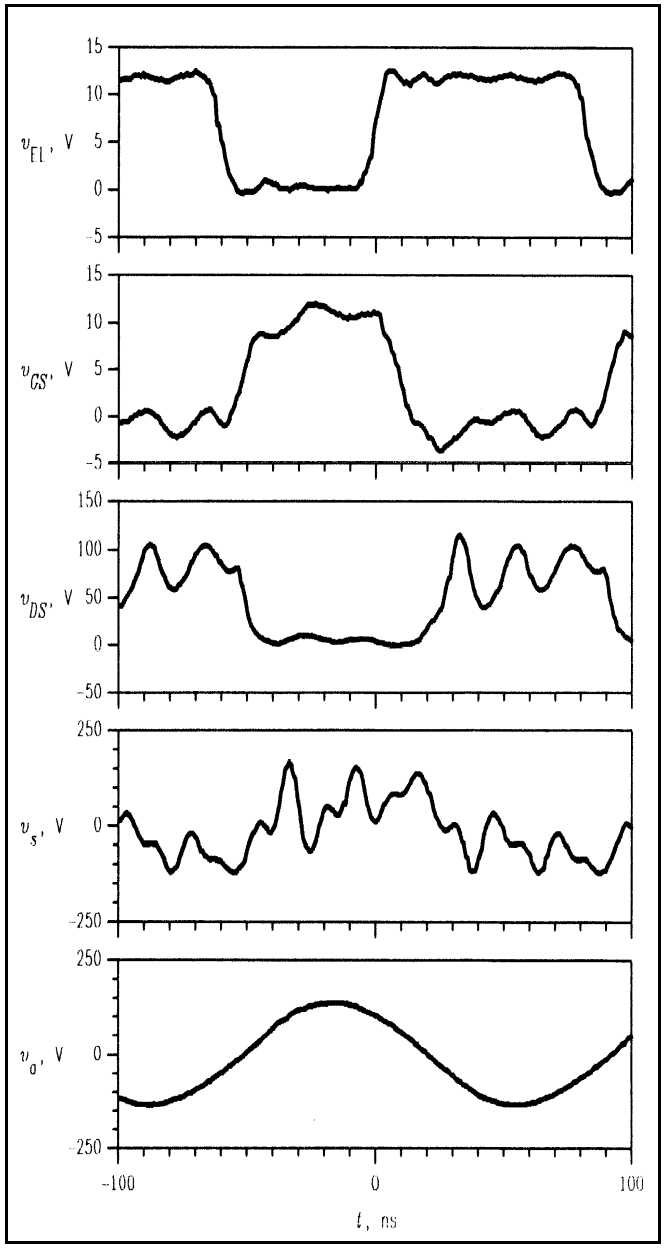

Figure 5. Waveform for Tuned Load at 7.0MHz

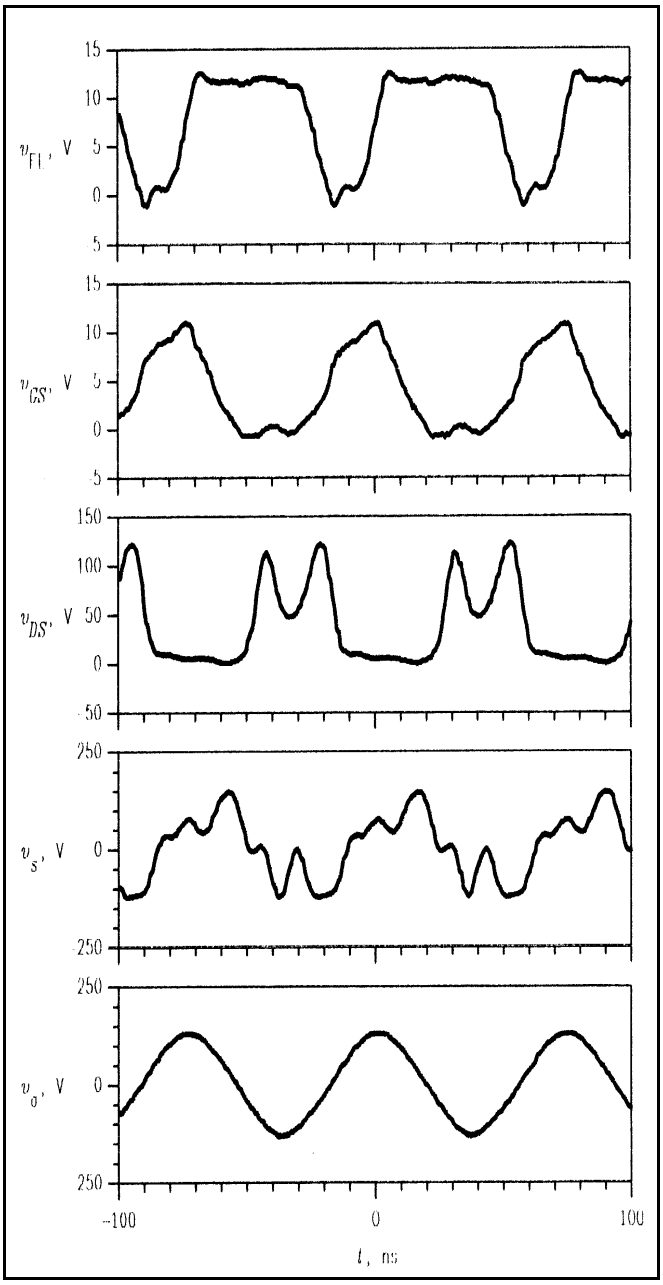

Figure 6. Waveform for Tuned Load at 13.56MHz

The variations of efficiency and power output with frequency are shown in Table 3 and Figure 7. Also included are predictions of performance for V_{DD}=50V. These are based upon on resistance, switching time, and drain capacitance, but do not include losses from the transformer and output filter. The measured efficiency is based upon measured RF output and dc input to the final amplifier (Q5 and Q6) and include *all* losses.

At the lower frequencies, V_{DD}=50V. The power output and efficiency are in excellent agreement with the predictions, especially with a few percent of loss in the transformer and filter added. At higher frequencies, the efficiency is a little less than expected and V_{DD} must be reduced slightly (Table 3) to maintain safe drain currents (i_{Dmax}≤11A, I_{dc}≤7A). The output power drops accordingly. The most probable explanation of the lower-than-expected efficiency at higher frequencies are imperfect timing of the drive and the long tail in the turn-on of the MOSFET.

The variations of efficiency and output voltage with supply voltage are shown in Table 4 and Figure 8. In contrast to class-A and -B PAs, the efficiency remains relatively constant and high for all output levels. The highest efficiency generally occurs at mid-range supply

f, MHz	V_{DD}, V	I_{DC}, A	P_i, W	P_o, W	η
1.8	50.0	6.55	327.5	273.0	0.833
3.5	50.0	6.83	341.5	274.0	0.802
7.0	48.6	6.85	333.0	250.0	0.751
10.0	45.0	6.74	303.5	206.3	0.679
12.0	40.0	6.72	268.6	184.8	0.688
13.56	45.0	6.72	302.6	184.7	0.610

Table 3. Power Output and Efficiency for Tuned Load.

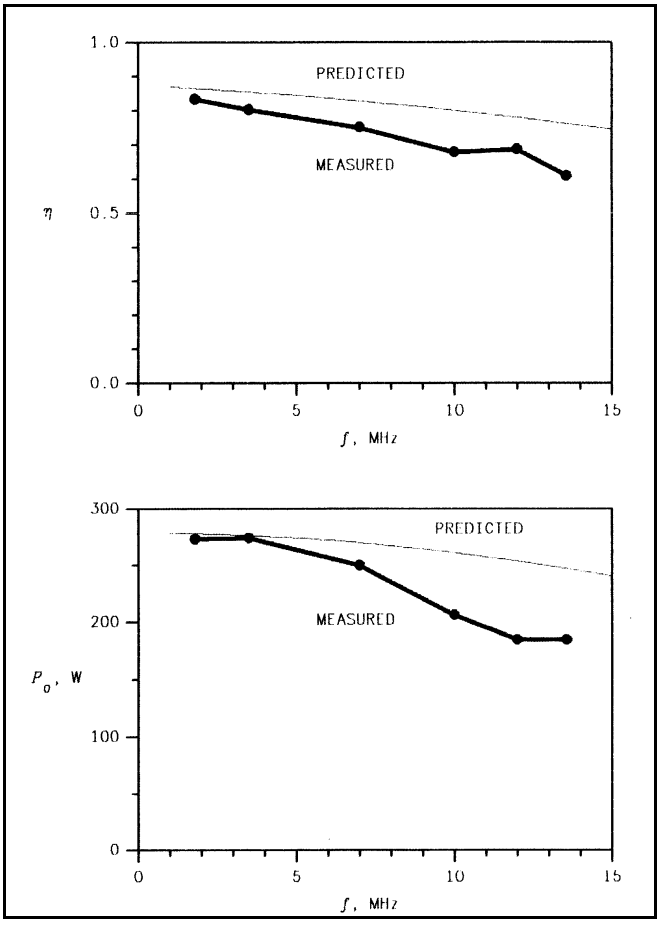

Figure 7. Efficiency and Output versus Frequency for Tuned Load

V_{DD},V	1.8 MHz		7.0 MHz		13.56 MHz	
	v_{om}, V	η	v_{om}, V	η	v_{om}, V	η
10	34.4	0.823	34.6	0.705	36.7	0.573
20	68.6	0.845	69.6	0.751	69.2	0.613
30	102.4	0.853	102.3	0.745	101.1	0.645
40	135.0	0.847	133.4	0.755	125.4	0.626
45	149.7	0.837	148.0	0.753	135.9	0.610
47.8	158.1	0.833				
48.6			158.1	0.751		
50	165.2	0.833				

Table 4. Output Voltage and Efficiency for Tuned Load.

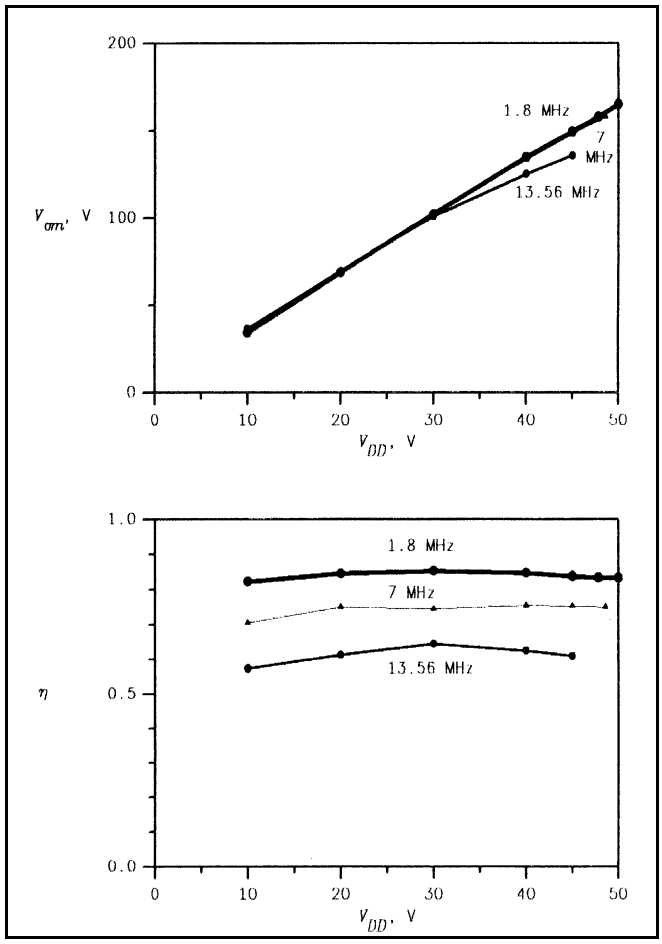

Figure 8. Efficiency and Output versus Supply Voltage for Tuned Load

voltages because the drain capacitance is reduced but the current is not yet high enough to increase R_{on}. The linearity for control and modulation is generally excellent.

Untuned Output

Untuned operation is used to deliver the maximum raw RF power to a resistive load. Tuning components L2 and C28 are omitted and the transformer output connected directly to the load. The measured output power includes all harmonics and is obtained from the rms voltage measured by an HP 54503 oscilloscope.

Because both the drain voltage and the drain current are square waves, this mode of operation can provide 27 percent more RF power than tuned class D. In an ideal square wave, 81 percent of the power is at the fundamental frequency and 19 percent is in the harmonics. The peak drain current and dc-input current are (ideally) equal.

The waveforms for 1.8, 7, and 13.56MHz are shown in Figures 9, 10, and 11. All of these waveforms are obtained with V_{DD}=40V. Transients are still present in the drain waveform, but are greatly reduced in the output waveform because of the resistive loading (in contrast to the high impedance for tuned operation).

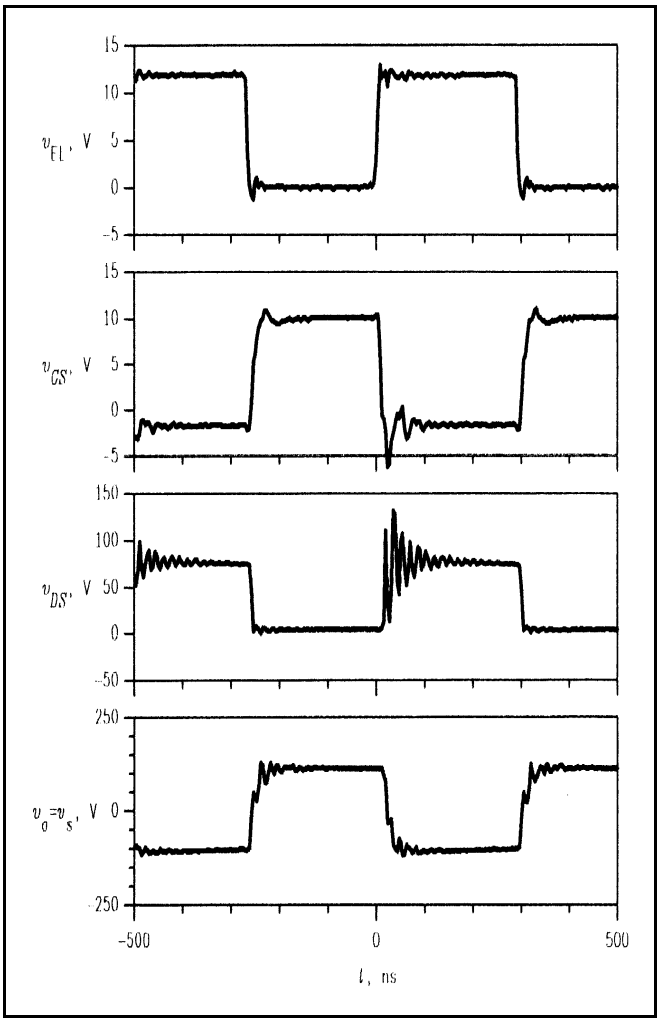

Figure 9. Waveforms for Untuned Load at 1.8MHz

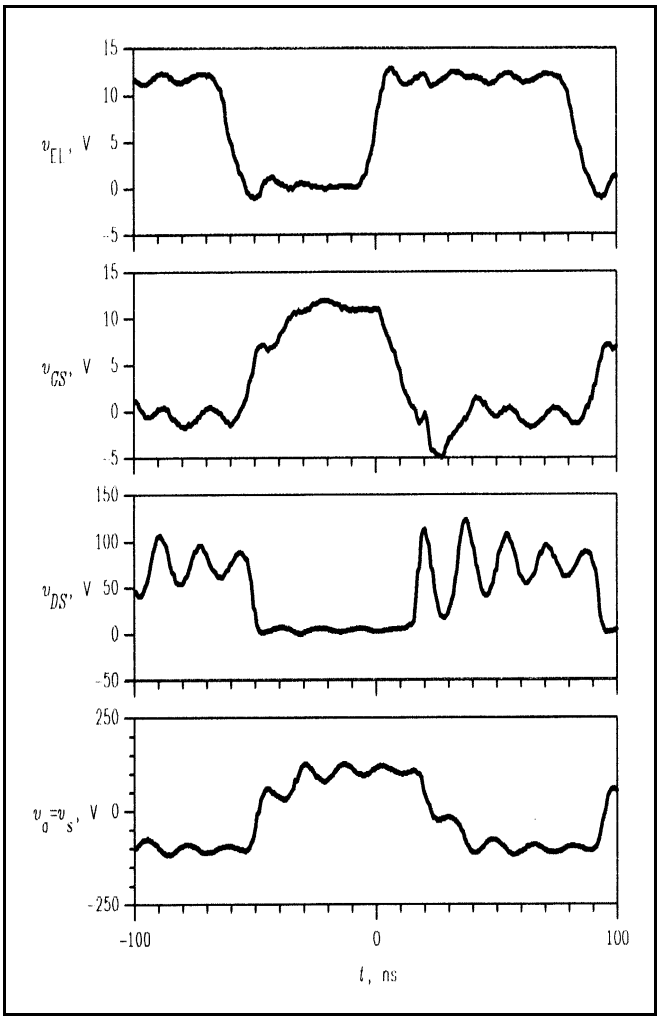

Figure 10. Waveforms for Untuned Load at 7.0MHz.

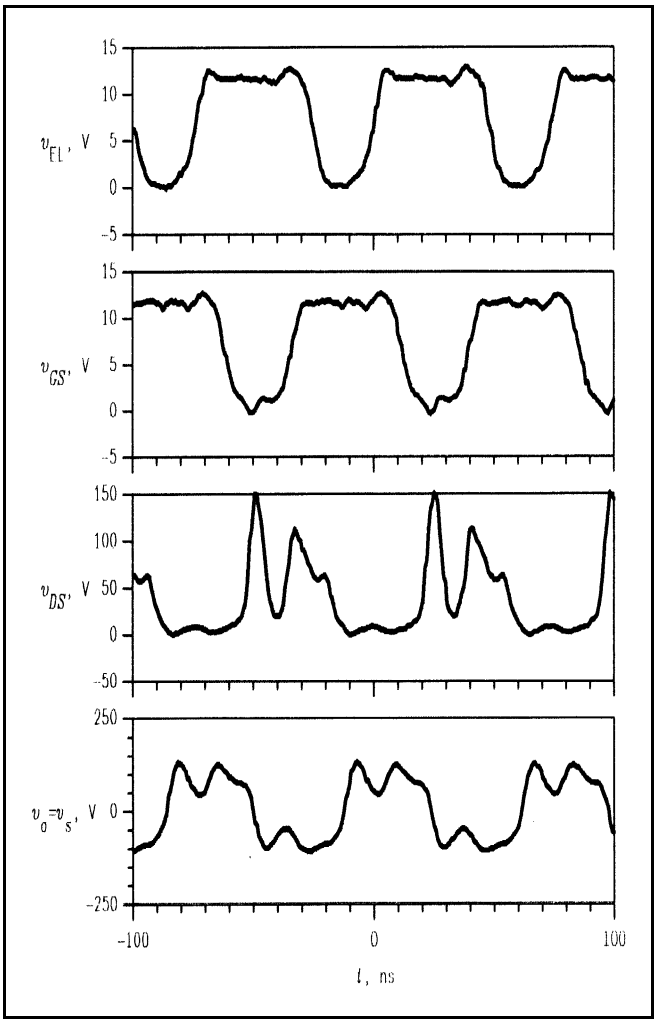

Figure 11. Waveforms for Untuned Load at 13.56MHz.

The efficiency and power output are shown as functions of frequency in Table 5 and Figure 12. At the lower frequencies, V_{DD}=50V produces outputs over 300W with efficiencies of 85 percent. At the higher frequencies, V_{DD} is increased to maintain an output of 250W. Slightly higher efficiencies are generally obtained for outputs of about 100W.

Driver

The power consumption of the pre driver and driver are given in Table 6. The power dissipations are slightly above those for static air and no heat-sinks. However, the use of the clip-on heat sinks and some moving air has afforded reliable operation.

The driver current is roughly twice that required to charge the gate capacitance, so some shoot-through current (both MOSFETs on simultaneously) is no doubt present. This can probably be reduced by lowering the gate biases.

6. COMMUNICATION APPLICATIONS

The power amplifier and driver can be keyed for CW transmission by interruption of either the RF drive or the dc supply. Amplitude modulation is very linear (Figure 8) and can be accomplished efficiently by a class-S modulator [4], [5]. Production of single sideband and other complex signals can be accomplished by the Kahn envelope-elimination-and-restoration (EER) technique [6] [7].

7. RECOMMENDATIONS

The proof-of-concept prototype described here demonstrates that this simple and inexpensive PA can produce significant power with good efficiency at frequencies up to 13.56MHz.

f, MHz	V_{DD}, V	I_{DC}, A	P_i, W	P_o, W	η
1.8	50.0	7.50	375.2	323.6	0.862
3.5	50.0	7.00	350.0	297.1	0.849
7.0	51.5	6.13	315.4	252.1	0.799
10.0	55.0	5.94	326.7	249.5	0.764
12.0	52.1	5.77	329.2	250.4	0.761
13.56	61.9	6.31	363.2	245.5	0.676

Table 5 Power Output and Efficiency for Untuned Load.

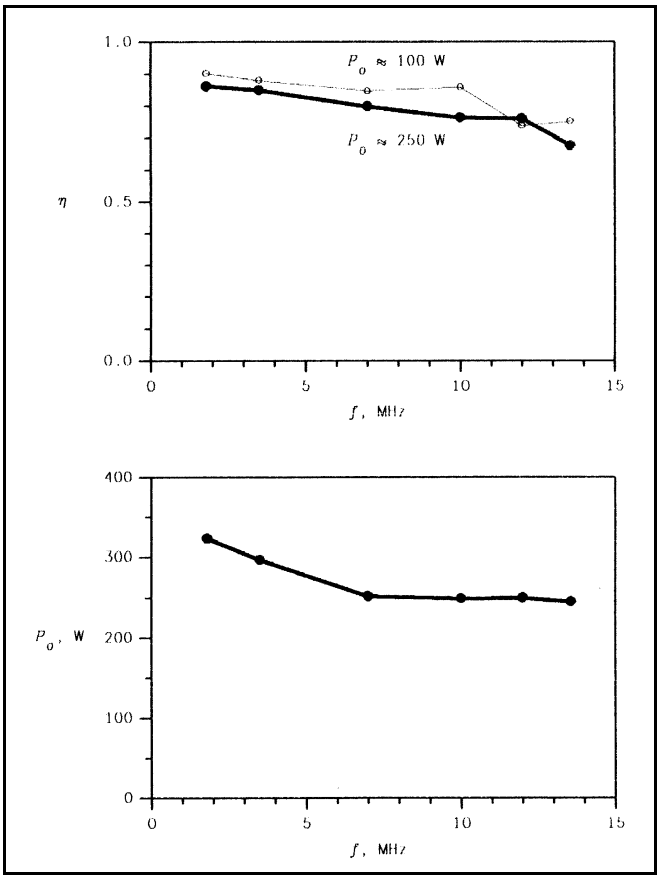

Figure 12. Efficiency and Output versus Frequency for Untuned Load

f, MHz	I_{dc1}, A	P_{i1}, W	I_{dc2}, A	P_{i2}, W
1.8	0.11	1.32	0.18	2.16
3.5	0.16	1.92	0.32	3.84
7.0	0.27	3.24	0.62	7.44
10.0	0.32	3.84	0.82	9.84
12.0	0.40	4.80	1.10	13.2
13.56	0.45	5.40	1.25	15.00

Table 6. Power Consumption of Drivers.

It should nonetheless be possible to improve both efficiency and power output at the higher frequencies. The following additional efforts are therefore recommended:

- Add monostable (timer) circuits to the predriver so that both the phase and the width of the driving pulses can be controlled.
- Identify and test suitable complementary pairs for the driver.
- Prepare a new PC board with broad, low-inductance traces connecting the driver output and ARF440/ARF441 gates. Use surface mounting rather than sockets.

The ARF440 and ARF441 have ratings sufficient to support an output of 500W or more. To obtain this will require the improved driver and a different load line, as well as some other changes in components. The following additional efforts are therefore recommended:

- Implement a new transformer for a 12.5Ω load line and compare its performance to that of a transmission-line transformer.
- Using the selected 12.5Ω transformer, test operation at outputs up to 500W with supply voltage up to 100V.

The switching times of the ARF440/ARF441 suggest that full-power operation (in class B) is possible to frequencies as high as 30MHz. This will require the transmission-line transformer mentioned above. The following efforts are recommended.

- Implement a conventional drive circuit using a transmission-line transformer and gate swamping.
- Test the PA in both class-D and class-B operation (similar to [2]).

8. REFERENCES

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APPENDIX A. SWITCHING CHARACTERISTICS OF ARF441

The basic switching characteristics of the ARF441 and the complementary driver are shown in Figure 13. For this test, the driver and pre driver are connected as shown in Figure 1. However, the drain of Q6 is connected to V_{DD3} through a 12.5Ω RF load resistor.

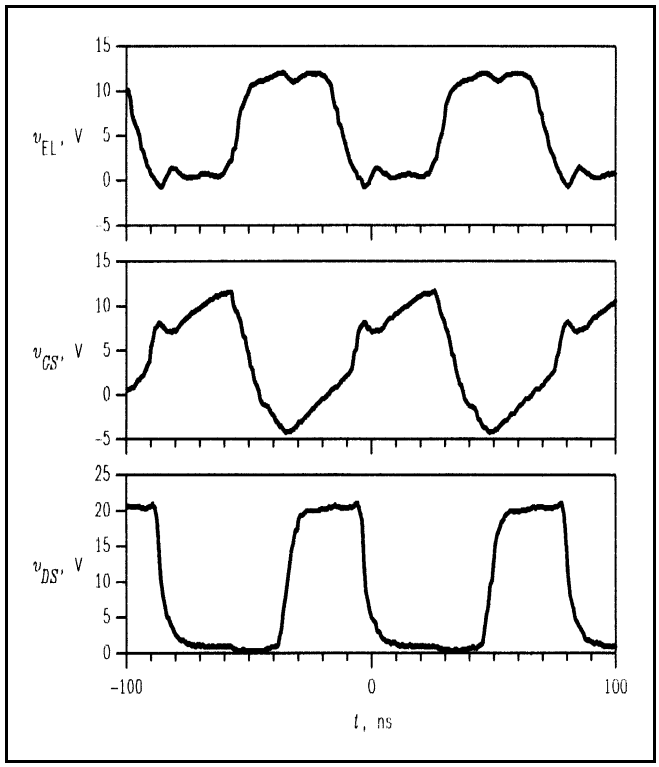

Figure 13. ARF441 Switching Characteristics.

The turn-on time is on the order of 6 to 7ns and suggests that full-power operation in class B is possible to frequencies as high as 30MHz. However, turn-off is delayed by about 11ns longer than turn-on.

The MOSFET is biased at its threshold voltage, so the turn-on and turn-off transitions involve the same voltage change. However, the gate-drain capacitance is considerably smaller during turn-on than turn-off, resulting in a shorter transition. Transients may also contribute to this difference.

The difference in turn-on and turn-off delays has important implications for operation of the amplifier at frequencies above about 7MHz. Drive signals with 50:50 duty ratios cause Q5 and Q6 to be on simultaneously during a portion of the RF cycle. The resultant build-up of current in T1 produces large transients and inefficiency. This problem is avoided by adjusting the predriver to produce shortened drive pulses so that the final MOSFETs operate with 50:50 duty ratios.

The long tail in the turn-on characteristic appears to be associated with the slower increase in gate voltage as the MOSFET nears the linear region and the gate-drain capacitance inflates. It results in a higher effective on resistance for a period of time, hence lower efficiency at higher frequencies. (This effect is called "RF-saturation voltage" in BJTs.) The long tail can probably be made shorter by a better driver.

405 S.W. Columbia Street
Bend, Oregon 97702 USA
Phone: (541) 382-8028
Fax: (541) 330-0694
http://www.advancedpower.com

Parc Cadera Nord - Av. Kennedy BAT B4
33700 Merignac, France
Phone: 33-557 92 15 15
Fax: 33-556 47 97 61

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