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APPLICATION NOTE

INNOVATIVE MOUNTING TECHNIQUES ENHANCE THERMAL PERFORMANCE OF THE SURFACE-MOUNT D^3 PAK PACKAGE

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INNOVATIVE MOUNTING TECHNIQUES ENHANCE THERMAL PERFORMANCE OF THE SURFACE-MOUNT D^{3}PAK PACKAGE

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ABSTRACT

The D^{3}PAK surface-mount power package accommodates silicon chips with dimensions up to 416 x 270 mils. Such chips, when housed in the TO-247 package, can dissipate up to 360W at a case temperature of 25°C. However, these same chips are limited to less than 7W at 25°C ambient, when housed in a D^{3}PAK and soldered to a standard FR-4 printed circuit board (PCB). Clearly, any technique capable of boosting the D^{3}PAK dissipation capability nearer to the TO-247 benchmark merits close attention.

This paper will compare the thermal performance of various mounting methods for the D^{3}PAK including classic surface mount device (SMD) printed circuit board mounting, insulated metal substrate (IMS) mount down, with and without an attached heat sink, oven fired ceramic substrate, with and without heat sink, direct bonded copper (DBC) substrates, with and without heat sink.

The importance of optimized bonding will be explored, independent of the actual substrate used, covering choice of appropriate solder alloys and fluxes, as well as the layout of the interface metallization patterns to preclude voiding during reflow operations.

Finally, a relative cost versus performance evaluation will be presented on the various methods described in the paper.

INTRODUCTION

The development of the D^{3}PAK was motivated by a demand for a surface mountable package with a higher power dissipation than the D^2. The larger D^{3}PAK addresses the increased power demand by it's ability to accommodate larger die, about 400 mils by 300 mils. The larger die reduces power losses in the device by providing lower ON resistance ($R_{DS(ON)}$) for MOSFETs or lower

forward voltage drop for diodes. Also, the D^{3}PAK with its large die results in lower thermal resistance allowing for more efficient removal of the heat generated.

MOUNTING AND SOLDERING

By definition, surface mounting a power semiconductor implies the attachment of a purposed-designed SMD, like the D^{3}PAK, to a heat dissipating arrangement through means other than the traditional screw, rivet or spring clip. In the great majority of cases, this attachment is via a soft solder joint between the pre-tinned tab of the SMD and a suitable landing pad on an appropriate substrate. Since the substrate normally must electrically isolate the circuit from the equipment chassis, it is generally made from a copper clad insulating material of some sort. The most commonly used materials are FR-4 glass epoxy printed circuit board (PCB) stock, insulated metal substrates (IMS), alumina or aluminum nitride ceramics (with either oven fired metallization or with DBC), and occasionally beryllium oxide. This latter material, although by far the most suitable in terms of thermal conductivity, presents serious health hazards should its dust be inadvertently inhaled. Independent of the material chosen, all connections between the circuit and SMDs are then made by etching the copper upper surface of the substrate with an appropriate pattern, in conventional printed circuit board fashion. In this way, through holes are eliminated, with all interconnections made simultaneously on a planar surface. Where power dissipation is such that additional cooling is required, the SMD/substrate subassembly may be soldered onto a copper base plate, which in turn may be affixed to a separate heat exchanger.

Rational thermal management in a power circuit equipped with conventional semiconductors is predicated on the optimized marriage between semiconductors, heat exchanger and cooling medium (natural convection, forced air, or water), as a function of maximum and minimum ambient temperatures, the need to minimize EMI and the possible onset of temperature-cycling induced thermal fatigue. The proper thermal management of SMD based equipment must be based on similar criteria, if minimum cost and long term reliability are to be assured.

In the case of surface mounted devices, because the total heat sink is often just the PCB or ceramic substrate to which the SMD is soldered, the sink to ambient thermal impedance will depend on the board or substrate material, the pad area available for heat spreading and the proximity of other heat sources. The heat transfer capacity of the system depends on the thermal conductivity of the board raw material. Table 1 lists this parameter for some of the most commonly used materials.

As previously mentioned, the tab and leads of the D^{3}PAK are preconditioned during manufacture with a solderable matte tin finish, thereby facilitating good solderability during the preferred solder reflow operation. Note that due to shadowing effects and to the difficulties in adjusting the wave height when other smaller SMD components are present on the same substrate, wave soldering is not recommended for this package. The minimum recommended footprint for the device is shown in Figure 1. After positioning on the board, the SMD is immobilized

in place, by either a previously dispensed adhesive, or the deposition of solder paste.

In the case of solder paste, because of the substantial area between the D^{3}PAK and its footprint, caution must be exercised in dosing the correct amount of paste. This is accomplished by special design of the stencil used to screen paste onto the footprint. Typically, these stencils are fashioned from either brass or stainless steel, with apertures normally corresponding to a 1:1 registration with the footprint. For the D^{3}PAK , such a registration would result in possible misalignment misalignment and might also cause "tombstoning" sue to an excess of solder. A suggested stencil layout, where openings for the paste cover approximately 50% of the footprint area, is portrayed in Figure 2 The actual pattern adopted is not at all critical, as long as it limits pad pre-coverage to about 50%. Openings for the source and gate leads are kept on a 1:1 registration.

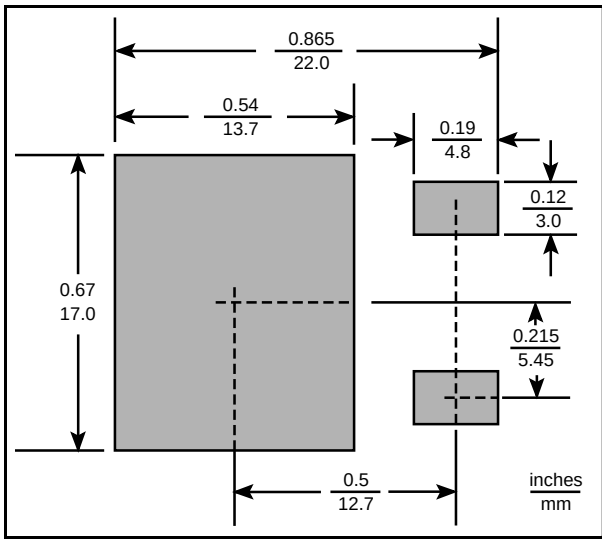

Figure 1. Minimum Recommended Footprint for the D^{3}PAK.

Material	Thermal Conductivity W/m•K	Percent Improvement Over FR-4
Glass Epoxy, FR-4-G10	0.37	----
Alumina	24	65
Aluminum Nitride	170	459
Beryllia	265	716
IMS (dielectric only)	3	8

Table 1. Thermal Conductivity of Commonly Used Materials.

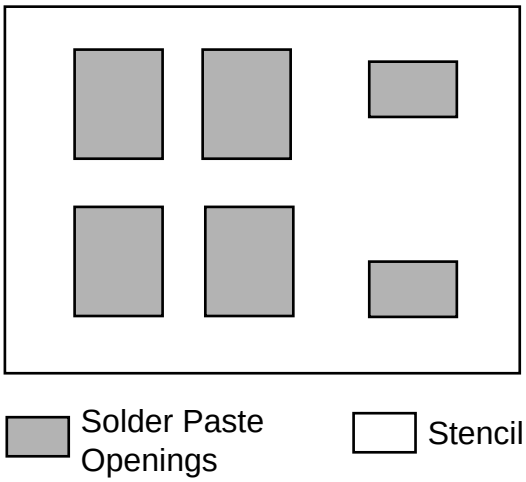

Figure 2. Recommended Solder Stencil Pattern for the D^{3}PAK.

The actual solder paste used for this operation contains in fact only about 70% solder, the rest being a binder consisting of an activator (usually "half-active" flux), solvent and a thickener-lubricator mix. The solder itself is most often 62% lead, 36% tin and 2% silver but is sometimes straight 60% lead, 40% tin. Constituent particles are typically of 300 mesh size and nominal solidus/liquids temperatures are 180/230°C. A high lead content is favored to reduce the risk of thermal fatigue, due to mechanical strain set up in the solder joint through temperature induced differential expansion. This paste is screened onto the substrate with a thickness of 8-10mils.

Reflow soldering methods generally usable for D^{3}PAK mount down are;

- Convection heated reflow, in a tunnel oven
- Combined convection/infrared reflow, also in a tunnel oven
- Vapor phase reflow

Other techniques, such as Pulse-heating with a gas fired collect tool, or even hand soldering, are less relevant to the D^{3}PAK than to smaller SMDs, given the high thermal masses involved and the large interface areas to reflow.

In all cases, meticulous preparation of the board is essential, if the joint quality necessary for good thermal and electrical contact is to be achieved. Oxide should be stripped using methods applicable to the degree of oxidation present. Trichlorethane is suitable for removing light oxidation, organic acid fluxes are fine for medium oxidation, with ferric chloride being reserved for severe corrosion.

CONVECTION HEATED REFLOW

In this process, the SMD/substrate assemblies are placed on the conveyor belt of a classic convection-heated tunnel oven (belt furnace), which then feeds the parts into the reflow zone inside. Dry nitrogen is used as a cover gas, to preclude oxidation at the elevated temperatures involved. Preheat and soak time is generally in the region of 10 to 15 minutes, during which time the subassembly temperature is raised to and stabilized at about 150°C. When the parts finally enter the middle region of the oven, where temperature is regulated at 230 to 250°C, solder fusion takes place over a period of some two minutes. A further 10 to 15 minutes cool down time elapses before the finished assembly finally exits from the furnace.

It should be pointed out that these time intervals might appear excessively long to anyone familiar with the assembly of small signal hybrid circuits.

In that discipline it is not uncommon to see recommendations for preheat and cool down times in the order of two minutes each with actual reflow times limited to 20 to 30 seconds! The reason for this apparent gross disparity is that the thermal mass involved with a D^{3}PAK and its massive substrate is many fold that of a 6 pin DIP and lightweight PCB. Attachment at reflow temperature would be impossible with shorter time lapses.

CONVECTION/INFRARED REFLOW

This process is very similar to the straight convection operation just described. Substrate and SMD preparation is identical. The tunnel oven employed is fitted with infrared radiators in its center section and these raise the temperature in that zone to reflow level. Care must be exercised not to overheat any voluminous "black bodies" that may be mounted on the substrate. Like the simple convection method this enhanced process is quite suitable for D^{3}PAK assembly.

VAPOR PHASE REFLOW

In this technique the solder paste is melted by passing the boards through a hot vapor. The solder is melted as the vapor condenses on the board and its associated components. As with certain other processes widely employed for the assembly of small signal level hybrid circuits, this method leaves much to be desired when applied to high power assemblies with high thermal inertia. Efficiency is very low and there is considerable wastage of costly raw materials.

TEST SETUP

The test setup, used to evaluate the thermal resistance of the different types of mountings, consisted of a circuit which produced constant power dissipation in the device under test, see Figure 3 for a simplified schematic. The junction

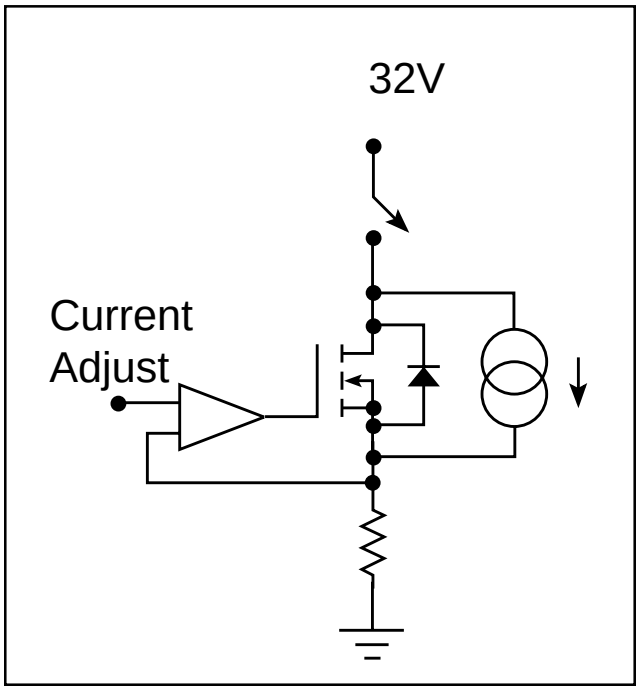

Figure 3. Simplified Test Setup Schematic.

temperature was monitored by removing the heating power once every second and forward biasing the body diode with low current and measuring the diode forward voltage to determine the junction temperature. The body diode had been previously calibrated for forward voltage versus junction temperature. The power was adjusted such that the junction temperature increased sufficiently to make the readings meaningful, about 75°C to provide a final junction temperature of about 100°C. The forward voltage of the diode was allowed to stabilize before the reading was taken.

This insured that the device and heat sink were thermally saturated and that the measurement represented the thermal resistance not the thermal impedance.

THERMAL PERFORMANCE

The power dissipation capability of the D^3PAK has two extremes, one where the device is mounted in still air with no circulation around the device and the wires connecting the device to the circuit provide no heat conduction. Under these conditions the device is only cooled by radiation and conduction into the air. The other extreme is where the device is mounted to an infinite heat sink with no thermal resistance between the package and the heat sink, making the thermal resistance junction to ambient equal to the thermal resistance junction to case. However, neither of these conditions are ever realized in the real world. The still air mounted device will always have some conduction through the wires, connecting the device to the tester and some convection cooling as the air will never be completely still. Also there is no such thing as a zero thermal resistance interface between a device and a heat sink as well as no such thing as an infinite heat sink.

The device used in the experiments was an APT4016SN. This device contains a die which is the largest die that can realistically be put in the D^3PAK (416 mils X 270 mils, 112,320 $mils^2$). The data sheet specifies the still air mounting junction to ambient thermal resistance to be 40K/W maximum. The measured still air mounting, junction to ambient thermal resistance, was 10 to 13K/W. This measurement indicates the data sheet value is quite conservative. However, the device was suspended in air by hookup wire and the air surrounding the device was not perfectly still, as there was some air movement in the room. This value will, however, be the baseline for the worst case junction to ambient thermal resistance.

To determine the best possible thermal resistance junction to sink (R_{qJS}) a device was mounted to a very flat machined water cooled copper heat sink. Thermalloy Thermalcote II compound was used to improve the thermal interface between the case and sink. This compound was used during all of the tests where a non-soldered interface was required between heat conducting parts. The data sheet specifies thermal resistance junction to case ($R_{\Theta JC}$) at 0.34K/W The measured value for $R_{\Theta JS}$ was 0.29 to 0.37K/W. This value will be used as the baseline for the best possible $R_{\Theta JS}$. The case temperature was monitored during the test and subtracted from the junction temperature to determine $R_{\Theta JC}$. The $R_{\Theta JC}$ was calculated to be between 0.19 to 0.27K/W.

PRINTED CIRCUIT BOARD MOUNTING

To determine the thermal efficiency of PCB mounting, the simplest method for mounting the D^3PAK, a board was built using FR-4, 0.0625 inches thick, with six mounting positions of three different drain pad sizes, see Figure 4. Each position had three pads, one pad of sufficient size to solder the package to and provide electrical connection for the drain and two pads for the gate and source leads electrical connections. The size of the drain pad was varied to determine how much additional cooling could be realized with a larger pad. The copper was left on the backside of the PCB to provide better heat conduction from the backside.

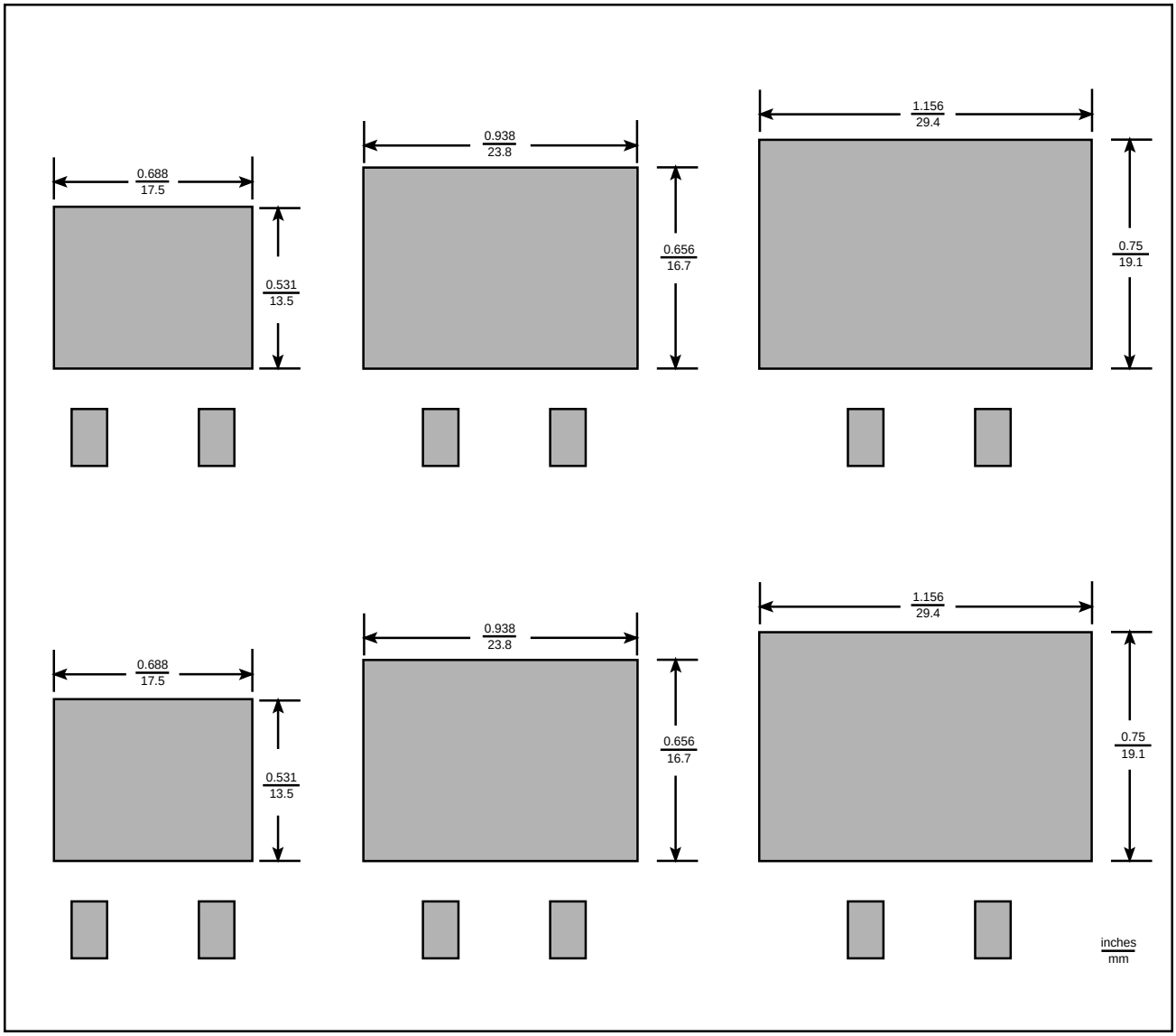

Figure 4. Printed Circuit Board Layout.

For the experiment, soldering was accomplished using a hot plate and a 63/37 tin/ lead solder with flux. Better results may have been achieved using the methods described earlier but we achieved reasonable results with our less sophisticated soldering method thanks to the design of the D^3PAK, which has a short tab extending beyond its plastic body, allowing for easy inspection of the solder fillet under the package. Unlike the TO-247 package, which is sometimes used as a surface mount package by plating the backside and forming the leads into a gull wing shape, where the solder joint is totally under the package body and it is impossible to inspect the solder joint.

The results are summarized in table 2.

As can be determined from table 2 increasing the solder pad size does indeed improve the dissipation capability of the device. However, the small amount of improvement does not justify the use of expensive board space for this purpose. The amount of improvement, shown by the figure of merit, represents diminishing returns for increased board space.

The addition of a heat sink on the backside of the PC board, under the smallest pad, see Figure 5, improved the performance by 60% over the no heat sink results, see Table 3.

The addition of the heat sink improved the performance considerably. The heat sink is costly, uses considerable volume and the amount of improvement, although substantial as a percentage, is not very significant in terms of an increased power of only 3.4 Watts.

This heat sink arrangement was subjected to forced air. First the air was forced over the heat sink only, Figure 6, and then over both the heat sink and the device, Figure 7. The results are shown in Table 4. Line 1 is the result of forcing air over the heat sink only and line 2 is the result of forcing air over both the heat sink and the device. In both cases the improvement is only marginal over the results with the heat sink with natural convection cooling.

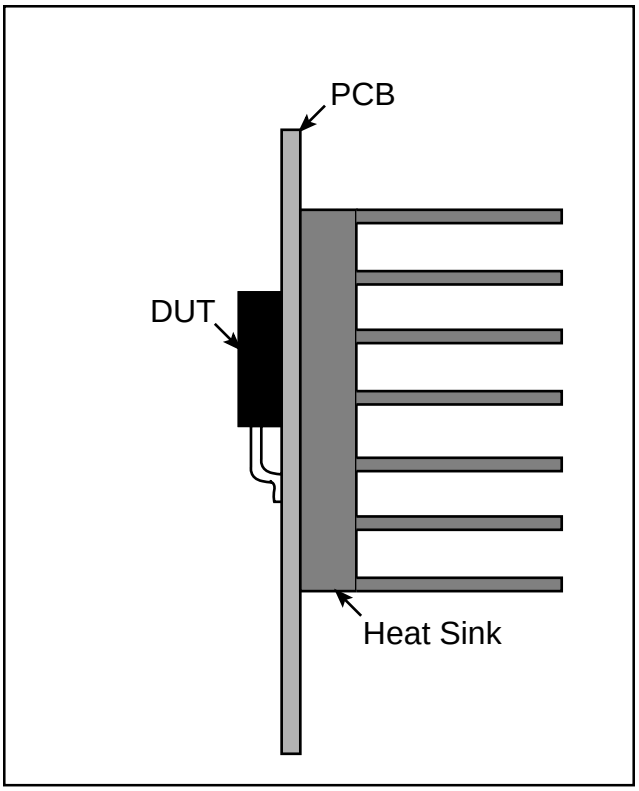

Figure 5. PCB With Heat Sink.

Pad Size mils L x W	Pad Area mils^2	$R_{\theta JA}$ K/W	Maximum Power Dissipation Watts	Figure of Merit W/inch^2
531 X 688	365,328	21.9	5.7	15.6
656 X 938	615,328	18.8	6.6	10.7
750 X 1,156	867,000	18.0	6.9	8.0

Table 2. Comparison of Pad Size on FR-4 PB, No Heat Sink

Pad Size mils L x W	Pad Area mils^2	$R_{\theta JA}$ K/W	Maximum Power Dissipation Watts	Figure of Merit W/inch^2
531 X 688	365,328	13.8	9.1	24.9

Table 3. Smallest Pad on the PCB with a Convection Cooled Heat Sink.

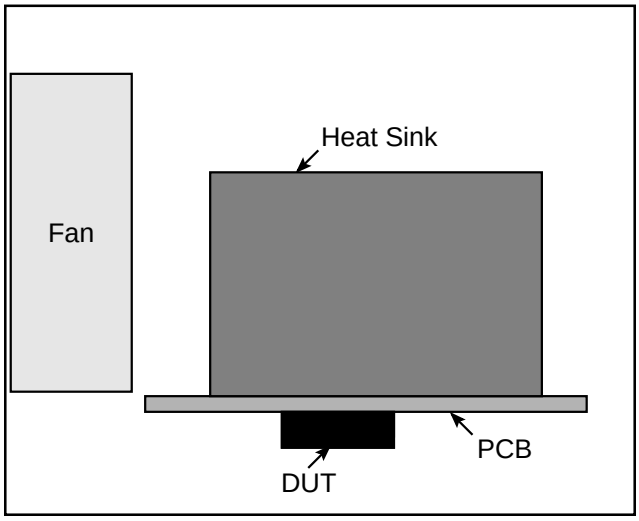

Figure 6. PCB With Forced Air on Heat Sink only.

Another method of heat sinking was tried using thin strips of copper former in a "V" shape and soldered to the largest pad as shown in Figure 8. It was necessary to use the larger pad to provide room to solder the heat sink down. The addition of this type of heat sink improved the performance by 18.8% over the same size pad without any heat sink, see Table 5.

The addition of this heat sink improved the performance only slightly. However, it would be less costly and use less volume than the backside heat sink. It does use more board space and only offers marginal improvement over the large pad without the heat sink.

To measure the best possible thermal performance, of a PCB mounted D^3PAK the smallest and largest pads were mounted to a copper water cooled heat sink. The results are shown in Table 6.

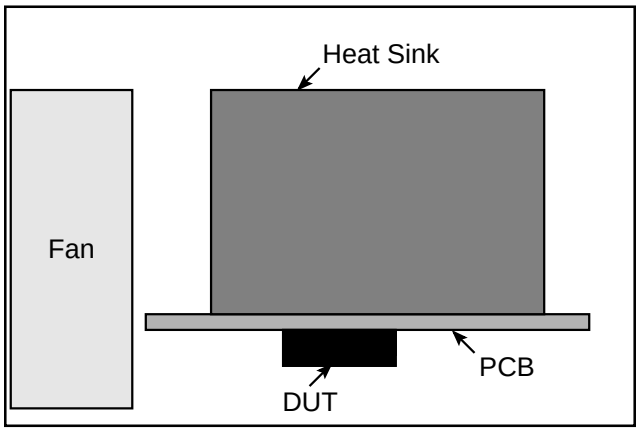

Figure 7. PCB With Forced Air on Heat Sink and device.

Pad Size mils L x W	Pad Area mils^2	$R_{\theta JA}$ K/W	Maximum Power Dissipation Watts	Figure of Merit W/inch^2
531 X 688	365,328	13.2	9.5	26.0
531 X 688	365,328	12.6	9.9	27.0

Table 4. Smallest Pad on the PCB with a Fan Cooled Heat Sink

Pad Size mils L x W	Pad Area mils^2	$R_{\theta JA}$ K/W	Maximum Power Dissipation Watts	Figure of Merit W/inch^2
750 X 1,156	867,000	15.3	8.2	9.5

Table 5. Largest Pad with "V" Shaped Heat Sinks

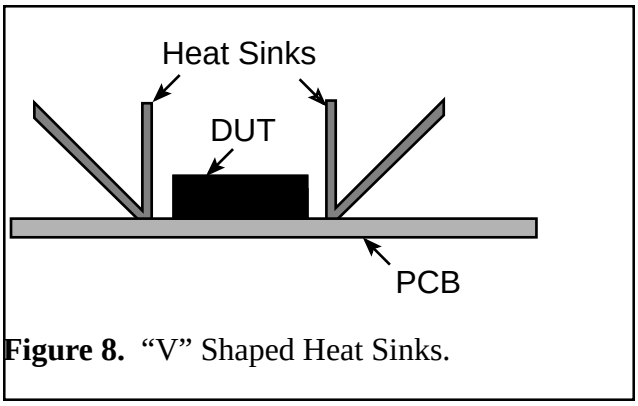

Figure 8. "V" Shaped Heat Sinks.

It should be noted that the D^{3}PAK mounted to a PCB in still air, even with heat sinks attached, is incapable of matching the thermal performance of an unmounted device is still air! The reason for this is the backside of the device is copper and having it exposed directly to air is better than covering it with a PC board. Therefore, it would seem that a device mounted vertically on the PC board would be a more efficient use of the device.

SUBSTRATE MOUNTING

Although SMD technology brings many benefits, such as lower profile assemblies and denser packaging, it is clear from the preceding section that mounting the D^{3}PAK to a standard FR-4 type PC board is not very efficient. It would be far more cost and performance effective to use a TO-247 device mounted vertically on the PC board.

To utilize the full benefit of the D^{3}PAK it is necessary to mount the device on some type of material which will provide a more efficient medium to remove the heat from the of the device.

Four different combinations of copper conductors and insulating substrates, Alumina (Al_2O_3) and Aluminum Nitride (AlN) with screen printed copper, Alumina DBC and IMS were attached to heavy copper bases. The attachment of the devices, substrates and copper bases was done with soft solder using the belt furnace method described earlier. Figure 9 shows a cross section of the D^{3}PAK mounted on the substrate and copper base.

To measure the best case conditions for the substrate mounted devices the assemblies were mounted to the water cooled copper heat sink, with the results summarized in Table 7.

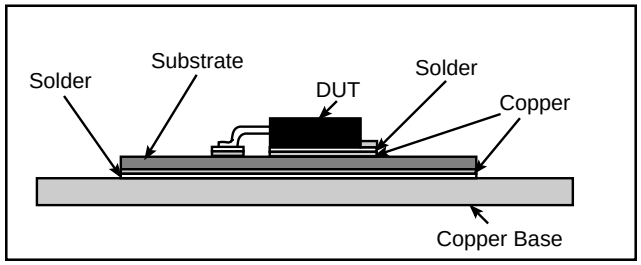

Figure 9. Cross Section of the D^{3}PAK Mounted on the Substrate and Copper Base.

Pad Size mils L x W	Pad Area mils^2	$R_{\theta JA}$ K/W	Maximum Power Dissipation Watts	Figure of Merit W/inch^2
531 X 688	365,328	11.3	11.1	30.4
750 X 1,156	867,000	7.3	17.1	19.7

Table 6. Comparison of Pad Size on FR-4 PCB with Water Cooled Heat Sink

The results followed the predicted thermal performance for the various type of substrate material. The Aluminum Nitride was the best, with the both the DBC and screen printed copper on Alumina being about the same and the IMS material the worst. There is considerable difference between the best and worst.

To measure performance with a more practical heat sink, the above assemblies were attached to the finned aluminum heat sink used in the PCB experiment. The heat sink was oriented such that the fins were perpendicular to the floor, maximizing the amount of convected air across the fins. The results are summarized in Table 8.

With the convected air cooled heat sink as the cooling media the difference all but disappears. The thermal resistance sink to ambient dominates the measurement.

POWER SUBSTRATE TRADEOFFS

A comprehensive range of substrate technologies is available, to match the particular needs of any given application. Performance factors influencing the selection process include power dissipation, operating temperature, switching frequency and the ability to withstand thermal cycling. Cost is likely to be critical too, since the best of substrate technologies in terms of pure performance are also the most expensive. The choice of an appropriate technology does not depend entirely on the application specifics, but may also be linked to the characteristics of the substrate itself.

IMS

When the isolation requirements of a particular application do not exceed 2.5kV RMS, circuit to

Substrate Type	R JS K/W	Maximum Power Dissipation Watts
Alumina Screen Printed Copper	0.36	347
Alumina DBC	0.27	463
Aluminum Nitride Screen Printed Copper	0.31	403
IMS	0.58	216

Table 7. Comparison of Different Substrate Materials with Water Cooled Heat Sink.

Substrate Type	R JS K/W	Maximum Power Dissipation Watts
Alumina Screen Printed Copper	1.37	91.2
Alumina DBC	1.23	101.6
Aluminum Nitride Screen Printed Copper	1.39	90.0
IMS	1.41	88.6

Table 8. Comparison of Different Substrate Materials with Air Cooled Heat Sink.

base plate and where power dissipation is low an IMS may be used. This type of substrate consists of three layers of different materials sandwiched together. A copper, steel or aluminum base plate, 0.8 to 3mm thick, is bonded to an 80µ thick polymeric insulating layer, which in turn is capped with a copper layer, 35 to 300µ thick. This approach combines design simplicity with fast processing and low cost. IMS technology is limited, however, by the maximum value of isolation voltage that may reasonably be obtained without an excessive increase in thermal resistance. Both parameters are of course linked to the thickness (or thinness!) of the polymeric insulator. The very thinness of this layer also impacts unfavorably on the parasitic coupling capacitance between circuit and base plate. With about 70pF/cm^2, this is a limitation on switching speed, in that it injects losses unrelated to the circuit topology.

Ceramic substrates

In applications requiring higher isolation voltages and/or operation temperature, metallized ceramic substrates are preferred. Thanks to their high dielectric strength, isolation voltage in excess of 10kV may be achieved. Varying the thickness between 0.25 and 3mm allows both isolation voltage and coupling capacitance, as well as thermal resistance, to be tailored for the application. Standard 0.635mm thick alumina (Al_2O_3) or aluminum nitride (AlN) combines a 2.5kV isolation withstand with a 10pF/cm^2 capacitance and is consequently usable at PWM frequencies above 100kHz. Beyond its beneficial effect on losses, a low value of coupling capacitance also minimizes EMI transmission to the normally grounded substrate/heat sink.

Thermal resistance is dependent not only on substrate thickness but also on the nature of the material itself. When an application demands simultaneously high isolation voltage, low coupling capacitance and best thermal performance, aluminum nitride is the obvious choice. Benefiting from, a thermal conductivity of 170W/m•K, compared to only 24W/m•K for alumina, AlN allows up to 40% higher power output than Al_2O_3. The downside of AlN is its very high cost, this being several times that of alumina.

Depending on power dissipation levels and to some degree on current density in the defined conductor traces on the substrate, there exists a choice between two separate metallization methods for use with ceramic substrates. When circuit current ratings are less than about 50 amps, screen printing is the most attractive option. Here, copper paste is screened onto the substrate and subsequently oven fired to create conductors up to 60µ thick. Screen printing yields excellent track definition, enabling the mounting of SMD and bare semiconductor chips on the same substrate. Protection and driver circuits may then be positioned close to the power switches for optimum performance and reliability. Multi layered conductors are readily produced by screen printing and the process also allows the deposition of screened power resistors directly onto the substrate. When current ratings climb much above 50 amps, it makes more sense to specify DBC metallization in place of screen printing. This process, which molecularly bonds relatively thick layers of copper to both faces of the ceramic sheet, yields substrates with superb thermal performance. The upper

metallization layer, which can be up to 0.5mm thick is then etched to match the desired circuit topology. Both screen printing and DBC technology are suitable processes for either AlN or Al_2O_3 substrates. DBC represents the best compromise between manufacturing cost and thermal performance.

Conventional FR-4 grade PCB material

The most widely used material for small signal level SMDs, the thermal performance of FR-4 is marginal when applied to potentially high power devices like the D^3PAK . In some instances, where a large semiconductor chip must be specified to handle high peak power but at low duty cycle and average power levels, this material may nonetheless be the most cost effective.

CONCLUSIONS

The D^3PAK SMD package can accommodate very large silicon chips, capable of dissipating more than 370W at 25°C case temperature. When this package is soldered onto a conventional FR-4 PCB, power dissipation plummets to about 7W at 25°C ambient.

An industry standard TO-247, mounted vertically in free air on a PCB, can dissipate more than this! It was demonstrated that, to extract a system performance more in keeping with chip capability, it is necessary to mount the D^3PAK on a substrate exhibiting far better thermal conductivity than FR-4 material and in turn attach this assembly to a suitable base plate or heat sink. Data was presented comparing the thermal behavior of a D^3PAK when mated to the most popular substrate materials. These included IMS, metallized alumina and metallized aluminum nitride ceramic substrates, the later in both over fired copper and DBC.

As expected, the results obtained are commensurate with the published thermal conductivity characteristics of the various materials, with aluminum nitride offering the best performance at the highest price, IMS the least performance at the lowest cost.

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