FREQUENCY LINEAR TUNING VARACTORS

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For several decades variable capacitance diodes (varactors) have been used as tuning capacitors in high frequency circuits. Most of these diodes have traditionally been the abrupt junction epitaxial type which have been described in many textbooks. This type of varactor is fabricated using readily available epitaxial silicon.

In the early 1970's hyperabrupt silicon varactors became available in which the capacitance - voltage curve of the abrupt junction diodes was modified by adding an N^+ layer under the junction, either by ion implantation, by an additional diffusion, or an additional epitaxial layer. This had the effect of increasing the capacitance ratio, and improving the linearity of the frequency-voltage curve.

With the introduction of programmed silicon epitaxy in 1980 an improved type of hyperabrupt silicon tuning diode was developed. The epitaxial reactor could be programmed to produce epitaxial silicon which yielded varactors with precisely controlled C-V curves of almost any shape. This technology, combined with our standard thermal-oxide passivated mesa process was used to produce tuning diodes which could be optimized for the best combination of high tuning ratio, high Q, and almost perfect linearity of frequency versus voltage.

This type of diode has been used since 1980, in many applications such as bipolar VCO's, FET VCO's, Gunn VCO's and tuneable filters. In most cases it has been possible to completely eliminate the use of linearizers, with resulting savings in size, weight, and cost, without giving up the traditional stability of thermal-oxide passivated silicon mesa varactors.

Now, these improved silicon diodes are available and are marketed as "Frequency Linear Tuning Varactors" or FLTVARs for short.

AVAILABILITY OF FLTVARS

This catalog shows the availability of FLTVAR chips with junction capacitance (at 4 volts) from 0.7 pF to 48 pF and sensitivities(s) of 8 or 11 percent per volt. These are available from stock for immediate delivery in small quantities. However, both higher and lower values of capacitance are available, as well as tuning ranges larger than 20 volts. (It is even possible to design diodes that have customized C-V curves to compensate for the parasitics of a particular circuit.) So, if our catalog does not show the exact diode you would like to have, contact our applications department to discuss your requirement.

Mechanically, these diodes are supplied as thermal oxide passivated chips from 15 to 30 mils square and 4 to 6 mils thick with gold back metalization. Either one mesa or four mesas per chip can be provided (with gold bonding pads). Mesa diameter depends on the junction capacitance. Although these chips can be supplied in any of our standard packages, we don't recommend this, because of the detrimental effect of the package capacitance on the linearity. It is best to bond the chips directly into the circuit, if possible.

THE DEFINITION OF S (RELATIVE SENSITIVITY)

The resonant frequency of simple series L-C circuit is given by the well known formula.

$$f = \frac{1}{2\pi\sqrt{LC}}$$

If the capacitor is replaced by a varactor whose junction capacitance is a function of voltage, then the resonant frequency will be a function of the reverse voltage on the varactor:

$$f(V) = \frac{1}{2\pi\sqrt{LC_j(V)}}$$

For many applications it is desirable for such a circuit to tune linearly. That is, the resonant frequency should be a straight line function of the reverse voltage across the varactor, and the idealized straight line can be expressed in terms of a parameter "s" which we call the (relative) "sensitivity".

$$f(V) = f_0(1 + sV)$$

This particular parameter is chosen because it turns out to be dependent only on the properties of the variable capacitance device, but independent of the series inductance, so it can be used to characterize a varactor. The number, s, can be considered the percent increase in frequency per volt. That is, if s = .11, the frequency will increase by 11% for each volt of reverse bias.

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In general, s may not be constant, as in the ideal case, but might be a function of voltage. In that case, s is defined as the slope of the graph of (f/f0) versus voltage. That is

$$s\,(V) = \frac{1}{f_0}\left(\frac{df}{dv}\right) \qquad \text{(definition)}$$

These equations can be combined to give you an equation for s in terms of the diode C-V curve alone:

$$s\,(V) = \frac{d}{dV}\left(\frac{\sqrt{C_{j0}}}{\sqrt{C_{j(V)}}}\right)$$

where C_{J0} is the varactor capacitance at zero volts. This defines the sensitivity for any varactor diode as a function of reverse voltage.
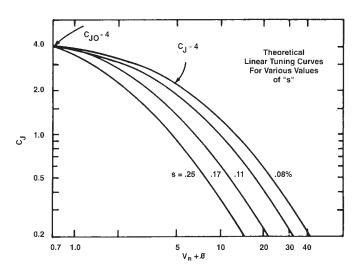
For the ideal case of linear tuning in a simple L-C circuit you would want a diode having a C-V curve with constant S. If this is the case, the C-V curve must follow the equation:

$$Cj(V) = \frac{C_{j0}}{(1+sV)^2} \qquad \text{(FLTVAR)}$$

It should be noted that the C-V equation for a constant sensitivity (Frequency-Linear) tuning varactor is mathematically similar to the C-V equation for an abrupt junction varactor:

$$C_j\,(V) = \frac{C_{j0}}{\left(1+\frac{V}{\theta}\right)^{\gamma}}$$

The difference is that in this equation, gamma (γ) is an adjustable parameter, typically .45 for an abrupt junction, which can be modified by various fabrication methods. However, ϕ is the temperature dependent contact potential between the p-type and e-type doped semiconductor regions. At room temperature it is about 0.7 volts in silicon and 1.2 volts in GaAs. In other words ϕ has a value which cannot be changed appreciably by a diode designer, except by changing to another semiconductor material.

SILICON VS GALLIUM ARSENIDE

While it is true that gallium arsenide diodes typically have higher Q than silicon diodes, this doesn't necessarily result in better performance. It would be expected that substituting gallium arsenide tuning diodes for silicon ones in a VCO would result in better FM noise because of the higher Q. Instead, the FM noise usually gets worse due to up-conversion of surface noise. There is no known passivation for gallium arsenide which limits surface states and the associated "I/f" noise, like thermal oxide does in the case of silicon. For this reason, thermal oxide passivated silicon is a better choice for high power, or wide band VCO's than gallium arsenide, if FM noise is a consideration.

Another reason for choosing silicon is the poor stability record of gallium arsenide diodes. Because of its higher thermal resistance, gallium arsenide does not settle as fast as silicon diodes in fast VCO's, and the high surface state density in GaAs results in significant long-term drift compared to silicon.

FLTVAR VS. CONVENTIONAL HYPERABRUPTS

With modern programmed epitaxy it is possible to continuously adjust the density of N-type dopant incorporated in a semiconductor while growing the epitaxial layer, in such a way that a wide variety of C-V curves can

be produced. (In principle, any C-V curve can be matched, the only restriction being that the capacitance must continuously decrease as reverse voltage increases.) The dopant density at a distance, x, from the junction relates directly to the sensitivity of the resulting diode, as shown by the formula:

$$N(x) \sim \frac{x^{3/2}}{s}$$

In other words, to produce a diode with constant sensitivity it is necessary to grow the epitaxial layer so the dopant density N(x) follows the $x^{-3/2}$ law. Within limits, it is possible to do exactly that, and this technology, combined with our standard mesa technology, results in tuning varactors with remarkably constant sensitivity over very wide voltage ranges. This, in turn allows the construction of oscillators and filters with linear tuning over more than one octave, without resorting to any form of external linearization.

The ion implantation or double-diffusion technologies used in conventional silicon hyperabrupt TVARs is a more limited technology which does not allow as close a match to the $x^{-3/2}$ doping law. In addition, the older diodes use planar technology instead of mesa technology, and therefore are compromised in both C-V law and Q, compared to what is theoretically possible.

THE EFFECT OF PARASITIC CAPACITANCE ON SENSITIVITY

Actual circuits consist of more than just a tuning varactor and a series inductor. Parasitics, both inductive and capacitive, can effect the sensitivity of the actual circuit. The most common cases can be analyzed as either capacitance in series with the tuning diode or a capacitance in parallel. Both types of parasitic capacitance decrease the sensitivity of the circuit, but parallel capacitance has a more drastic effect on linearity. (By linearity, we mean the ratio of maximum to minimum sensitivity over the whole tuning voltage range.)

For series capacitance, Cs, the following table shows the effect of several parasitic capacitance values on an ideal frequency-linear diode with S=.11

	Tuning Voltage:			
Cs/Ci0	0	10	20	Linearity Ratio
0.5	0.37	.053	.058	1.58
1.0	.055	.070	.074	1.35
2.0	.073	.085	.088	1.20
∞	.110	.110	.110	1.00

The formula for the sensitivity of the total (diode + parasitic) in terms of the sensitivity of the junction (S_J) is:

$$S_t = \frac{S_j}{\sqrt{\left(1 + \frac{C_{j0}}{C_s}\right)\left(1 + \frac{C_j}{C_s}\right)}}$$

For parallel capacitance, Cp, the effect on the linearity is much more severe, as shown in the following table:

Cp/Ci0	0	10	20	Linearity Ratio
0	.110	.110	.110	1.00
.025	.107	.095	.079	1.35
.050	.105	.083	.061	1.72
.100	.100	.067	.040	2.50

The corresponding formula is

$$S_t = \frac{\sqrt{1 + C_p / C_{j0}}}{\left(1 + C_p / C_j\right)^{3/2}} \; S_j$$

As you can see, the effect of parallel capacitance on linearity is far more severe than the effect of series parasitic capacitance. Therefore, we recommend that frequency-linear tuning varactors be used in series resonant circuit configurations rather than parallel resonant ones. In this way, the effective capacitance of the transistor (or other device) will appear in series rather than in parallel with the tuning diode.

Finally, it should be noted that a parallel capacitance reduces sensitivity mainly at the high voltage end of the tuning range. This allows you to use a small amount of capacitance directly in parallel with the tuning varactor to compensate partly for the sensitivity variation caused by the series capacitance.

For the case Cs/Cj0=1.0, Cp/Cj0=.025 and Sj=.11, the result is:

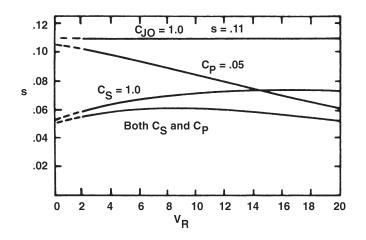| Cs/Ci0	Cp/Ci0	0	10	20	Linearity Ratio
1.0	.025	.053	.060	.052	1.15

This means, for example, that if a frequency linear diode with Cj0=5 pF is used to linearly tune a transistor whose input capacitance is 5 pF, the optimum parallel capacitance is .12 pF (a little lower than typical package capacitances). In this case, the circuit sensitivity would range from 5.2 percent/volt to 6.0 percent/volt over the tuning range, averaging 5.7 percent/volt. The total tuning

range would be .057 x 20 = 1.14 times the zero-volt frequency, or a frequency ratio of 2.14:1 (more than one octave).

The above example shows why we recommend the use of frequency-linear diodes as chips, not packaged, unless the junction capacitance is high enough to tolerate the typical 0.2 pF package capacitance in parallel with the junction.
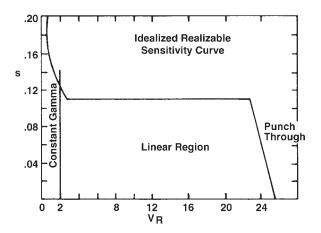

IDEAL VS REALIZEABLE C-V CURVES

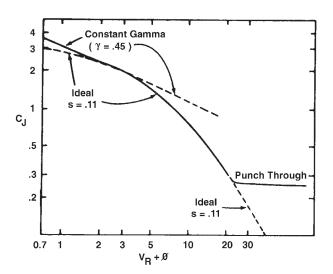As shown above, the ideal tuning curve of a FLTVAR follows the equation

$$C_{j(V)} = \frac{C_{j0}}{(1+sV)^2}$$

which provides constant sensitivity(s) at all reverse voltages. In practice it is necessary to deviate from this ideal both at low voltages (0-2 volts) and at high voltages.

In order to provide as high Q as possible, it is necessary to restrict the thickness of the epitaxial region, which places an upper limit on the width of the depletion layer inside the semiconductor. As a result, the capacitance will stop changing as a function of voltage above a certain voltage, called the punchthrough voltage. This defines the upper limit on the tuning range. Therefore, there is a trade off between high Q and high tuning range for a given value of s. In other words, for highest Q, the varactor should be designed to have a punchthrough voltage that is equal to the highest voltage available (tuning voltage + RF signal voltage) from the circuit.

At the low voltage end, a different limitation occurs. The ideal C-V curve results in a dopant density curve which is infinite at the junction, which is impossible, as it implies an infinite electric field at the junction. In practice, the diode designer must limit the maximum density to a finite value near the junction, which has the effect of "splicing" a constant-gamma C-V curve to the frequency linear curve below a certain voltage (typically 0-2 volts). Otherwise, the diodes would have very low breakdown voltages!
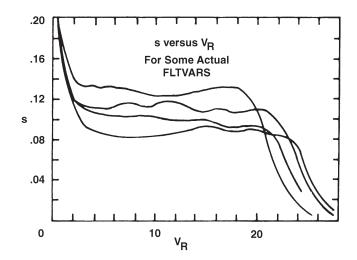

Because of these factors, the constant-sensitivity portion of the C-V curve is limited to a voltage range like 2-20 volts or 2-25 volts. The value of s becomes large below 2 volts, and very small above punchthrough. Within the linear tuning range (2-20 volts) the sensitivity (s) is typically constant within ±5% of its average value.

s versus V_R
For Some Actual FLTVARS

Epi-Layer Q vs Tuning Ratio

TRADEOFFS

As mentioned before, punchthrough of the capacitance curve is introduced to improve the Q of the diode by decreasing the series resistance Rs. In fact, the Q of a silicon FLTVAR at high reverse bias (in punchthrough) can approach 100,000 at 50 MHz for unpackaged chips. (The Q at higher frequencies will be decreased by the ratio 50/f for frequency in MHz). Unlike abrupt junction varactors, the series resistance is nearly independent of voltage over most of the tuning range, which makes it easy to calculate the Q at voltages other than the specification voltage (4 volts). As for all tuning varactors, the Rs is nearly independent of frequency. The following formulas can be used to approximate the Rs, and the Q at all frequencies and voltages; using the specified Q-4 from the data sheet:

$$Q(f) = \left(\frac{50}{f}\right) Q - 4 \quad \text{(f in MHz)}$$
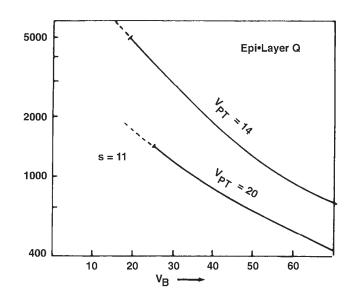
$$Q(v) = \frac{C_j - 4}{C_j(v)} \; Q - 4$$

$$R_s = \frac{3183}{Q - 4 \; C_j - 4}$$

In specifying a frequency linear varactor, the tradeoff between tuning ratio and Q should be noted. By tuning ratio (TR) we mean the ratio of the highest junction capacitance, at zero volts, to the lowest function capacitance. (In a circuit without capacitive parasitics, the frequency ratio, fmax/fmin, is just √TR). The Q for a theoretically optimum Frequency Linear tuning diode falls drastically as the tuning ratio is increased.

Therefore if high Q is desired, it is important to reduce both series and parallel parasitic capacitances as much as possible so you can use a varactor with minimum possible TR and gain the advantage of highest possible Q.
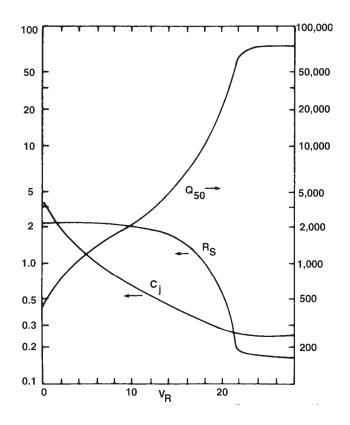
It is also important not to specify a higher breakdown voltage than needed (5 volts above punch-through is usually sufficient). There is a trade-off between Vb and Q, because the sensitivity and thickness of the epitaxial layer must both be increased to get higher breakdown voltage, and this increases the series resistance for a given capacitance.

Epi•Layer Q

LARGE SIGNAL EFFECTS

When using frequency linear tuning varactors in VCO's and other large signal applications, several large-signal effects can occur which can either degrade or improve linearity. First, these diodes, like all silicon varactors, rectify slightly if the RF signal swing results in the diode being forward biased for part of a cycle. As a result, the diode starts to draw current which flows through the DC bias resistor and the effective source impedance of the bias circuit, resulting in additional reverse bias. The amount of additional reverse bias increases as the intended reverse bias moves closer to zero volts, resulting in a decrease of sensitivity(s) because the rate of change of the actual reverse bias is less than the rate of change of the intended bias. If the DC bias resistor is chosen properly (it's value depends on the signal level) the decrease of s near zero volts can almost exactly compensate for the rapidly changing high s encountered in the constant gamma region (0-2 volts) of typical FLTVARs. The result is a voltage tuned oscillator which tunes linearly right to zero volts, and often a volt or two into what would normally be considered forward bias (but the diode is really reverse biased by rectification).

At the high voltage end of the tuning range, high signal level causes a gradual reduction of sensitivity as the voltage approaches punchthrough. The reason is that the signal voltage reaches into the low-s region beyond punchthrough, thereby reducing the average s over a cycle. This effect increases gradually as bias voltage increases, resulting in a gradual rolloff of sensitivity similar to the effect of parallel capacitance. Although the effect on linearity can be compensated by adding series capacitive reactance, this reduces overall sensitivity, so it is usually best to specify a device whose punchthrough voltage exceeds the sum of the highest bias voltage plus the highest signal swing. This allows the highest possible overall sensitivity for the circuit, although with some compromise of diode Q, since there is a tradeoff between diode Q and punchthrough voltage.

The third large signal effect that may be of some concern is harmonic generation. Since the frequency-linear diode is an active device, large signal levels will be accompanied by harmonics generated by the nonlinear capacitance. Since the nonlinearity of the capacitance is larger at high bias voltages than in the more familiar diodes, larger harmonic generation can be expected. In typical VCO's covering less than one octave, this may not be detrimental but in wider band designs it may be an important consideration. In this case, the designer should consider push-push oscillator design, or consider using two tuning varactors in series (mounted-to-back). Both approaches tend to reduce harmonics, making them useful for multi-octave designs.

The linearity of the tuning circuit can also be affected by signal and frequency dependent effects in other nonlinear devices. For example, if a bipolar transistor is used as the active device in a VCO the input capacitance is dependent both on signal voltage and frequency. Suppose the transistor is to be used as a common-collector oscillator, with the tuning inductor and tuning diode connected in series with the base, and a feedback reactance in series with the emitter. The transistor presents a series capacitance (and negative resistance) to the tuning diode. To determine the magnitude of Cs it is necessary to obtain the S11 of the transistor (with feedback in place). Then use the formula

$$X_s = 1/2\left(X_{11} - f\frac{dX_{11}}{df}\right)$$

to obtain the reactance of Cs as a function of frequency. From this, the effect of Cs on sensitivity can be determined (the value of the series inductance has no effect on sensitivity).