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LX1673 PR0DUCT DESIGN GUIDE

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Rev. 0.2, 2002-09-12

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1.0 INTRODUCTION

This document is intended to be used with the LX1673 data sheet as a guide to designing buck regulators with the LX1673 controller. Information is presented on operation of the complete circuit and selection of critical components that should allow the design of a complete regulator.

2.0 THEORY OF OPERATION

Buck regulators are used in a variety of applications where the input must be stepped down to a lower output voltage. The increasing power demands of microprocessors and their support chips require power levels that would be impractical with linear regulators. The demand for better efficiency is another driving factor in the use of switching regulators.

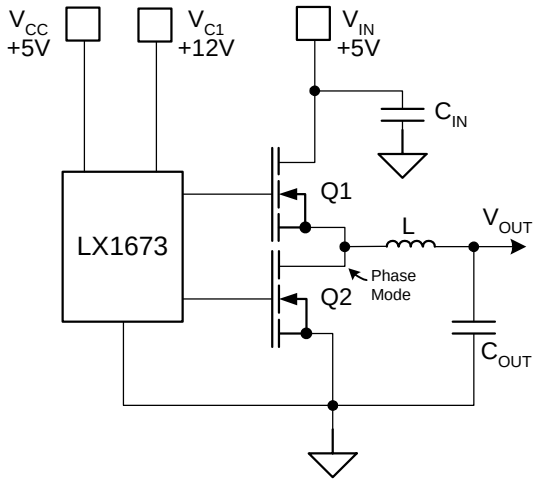

Figure (1) - Synchronous Buck Regulator

The inductor is used as an energy storage device and acts as a current source. When the main FET (Q1) is turned on, current from the input flows through the inductor and into the load. When the output voltage reaches the control point, the main FET (Q1) will be turned off and the sync FET (Q2) will be driven on. There is a short non-overlap period at all switching transitions to insure that there can be no instance where both FETs are on at the same time.

Both FETs are constantly switching at the PWM frequency to maintain regulation.

The control loop consists of an error amplifier with the non-inverting input connected to a reference voltage and the inverting input connected to the output voltage through a resistor network that determines the output voltage.

The error amplifier output is used to drive a comparator with a voltage ramp on its other input. The error amplifier output will move up and down on the ramp voltage causing the comparator to generate a timing signal that determines the PWM duty cycle. See Figure (2)

Since the inductor current cannot change instantly when the main FET switches off the body diode in the sync FET will conduct and current will flow up from ground to maintain the inductor current at its previous value. Inductor current ramps up at a linear rate when Q1 is on and down at a linear rate when Q2 is on because in both cases there is constant voltage forcing function.

When the body diode is conducting there will be a negative voltage on the drain of Q2 due to the direction of current flow and the body diode drop. The voltage drop across the source to drain will be much less than across the diode. Hence, when Q2 turns on the phase node voltage (Q1 source - Q2 drain) will be approximately equal to ground.

When Q1 turns on, the body diode of Q2 is still conducting so current must be commutated from the diode to the upper FET. Due to slow recovery time and stored charge in the Q2 body diode a current spike will be present on the leading edge of Q1 drain current. This condition can be greatly helped by putting a Schottky diode in parallel with the synchronous FET.

Figure (3) shows some waveforms at key nodes. High frequency details have been omitted for ease of understanding.

The inductor also works with the output capacitor to form a low pass filter that filters the voltage pulses present on the phase node and results in a clean DC output. The voltage on the top of the output capacitor is a saw-tooth that is centered on the output voltage and has an amplitude equal to the inductor ripple current times the capacitor ESR.

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APPLICATION INFORMATION (CONTINUED)

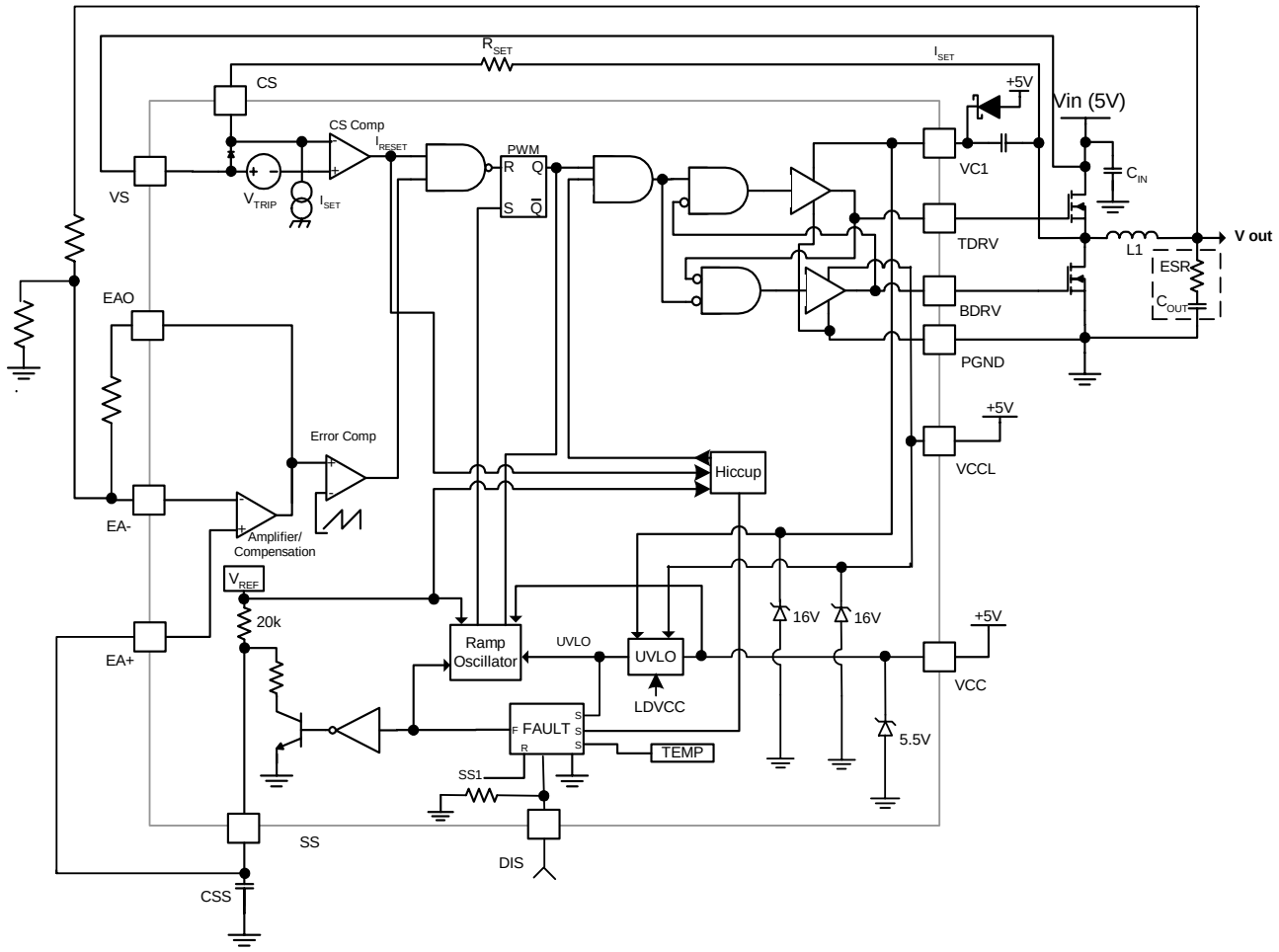

Figure (2) – PWM Block Diagram

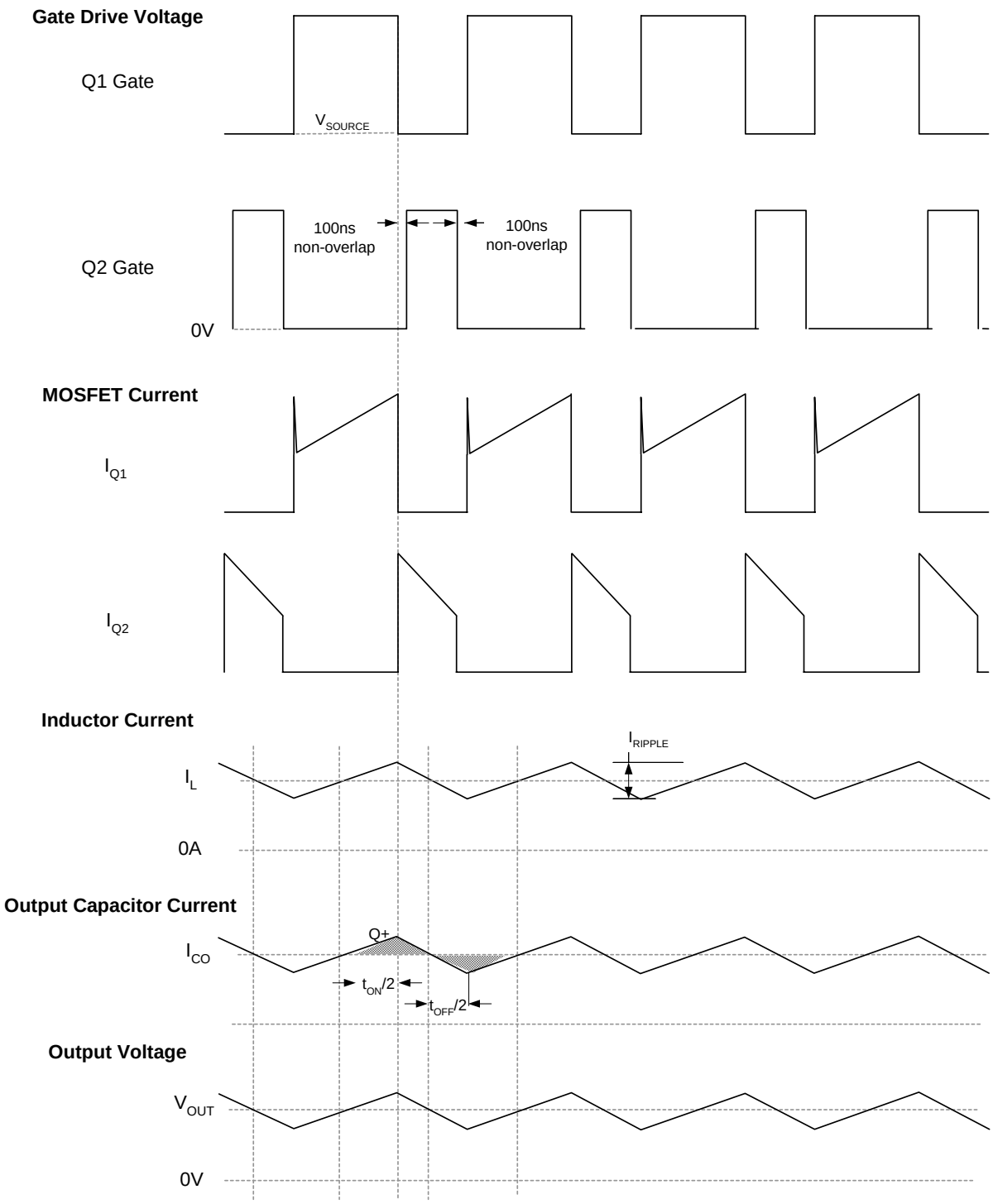

Figure (3) - Buck Regulator Waveforms

3.0 BOOTSTRAP

The bootstrap circuit will add approximately 5 volts to the PWM input (high side FET drain) to provide sufficient voltage to enhance the high side FET. See Figure (4a)

The bootstrap circuit consists of a capacitor (C) that charges to 5 volts through the bootstrap diode (D) when the lower FET (Q2) turns on. When the upper FET (Q1) turns on, the five volt charge on the capacitor is coupled to the VCX pin and added to the FET source voltage. This back biases the diode to allow the VCX pin to float up to Q1 source potential plus 5 volts. The diode must have a low stored charge to prevent partial discharge of the capacitor, Schottky diodes are quite often used for this reason. The capacitor must store enough charge over a PWM cycle to keep the driver supply voltage from drooping. For most applications a .1 uf capacitor is sufficient. As long as the bootstrap capacitor is substantially larger than the FET input capacitance it will store enough charge for proper operation. A value that is 50 to 100 times the FET gate capacitance (Ciss) will be adequate.

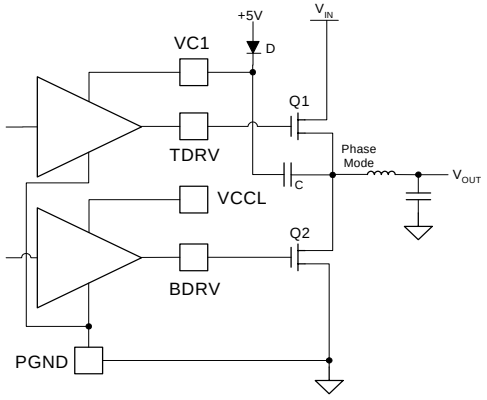

Figure (4a) - Bootstrap Circuit

When using this bootstrap configuration the voltage on the VC1 pin is a square wave between the PWM input voltage and +5 volts.

When using the bootstrap or rectifier / filter the voltage on the VC1 pin must not reach a level where excessive current will flow into the internal zener diode.

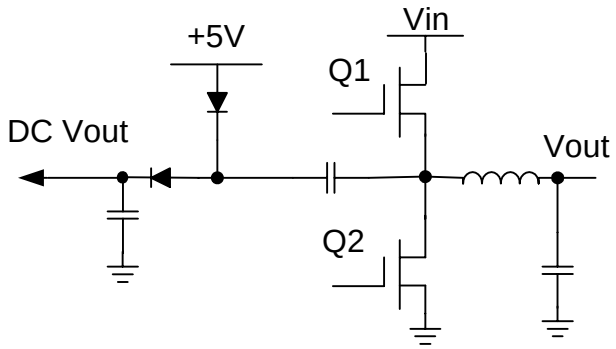

Figure (4b) - Bootstrap with Rectifier / Filter

4.0 SOFT START , ENABLE

PWM has a soft start pin SS that is used to connect an external soft start capacitor Css. Css is charged by an internal 20KΩ resistor (Rss) connected to the reference voltage. The SS pin also provides an enable function, holding the SS pin low disables the corresponding phase.

The LDO has an enable pin LDDIS that disables the LDO output when it is held high.

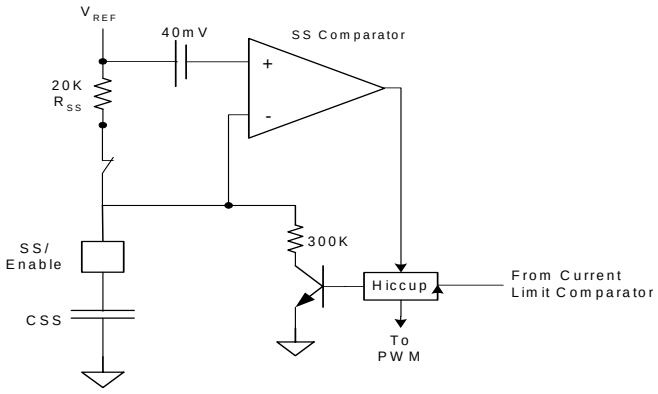

Figure (5) - Simplified Soft Start

At power on the under voltage lockout conditions, see data sheet for values, for VCC, VCCL and VC must be met before Css will begin to charge. The output voltage will then increase from zero volts towards Vout and track the Css voltage until the soft start circuit is switched out after three time constants of Rss-Css. The three time constants allow Vout to be within 95% of the correct value at the termination of soft start, an internal comparator monitors the soft start pin and terminates the soft start cycle.

During the soft start ramp period the Over Current Protection is functional but the hiccup function is disabled till the soft start interval is complete.

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When the soft start interval begins the PWM is disabled. No PWM pulses will be generated until the ramp has reached a 300mV level where a comparator enables the PWM. This will result in a current spike into the output capacitor that may result in a series of over current commands for a few cycles until the output capacitor has charged up to the same level as the soft start ramp.

5.0 OVER CURRENT PROTECTION AND HICCUP

The external resistor R_{SET} along with Q1 $R_{DS(ON)}$ will determine the current limit set point. See Figure (6), the voltage drop across Q1 $R_{DS(ON)}$ plus the drop developed across R_{SET} by the internal 50uA current source must exceed the internal 300 mv threshold to initiate a current limit. There is a 350nSec delay in the current limit comparator to prevent false triggering due to ringing and noise. Note that the $R_{DS(ON)}$ of any FET has a positive temperature coefficient, be sure to use the value corresponding to the expected operating temperature, usually at least 100 ° C, at the FET die. Once the upper FET $R_{DS(ON)}$ is known the value of R_{SET} can be calculated.

$$R_{SET} = \frac{300\,mV - \left(I_{CL} \times R_{DS(ON)}\right)}{50\,\mu A}$$

Where I_{CL} is the current limit threshold.

Note: The minimum value for R_{SET} is 1KΩ to prevent damage to the LX1673 input, the maximum value is 6KΩ where I_{CL} equals zero (50uA x 6KΩ = 300mV).

At low duty cycles where the upper gate drive is less than 350nS wide the 350nS delay for current limit enable may result in current pulses exceeding the desired current limit set point. If the upper MOSFET on time is less than 350nS and a short circuit condition occurs, the duty cycle will increase since Vout will be low. The current limit circuit will be enabled when the upper gate drive exceeds 350nS. The actual peak current limit value will be higher than calculated with the above equation.

Short circuit protection still exists due to the narrow pulse width even though the magnitude of the current pulses will be higher than the calculated value.

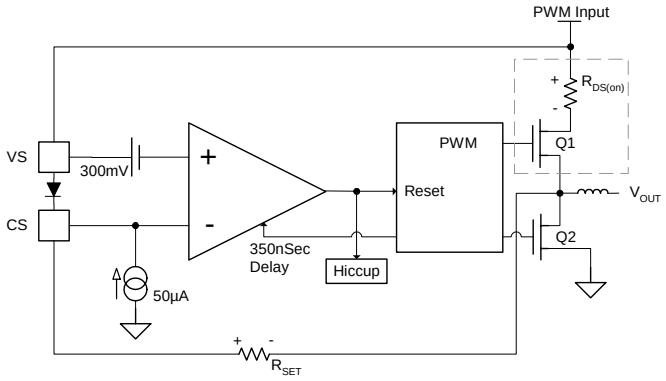

Figure (6) - Over Current Protection

The R_{SET} resistor and VC pin should be as close to a Kelvin connection to the FET source and drain terminals as possible. Very low $R_{DS(ON)}$ values will result is significant errors otherwise.

The Over Current Protection is functional during the soft start ramp period. If currents in access of I_{CL} are detected the PWM will be commanded off for the remainder of that cycle but will restart on the next PWM cycle.

If no current limit is wanted the R_{SET} resistor can be left out and the CS and VS pins connected together and tied to VCC. A floating VS pin will result in operation resembling a hiccup condition.

The hiccup function is disabled during the soft start ramp period. Once the soft start ramp has been terminated the hiccup function will be enabled. If an over current command is issued after the termination of soft start the soft start capacitor will be pulled low by the 300KΩ resistor, Figure 5, the switch in series with RSS will open during this time to allow discharging CSS. The voltage on CSS will drop till it reaches a lower limit of 200mV when a comparator will begin the soft start interval again.

The hiccup process will continue indefinitely if the load is greater than the current limit threshold determined by R_{SET}.

6.0 COMPONENT SELECTION

Component selection in a DC to DC converter requires a lot of consideration and tradeoffs since there are a number of conflicting requirements such as size, cost, and performance. The components that are the most critical and require the most effort are the switching FETs , inductor , and input / output capacitors. The output filter is generally designed with output ripple and load transients as the main consideration but it has a very important role in loop compensation that should be considered.

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The LX1673 is a voltage-mode controller intended for use in the continuous mode (i.e., inductor current never reaches zero). All equations presented in this document are based on these conditions.

7.0 FET SELECTION

Because the PWM FETs are the primary active power handling components they must be carefully chosen and properly sized for the power that will be dissipated. In many cases the main and synchronous FETs can be the same part number but as switching frequencies and currents become higher it is often desirable to use different devices that are optimized for each circuit application. The upper FET is commonly called the main switch and the lower FET is typically referred to as the synchronous switch since it is used as a synchronous rectifier.

Eq (1) Main FET Duty cycle

$$D = \frac{V_{OUT}}{V_{IN}}$$

Eq (2) Sync FET Duty Cycle

$$= \frac{V_{IN} - V_{OUT}}{V_{IN}} = 1 - \frac{V_{OUT}}{V_{IN}} = 1 - D$$

In a buck regulator topology there are no high transients that require a drain to source voltage much in access of the PWM input voltage. On resistance, maximum drain current, and thermal performance are closely related and must be considered together. Thermal management is a key element in a buck regulator design and requires careful component selection and board layout. The gate threshold voltage must be low enough to guaranty that the FET will be fully enhanced with the available gate drive voltage. Gate charge, Qg, should be less that 40nC.

8.0 UPPER FET POWER DISSIPATION

The power dissipation in the upper FET, Q1 is the sum of the switching loss and conduction or I^2 R loss. As a close approximation it can be assumed that the current through the upper FET is a linear ramp during the switching interval.

Eq (3)

$$P_{Q1} = \left[\left(\frac{I_D}{2}\right) \times V_{IN} \times \left(t_r + t_f\right) \times f\right] + \left[I_D{}^2 \times R_{DS(on)} \times D\right]$$

Where I_D is the FET drain current, tr and tf are the rise and fall times, f is the PWM switching frequency, and D is the duty cycle. For some typical numbers we will pick:

- Vin = 5 V
- Vout = 1.5 V
- Iout = 5 A

This gives a duty cycle of (1.5V)/(5VA) = 0.3 or 30%. Using the Si4842DY with the circuit values given above, the switching loss in the main FET is [(5/2)(5)(80nS + 80nS)(300KHz) = 0.60W. Note: These turn on and off times are approximate in-circuit values. Using RDS(ON) at 100 ° C the conduction loss is ($5A^2$)(0.0084Ω)(0.3) = 0.063W.

Total main FET power dissipation equals (0.60+0.063) = 0.663W.

9.0 LOWER FET POWER DISSIPATION

The lower FET has no significant switching loss due to the parallel diode. All power dissipation is from the I^2R loss during conduction; the formula for power dissipation reduces to:

Eq (4) $$P_{Q2} = \left[I_D{}^2 \times R_{DS(on)} \times (1 - D)\right]$$

With the previous operating conditions, the conduction loss equals ($5A^2$ x .0084Ω) x (1-0.3) = 0.147W. The sync FET body diode will start to conduct immediately after the main FET turns off and before the synchronous FET turns on. Hence, there is always a short non-overlap period to prevent simultaneous conduction of both FETs. The body diode causes the sync FET to transition with a low drain to source voltage while the main FET transitions with a drain to source voltage of approximately Vin. When the synchronous FET turns off, the body diode will conduct for a short period of time before the main FET turns on. Due to this it is assumed that the switching losses in the synchronous FET are negligible. There is some power dissipation in the body diode but the conduction time is so short that these losses are also very low. The body diode in most FETs is a very non-ideal diode with a long recovery time and high stored charge.

10.0 GENERAL FET CONSIDERATIONS

In the above example the I^2R losses in the main FET are less than one half that of the synchronous FET (i.e., the switching losses are dominate). Note that the temperature, drain current, and gate-to-source voltage all have an effect upon the $R_{DS(ON)}$ value and should be taken into account. A common practice is to pick a main FET that is optimized for switching losses and a sync FET that has low $R_{DS(ON)}$ to minimize conduction losses. As currents get higher it is possible to parallel several FETs to get a lower effective $R_{DS(ON)}$ and

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spread the heat over a larger area to get better heat sinking from the circuit board.

The reverse transfer capacitance, Crss, is another critical parameter that effects FET switching by requiring more gate drive. Also when the upper FET turns on it will attempt to pull the lower gate high through Crss of the lower FET. If this effect is to great the lower FET can turn back on causing cross conduction.

11.0 FET GATE DRIVE

Any FET used in a switching application should have a low total gate charge to minimize the peak current required to charge and discharge the gate capacitance each cycle. If the gate charge is too high it places a greater demand on the driver causing possible thermal problems and slow switching. Increasing FET transition times further degrades the circuit's switching losses. The FET drivers in the LX1673 must charge and discharge the input capacitance of the external FET switches on every PWM cycle. Due to the very fast switching times needed for efficiency, the peak current required to charge the gate is significant. Charging a 2500pf gate capacitor to 5 volts in 50ns requires an average current of 0.25A. This current flows through the controller output transistors and results in internal power dissipation. It is common to use total gate charge rather that gate capacitance to calculate drive power. As a guideline 40nC should be considered the maximum FET input charge to be driven. The input capacitance of a FET is not a simple capacitor but rather a combination of several internal capacitors that change value with operating conditions. FET data sheets show a total gate charge Qg that accounts for this complexity and can be used to calculate the power required to drive the gate.

The charge on a capacitor is:

Eq (5) $$Q = CV$$

The power required to charge a capacitor is:

Eq (6) $$P = CV^2 f$$

By substituting terms the power required to drive the FET gate is:

Eq (7) $$P = QgV f$$

Where Qg is the total gate capacitance from the FET data sheet, V is gate drive voltage, and f is the PWM frequency.

The LX1673 evaluation board is often delivered from the factory with the lower gate driver powered by 5 volts on the VCCL pin. The upper gate driver (VC1) is connected to 12 volts. Using these numbers we can calculate the power required to drive the FETs with a 300KHz LX1673.

Assuming a gate charge of 40nC we have:

- Lower gate driver = 40nC x 5V x 300KHz = 60mW.
- Upper driver = 40nC x 12V x 300KHz = 144mW.
- The total gate drive power is 60+144 = 204mW.

With Vcc at 5 volts and an Icc of 15ma there is an additional 75mW of package dissipation that must be added to the 204mW for gate drive. This equals 279 mW total for the LX1673 MLP package. The data sheet specifies the MP package junction-to-ambient (θja) thermal resistance at 35°C per watt. This value assumes that the MLP package is mounted to a circuit board. The junction temperature can be calculated from:

Eq (8) $$T_J = T_A + (P_D \times \theta_{JA})$$

Assuming an ambient temperature of 23°C we get a junction temperature of:

$$T_J = 23 + (.204 \times 35) = 30°C$$

The 150°C maximum operating junction temperature allows a maximum rise of:

$$150 - 30 = 120°C .$$

The LX1673 can be operated with up to 16 volts DC on the VCCL pin but that would be inadvisable from a power dissipation perspective.

12.0 FET THERMAL CONSIDERATIONS

Since it is always desirable to avoid the use of heat sinks (other than the circuit board itself) careful consideration should be given to component selection and layout from a thermal point of view. FET package selection is a significant part of the overall thermal picture and has a significant effect on thermal performance. For example, large cases like the D^2 package have a much lower junction to circuit board thermal resistance than the popular S08.

Another popular surface mount package is the D pack slightly smaller than the D^2 and has a corresponding lower current handling capability. The tried and true TO220 is always worth looking at if the mounting tab is acceptable, it is a low cost package with good performance. The TO220 is quite often used with no heat sink on the tab but the thermal resistance to air is fairly high so this requires careful consideration. For

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surface mount components the maximum allowable thermal resistance from the circuit board to air $R\theta_{(CB-A)}$ can be calculated by.

$$R\theta_{(CB-A)} \le \frac{(T_J max - T_A max)}{P_D max} - R\theta_{(J-C)}$$

Eq (9)

This formula assumes that the FET case and the circuit board are at the exact same temperature which is valid only for surface mount components. Once the power dissipation of each FET has been determined and a maximum operating junction temperature chosen the required thermal resistance of the circuit board to air can be calculated.

If we look at the example where an Si4842DY FET dissipates 1 watt at a maximum ambient of 85 ° C, and allow the junction temperature to reach the maximum data sheet spec of 150 ° C, θj-c of the Si8442DY is 16° C per watt.

$$R\theta_{(CB-A)} \le \frac{(150-85)}{1} - 16 = 49^\circ C/W$$

The circuit board to air thermal resistance $R\theta_{(CB-A)}$ must be less than 49 degrees C per watt. The thermal resistance to air of a 1 in^2 circuit board, with properly designed copper power and ground planes to help spread the heat, will typically be 45°C per watt. Keep in mind that adjacent heat generating components will add to the thermal load on the circuit board and require more area. Small clip-on heat sinks and airflow will help reduce component heat dissipation considerably.

13.0 INDUCTOR SELECTION

The inductor is usually one of the largest components in a buck regulator and has a large influence on performance. There are two loss mechanisms copper loss and core loss both of which must be considered in order to maximize circuit efficiency. Since it is often desirable to use off the shelf components some compromises are usually made with the inductor. Selecting an inductor with a low series resistance is always desirable. Further, make sure that the core material will perform properly at the PWM switching frequency.

The core must be able to handle the maximum output current plus one half of the ripple current without a significant drop in inductance. If the core is allowed to saturate, the inductance will drop dramatically and result in a significant increase in ripple current.

A lower inductance value will provide better transient response and a smaller package at the expense of increasing the ripple current. As the inductance value increases, transient response degrades and component size increases; however, the ripple current decreases. Ripple current is an important factor since it must flow into the output filter capacitor and will result in an output ripple voltage that is the product of the capacitor ESR and the inductor ripple current. Inductor ripple current is usually set to be within 10% to 40% of the output current and typical inductance values range from 1 to 10uH. The output inductor and capacitor play a critical role in determining overall regulator performance. Hence, it may be necessary to do an iterative design if the first inductor choice results in an unacceptable capacitor value. The relationship for voltage across an inductor takes the well recognized form of:

$$V = L\frac{di}{dt}$$

Eq (10)

In a buck regulator the forcing function is always a constant voltage source resulting in a linear ramp of current so we can use the ΔI and ΔT terms rather than be concerned with integrating a nonlinear function. The rate of change, or slew rate, that can be achieved for an inductor is then

$$\Delta I = \frac{V\Delta t}{L}$$

Eq (11)

Substituting terms used in a buck PWM regulator

$$\Delta I = \frac{V_{IN} - V_{OUT}}{L} \times \frac{D}{f s}$$

Eq (12)

and rearranging terms to calculate inductance

$$L = \frac{V_{IN} - V_{OUT}}{\Delta I} \times \frac{D}{f s}$$

Eq (13)

Where fs is the PWM switching frequency , L is the inductance and D is the Duty Cycle.

To examine the inductor slew rate for a step change in output current

$$Trise = L \bullet \frac{CurrentStep}{Vin - Vout}$$

Eq(14a)

$$Tfall = L \bullet \frac{CurrentStep}{Vout}$$

Eq(14b)

Equations 14 a and b are useful because they give us the maximum slew rate that can be achieved for a given inductor.

An important point on slew rate is that the above number does not represent loop response. The final

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rate of change of the output voltage in response to a step change in current is determined by the frequency response of the closed loop and the loop phase margin. The control loop will always respond slower than the inductor current ramp.

The following example calculations use the conditions listed below:

Vin = 5 V

Vout = 1.5 V

D = 1.5/5 = 30%

I out = 8 A

Inductor ripple current = 20%

PWM frequency = 300 KHz

Maximum load step = 4A

Output ripple < 50mV

Total output change due to 4 A step < 100 mV

Using equation 13, the inductance value is determined as follows:

$$L = \frac{5 - 1.5}{8 \times .2} \times \frac{D}{f\,s} = 2.18\,\mu H$$

14.0 OUTPUT CAPACITOR SELECTION

Once the inductor value has been determined an output capacitor can be chosen. The ESR value is the main selection criteria for this capacitor. Package size at the required voltage and capacitance will also need to be determined after the ESR is known. The output ripple voltage and allowable error for a step change are important since both of these influence the required ESR of the capacitor.

If no load step is specified

$$\text{Capacitor ESR} \le \frac{\text{Output Ripple Voltage}}{\text{Inductor Ripple Current}}$$

Eq (15)

For the 50mV ripple voltage:

$$\text{ESR} \le \frac{50\,\text{mV}}{1.6\,\text{A}} \le .031\,\Omega$$

This will not be a difficult ESR to achieve with good quality capacitors. A 4A load step will give a drop in the output of .031Ω x 4A =125mV which is greater than the total 100mV allowed so we will need a lower ESR due to the current step and output ripple combined.

When a step change in load current is known:

Eq (16)

$$\text{Capacitor ESR} \le \frac{\text{Total Allowable Voltage Drop}}{\text{Inductor Ripple Current} + \text{Load Step}}$$

The total allowable drop will be the amount allocated to the load step minus one half of the ripple voltage.

$$\text{Capacitor ESR} \le \frac{100\,\text{mV} - 25\,\text{mV}}{1.6\,\text{A} + 4\,\text{A}} = .0134\,\Omega$$

This ESR value is easily achieved. It is almost always true that once the ESR requirement is met the bulk capacitance will be adequate for energy storage. Some common capacitor types are the Sanyo MV-GX, and Sanyo OS-CON. Others like the surface mount Panasonic SP-CAP also have low ESR. It is common practice to parallel a number of capacitors to get the required ESR while maintaining acceptable package size. Do not overlook the reliability of the capacitor at the required temperature, operating voltage, and ripple current.

15.0 INPUT CAPACITOR SELECTION

The main criteria for selecting the input capacitor is ripple current. When the PWM main FET switches on it places a high current demand on the input rail. The energy must be supplied by the input capacitor because the input path typically has sufficient impedance such that it cannot supply the peak demand made by the PWM. For a single phase PWM the worst case input current condition occurs when the duty cycle is at 50% resulting in an RMS current of Iout/2.

The actual RMS input current for a single phase PWM is given by

$$I_{IN}(RMS) = I_{OUT}\sqrt{D(1-D)}$$

Eq(17)

For a single phase Buck PWM and the 8A output in our previous example the actual input ripple current from Eq 17 would be 3.67A RMS. Since the input voltage is always higher than the output this puts an additional burden on the input capacitor.

Several capacitors connected in-parallel will be required to meet the 3.67A RMS ripple current and voltage constraint. For example, the Sanyo MVGX series 10 volt 1500uF capacitor has a ripple current of 1.3Arms. This would require 3 devices in-parallel to meet the 3.67A RMS input ripple requirement.

A plot of Equation 17 will show that considerable deviation from a 50% duty cycle is required to gain any significant reduction in RMS input current from the worst case of .5 x Iout. If the input voltage is not well

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controlled be careful to use the maximum input voltage when sizing the input capacitor.

As with the output capacitor the bulk capacitance will be more than adequate once the main criteria of ripple current has been met. ESR should also be considered because it results in an overall loss of efficiency, the power loss in the capacitor is equal to (I2 x ESR). This loss should not be ignored if maximum efficiency is a goal. The ripple current in the capacitor will also cause component heating, adversely effecting reliability.

Always consider temperature and voltage stress at the worst case conditions when picking a capacitor.

16.0 EFFICIENCY

The key components that significantly effect overall efficiency are the power handling components in the PWM output stage. The switching FETs have the greatest effect on overall efficiency. In order to maximize efficiency, the selected FETs must have the lowest possible switching and conduction losses. These factors are covered in the Component Selection section. FET gate drive can require significant power, always pick FETs with low gate charge and use the lowest practical gate drive voltage. PWM frequency is a significant factor in overall design. At higher PWM frequencies the switching losses become greater. However, at higher PWM frequencies, other components become smaller.

A trend in FET development is to improve switching and conduction losses hence, better components continually become available. The Inductor can dissipate a significant amount of power if the I^2R losses are too high or if the inductor core has a lot of loss at the PWM frequency. Always pick an inductor with low ESR and be certain that it will operate efficiently at the maximum PWM frequency. If the core begins to saturate the core loss and ripple current will increase. Be certain that the inductor is rated for the full output current plus one half of the ripple current. Remember that the ESR of input and output capacitors dissipate power and should be taken into account.

Even with good power planes and wide traces drop across the circuit board copper can be significant.

The MOSFET upper driver supply voltage (VCX) should be kept as low as possible for best efficiency.

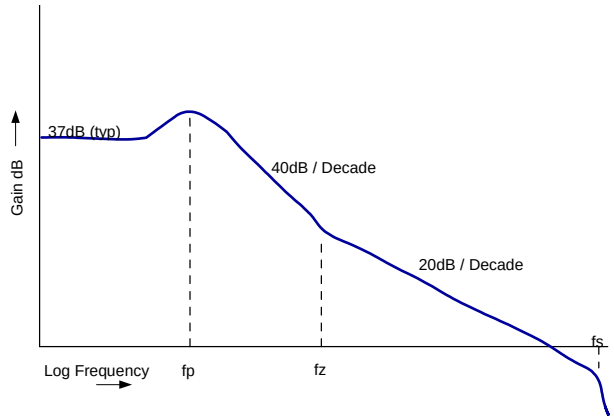
17.0 LOOP COMPENSATION

A complete mathematical analysis of a buck PWM is possible however, due to the number of component tolerances and variations in input voltage a simple graphical method using a Bode plot will generally give satisfactory results.

A buck regulator using the LX1673 controller is quite forgiving and generally does not require any additional compensation components to implement a stable system with sufficient phase margin. The evaluation board component values result in a stable system with superior transient response. One version of the factory delivered eval board has phase 1 and 2 operating in Bi-Phase, the feedback for the phase 1 error amplifier is a resistor that sets a fixed gain. The phase 2 error amplifier has a capacitor in the feedback path to form an integrator that gives a very high gain at low frequencies so that it can track phase 1. This is one example of how the feedback components can be used.

The output inductor and capacitor are the primary components that determine the frequency response of the closed loop by creating a double pole and a zero that set the dominant break points and determine the unity gain crossover point (unless frequency compensation components are added). Loop gain is another variable used to determine the unity gain crossover frequency and overall loop stability.

A common design goal is to have the unity gain crossing occur at a slope of -20dB per decade. It is possible to cross through zero gain at -40 dB per decade if the ESR zero is close enough to the zero crossing to provide sufficient phase margin. The unity gain crossing should be below the switching frequency pole by a factor of 5 if possible. Once the break points have been calculated a Bode plot can be drawn on semi log paper to obtain a graphical representation of the loop response. A typical Bode plot for a PWM regulator using the LX1673 is shown in Figure (7)



fp: is the double pole set by L & C
fz: is a zero set by the capacitor ESR
fs: is a double pole at the switching frequency

Figure (7) - PWM Bode Plot

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A double pole at a break point frequency (fp) is determined by the output inductor and capacitor:

$$f(\mathrm{p}) = \frac{1}{2\pi\sqrt{LC}}$$

Eq (18)

A zero is set by the output capacitor at the frequency (fz):

$$f(\mathrm{z}) = \frac{1}{(2\pi)\mathrm{ESR}\times C_{OUT}}$$

Eq (19)

Figure (8) shows the blocks in the control loop that effect frequency response and gain. The error amplifier is the primary gain block and can be treated like any operational amplifier. The PWM and FET switches are considered one stage. The amplifier gain is simply the feedback impedance between the EA- and EAO pins divided by the input impedance. The resistors connecting the PWM output to the amplifier input at the EA- pin (ZIN) must be considered as a Thevinin equivalent to calculate the correct gain.

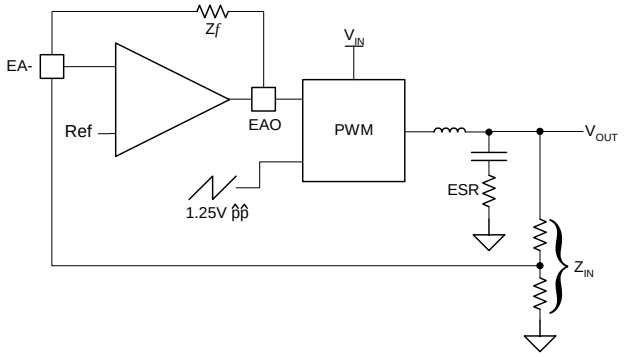

Figure (8) - LX1673 Control Loop Block Diagram

$$\text{Amplifier Gain} = \frac{Z\,f}{Z_{IN}}$$

Eq (20)

The gain of the PWM stage is:

$$\text{PWM Gain} = \frac{\text{PWM Vin}}{\text{RampVoltage}}$$

Eq (21)

Loop gain is the product of the amplifier and PWM gains calculated with equations 20 and 21. Note that these equations give a unitless numerical gain (A). The gain in db is 20log(A), gain in db is added for cascaded stages.

A very import point is that the input voltage is a gain term in the loop transfer function so that varying the voltage on the main FET drain will have an effect on loop gain and stability. The difference in gain going from 3.3 to 12 volts input is 20log12/3.3 = 11.2db, a considerable change in loop gain.

18.0 TRANSIENT RESPONSE

A useful check of performance is to apply a step change of current to the output using a FET switch with a series load resistor and observe the response of the output voltage and inductor current. A large overshoot that takes a number of cycles to settle indicates low phase margin. A system with greater phase margin will have less overshoot but take longer to correct the error introduced into the feedback loop.

19.0 CIRCUIT BOARD LAYOUT

Switching regulators operating at multiple amps of output current are very sensitive to layout due to the high current pulses and fast rise times when the FETs are switched. It is important to keep the currents in the FET switching and filtering section confined to their own ground plane and use a single point ground connection to the analog and digital ground pins on the LX1673.

The connection between the lower FET drain and upper FET source should be as short as possible and properly sized for current. Inductance in this path will result in unwanted transients that will impair proper switching operation. The input and output capacitor ground leads should be returned to the source of the lower FET. The PGND pin should be connected at the lower FET source. Large traces are required in all output filter connections. A good layout keeps all circulating currents produced by the output switching and filter sections away from the low signal level analog circuitry. Feedback lines going to the LX1673 for voltage and current should be routed on a lower layer protected from the output section by a ground or power plane. Separate bypass capacitors should be used on the VCC and VCCL pins to prevent possible UVLO problems during startup All filtering components on lines bringing signals back to the controller should be located near the controller and tied to the ground plane for the analog ground pin. The evaluation board is a four-layer design with separate power and ground planes. The evaluation board uses a separate analog ground plane on the top layer, this is an important feature that should be included in any layout. Figure (9) shows the output filter components and FETs, the heavy traces should be sized in accordance with the current requirements, be as large as possible, and connected as shown.

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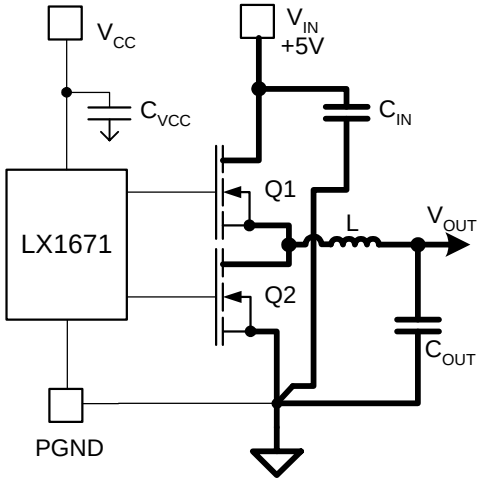

Figure (9) PWM Switch and Output Filter

21.0 DDR VTT TERMINATION SUPPLY

DDR memory systems require a termination voltage (VTT) in addition to the line driver supply voltage (VDDQ) and receiver supply voltage (VDD). A unique feature of the VTT supply is that it must be able to source and sink current as the signals on the bus change states.

VTT for DDR SDRAM can be generated with the LX1673 by using the positive input of the phase 2 error amplifier (EA+) as a reference input. Using VREF, which is defined as one half of VDDQ, for the phase 2 reference input will insure that VTT equals VREF and that all voltages will track each other as required by the JEDEC specification.

See Microsemi Application Note 17 for details on DDR termination requirements and circuit configurations.

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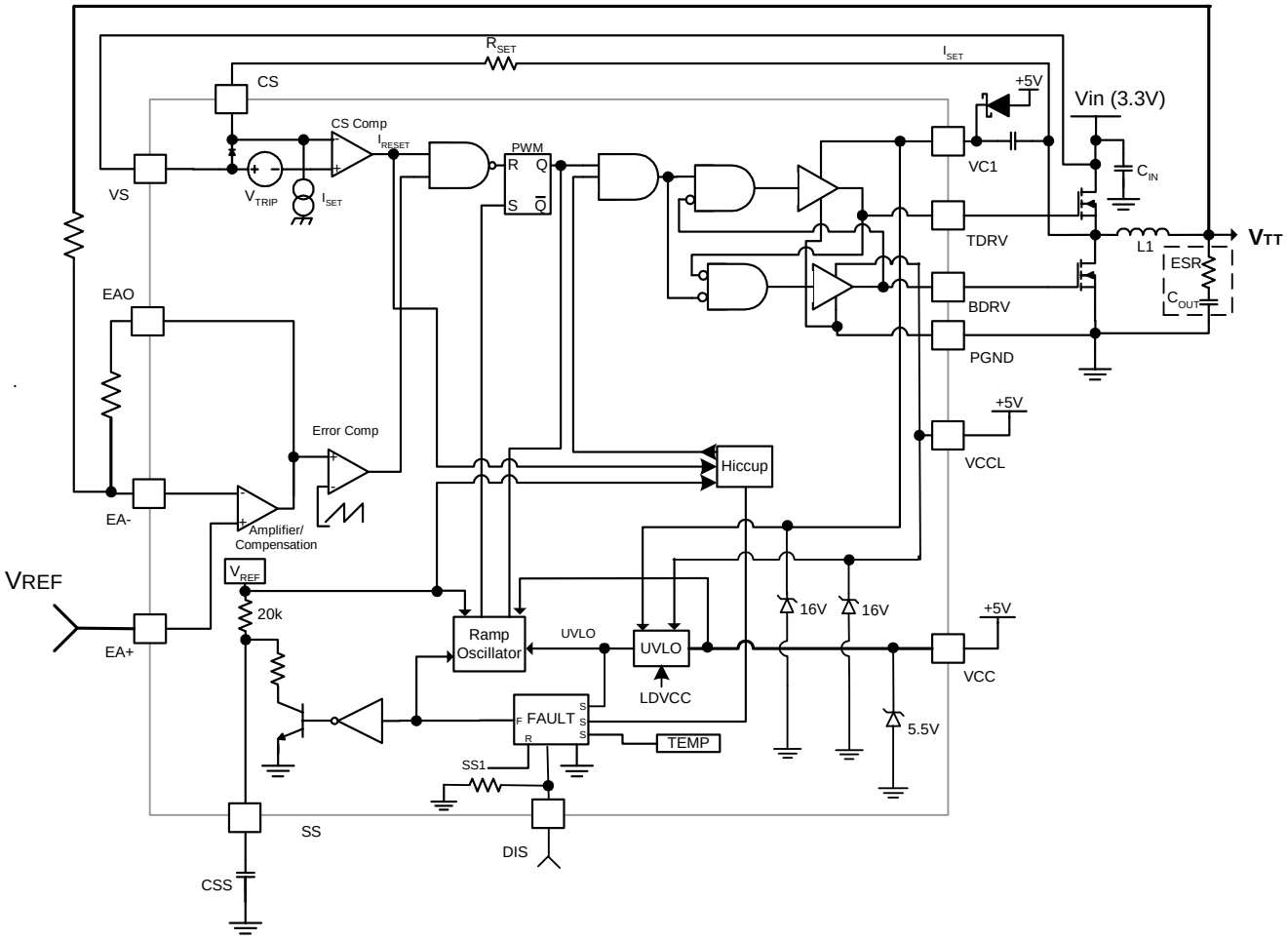

Figure 10 - DDR V_{TT} Supply