AN-17

USING THE LX1672 AND LX1673 FOR DDR SDRAM MEMORY TERMINATION

Microsemi
INTEGRATED PRODUCTS

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1.0 INTRODUCTION

The demand for higher memory speeds has resulted in evolution of the established PC100 / PC133 SDRAM to the newer Double Data Rate (DDR) SDRAM which clocks data on both positive and negative transitions of the clock, two data transfers per clock cycle result in a data rate of 266 MHz while the command and address lines only transition on the positive clock edges for a 133 MHz rate, speed grades for DDR allow for both 200 MHz and 266 MHz data transfer rates.

At higher data rates it is necessary to terminate the bus accurately to manage ringing and reflections. Stub Series Terminated Logic (SSTL) has been developed to allow data rates of 266MHz as required for DDR SDRAMs. JEDEC has released a specification (EIA/JESD8-9A) that defines I/O levels and conditions for operation with SSTL_2 , for 2.5 volt levels vs. the 3.3 volts used in PC133.

A new terminating voltage (V_{TT}) is required as a supply for the terminating resistors and the line driver / receiver supply (VDDQ) is a second new supply voltage required by DDR SDRAM.

The LX167X family of synchronous buck controllers can supply the power required for the termination voltage. The three members of this family LX1671,72,73 have either three, two, or one PWM controllers and one linear regulator controller. Power requirements in addition to V_{TT} can be met with the additional controllers. The LX1672 can supply both VDDQ and V_{TT} using only one package, an example of a circuit using this part is shown in section 8.0.

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2.0 SDR vs DDR SDRAM

DDR memory systems are configured in the same way as the PC133 SDRAM with many similarities in the DIMM packaging and communication protocols, however significant differences exist. The internal addressing , command control interface, and refresh requirements are identical.

Some key differences are the reduction in VDD and VDDQ voltages to 2.5 volts and the requirement for a terminating voltage (V_{TT}), there is also a reference voltage (V_{REF}) that is used on one side of the differential line receiver. The new voltages V_{REF} and V_{TT} must meet the JEDEC standard to insure proper data transmission. V_{TT} has a unique feature in that it must source and sink current.

The DDR clock is a differential signal and allows data transfer on both positive and negative transitions, all other lines are single ended, DDR also uses a new bi-directional data strobe. SDR memory employed a fixed voltage level for signal interface and while DDR data is still single ended the addition of V_{REF} on the negative side of the line receiver allows symmetrical data transfer with superior noise immunity, lower voltage swings on the signal lines, and less jitter.

Table 1 shows some of the key differences between SDR and DDR memory systems with emphasis on DC voltages since memory commands are not the focus of this document.

PARAMETER	SDR	DDR	COMMENTS
VDD and VDDQ	3.3 V	2.5V	Lower power requirements for DDR
V_{REF}	N/A	1/2 VDDQ	Used on line receiver negative input
V_{TT}	N/A	= V_{REF}	Supply for terminating resistors
Data Rate	1X Clock	2X Clock	DDR has a Differential Clock
Signal Interface	LVTTL	SSTL_2	DDR --- JEDEC standard EIA/JESD8-9A

Table 1 – SDR vs DDR Key Differences (Partial List)

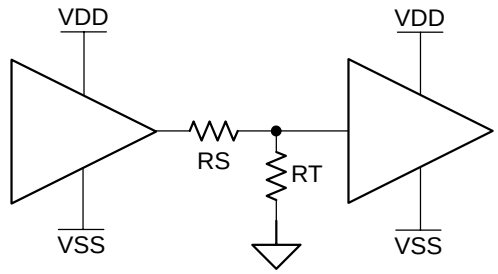
3.0 TERMINATION METHODS

Several methods shown in Figure 1 can be used to terminate a transmission line into its characteristic impedance to minimize ringing and reflections. From the power dissipation point of view there are significant differences that must be taken into account when a large number of lines are being terminated.

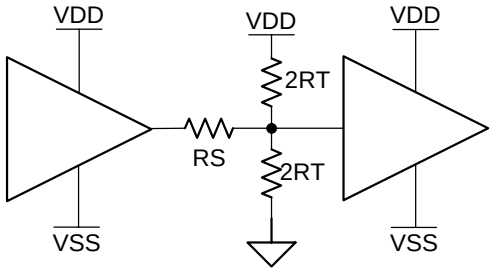
(Fig 1a) Shows a simple resistor to ground with no power dissipation when data is low, dissipation is VDD^2 / RT+RS) for a high signal. Although this works well for single ended lines power consumption is data dependant. The open circuit voltage is zero which will not work with the line receiver used for SSTL.

The second method (Fig 1b) uses two resistors on each line. The Thevenin equivalent is a terminating resistor of RTΩ and an open circuit voltage of VDD/2. For RS=RT power dissipation for both high and low signals is $(3\ VDD)^2$ / 8RT. If the data line is floating there is a constant power dissipation of VDD^2/4RT.

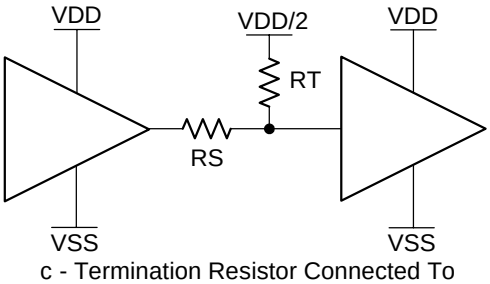
A third method (Fig 1c) uses a single resistor connected to a terminating voltage VDD/2. For either a high or low signal the dissipation is $(VDD/2)^2$ / (RT+RS). There is no power dissipated when the line is floating. This offers a three to one power dissipation advantage over the Thevenin termination with only one termination resistor and also has an open circuit voltage of VDD/2.



a - Grounded Termination resistor



b - Thevinin Termination



c - Termination Resistor Connected To VDD / 2

Figure 1 – Three Bus Termination Methods

4.0 SSTL_2 TERMINATION

Some key differences between SSTL_2 and Figure 1c are the addition of a different supply voltage for the line driver (VDDQ), a termination voltage (V_{TT}), and the reference voltage (V_{REF}) on the negative input of the line receiver .

The SSTL_2 specification requires a minimum signal level, at the input of the line receiver, of 380 mV above and below V_{REF} with the line driver Vout at its maximum high and low voltages. Two classes of termination (Class I and II), Figures 2 and 3, are specified and are intended for different line drivers

Power dissipation in RT and RS is determined by the current output of the line driver which will determine the magnitude of the signal swing. With worst case conditions for a Class II line driver the maximum current in RT could be 31.8 mA (see section 7.0).

There are several other termination methods allowed by the SSTL_2 specification that are not in wide spread use and are not shown here.

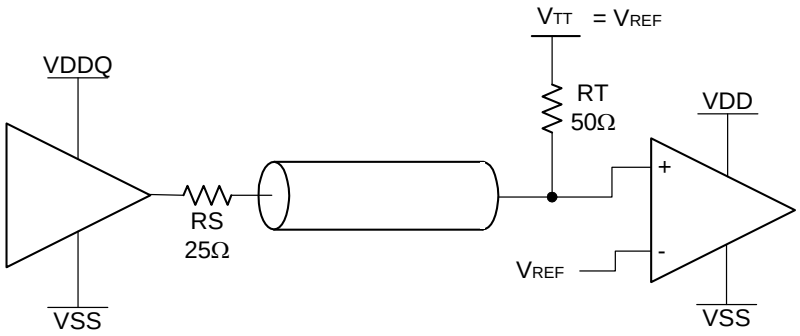


Figure 2 – SSTL_2 Class I Termination

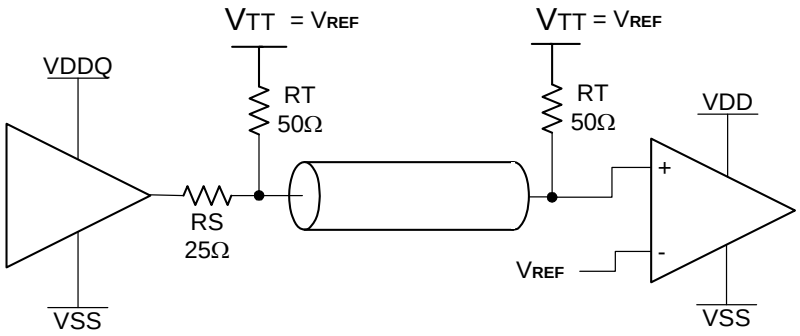


Figure 3 – SSTL _2 Class II Termination

SSTL_2 Class I is used with line drivers having a minimum of 7.6 mA sink or source capability and Class II is used with line drivers having a minimum of 15.2 mA sink and source capability. A variation of Class II is to use a single 25Ω termination resistor at the line receiver. In either case the effective RT is 25Ω resulting in the same current demand on the V_{TT} supply.

5.0 SSTL_2 DRIVERS AND RECEIVERS

Figure 4 shows the basic configuration for the driver and receiver used with SSTL_2. The driver in Fig 4a is not much different from line drivers used in PC133 but has greater drive capability. The receiver in Fig 4b has a differential input and a reference voltage on one side. The data is single ended but must be centered on the V_{REF} voltage for best noise margins, this gives very good performance since the two transistors are matched and the threshold voltage can be tightly controlled by V_{REF}.

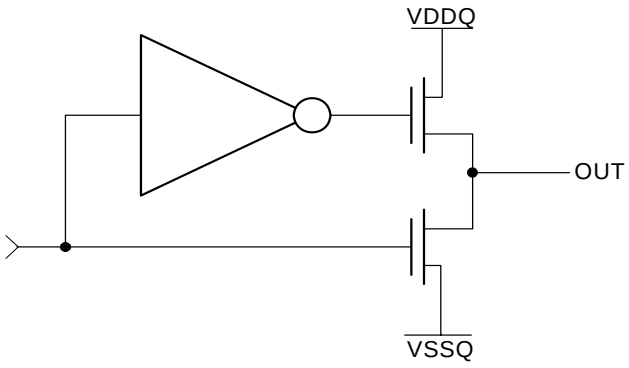


Figure 4a

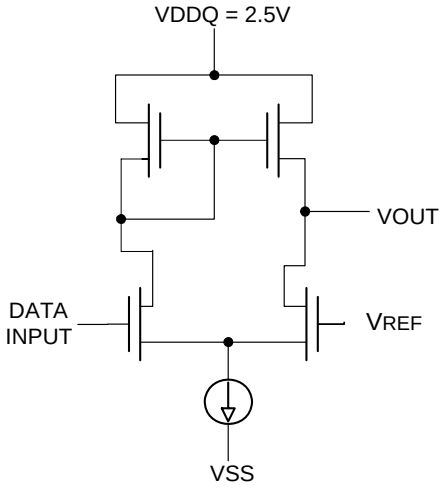


Figure 4B

Figure 4 – SSTL_2 Line Driver and Receiver

6.0 SSTL_2 VOLTAGES

JEDEC standard JESD8-9A contains values for the key voltages which are summarized in Table 2

SYMBOL	PARAMETER	MIN	NOMINAL	MAX	UNITS
VDD	Device Supply Voltage	VDDQ			
VDDQ	Output Supply Voltage	2.3	2.5	2.7	V
V_{REF}	Input Reference Voltage	1.15	1.25	1.35	V
V_{TT}	Termination Voltage	V_{REF} -.04	V_{REF}	V_{REF} +.04	V

Table 2

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Some points to keep in mind when working with these values.

1 VDD is not specified but must be greater than or equal to VDDQ (3.3 V is allowed although the DDR SDRAM specification JESD79 calls for a migration to 2.5 V)

2 V_{REF} is one half of VDDQ (plus or minus 8%) and must track it at all times. (The JEDEC specification allows deviation from VDDQ/2 but most designers will stay with nominal values.)

3 V_{TT} must be within 3.2% of V_{REF}.

4 V_{TT} must track any changes in V_{REF} over all operating conditions.

5 The peak to peak noise on the V_{REF} line must not exceed +/-2% of the V_{REF} DC value. This only allows 25mV of noise.

6 There is no specification for noise on the V_{TT} voltage.

7.0 VTT AND VREF

V_{REF} is only used as an input to devices with very low input current so does not need a low source impedance except for the requirement to keep noise within the 25mV limit. V_{REF} can be supplied by the output of an operational amplifier with appropriate bypassing but this may cause stability problems with the amplifier. A simple and easy V_{REF} source is to use a resistive divider from VDDQ and bypass it at a number of locations with capacitors to the VDDQ and VSSQ rails. The balanced bypassing helps to insure that V_{REF} is kept midway between VDDQ and VSSQ even in the presence of transients.

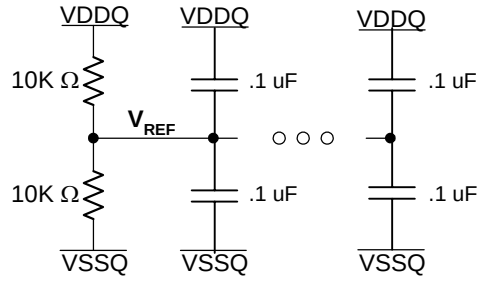

Figure 5 – V_{REF} Divider and Bypassing

The receiver uses V_{REF} as one side of the its input so any noise or deviation in V_{REF} voltage will result in timing errors and jitter. A number of bypass capacitors (ceramic multilayer) located at each DIMM will keep the noise within specification. As always good layout techniques are essential.

Since V_{TT} is used to supply current to the terminating resistors it must have a low source impedance and be able to supply enough current for the number of lines to be terminated.

Using worst case conditions (VDDQ max = 2.7V, V_{TT} min = 1.11V, V_{TT} max = 1.39 V and 0 Ω driver output resistance) but nominal 25 Ω RS and RT.

A driver could source (Figure 10)

(VDDQ max-V_{TT} min) / (RT+RS) = 31.8 mA of V_{TT} current when high,

or sink

V_{TT} max / (RT+ RS) = 27.8 mA when low.

The assumption of a 0 Ω driver is made because SSTL-2 specifies only the minimum output driver current.

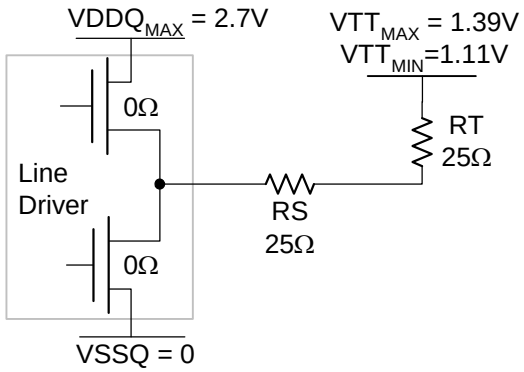

Figure10 – Worst Case RT current

Under nominal conditions (VDDQ=2.5 V and V_{TT} = 1.25 V) the line driver can source or sink 25 mA per line with a 0 Ω output impedance line driver. A bus with equal distribution of high and low signals would place no demand on the V_{TT} supply, however a bus that had all high or all low signals could source or sink currents of several amperes, even with nominal values. V_{TT} must be supplied by a low output impedance source to remain within specification as the loads change.

8.0 LX1672 CONTROLLER

With a number of DIMMs operating from 2.5 volts and the need to generate V_{TT} at a significant amount of current two new voltages are now required on the motherboard. The LX1672 is a dual PWM that can supply both voltages and output current can be scaled to suit the specific board requirements. The LX1671 with three PWMs and the LX1673 with one PWM can be substituted if applicable. The PWM controllers are nearly identical on all devices.

The V_{TT} voltage must track V_{REF} and be able to source and sink current depending on the state of the data. A supply topology that meets this requirement is a synchronous buck regulator with an error amplifier input that can be connected to an external reference voltage. The LX1672 has one PWM with the error amplifier inputs pinned out. V_{REF} can be connected directly to the positive error amplifier input to insure that V_{TT} will be at one half of VDDQ and stay within tolerance over changes in the VDDQ voltage as required by the SSTL_2 specification.

Due to the relatively high currents required for a large number of terminating resistors, 2A to 6 A, the V_{TT} supply should be as close as possible to the terminating resistors and use wide etch in both the V_{TT} and return paths, a number of bypass capacitors (.1uf ceramic multilayer) should located at the terminating resistors.

Figures 6 and 7 are block diagrams showing the LX1672 developing both V_{TT} and VDDQ from a 3.3 volt input, Figure 8 is a schematic of the same configuration showing the complete solution to develop both voltages. The LDO is not shown but could be connected if a third output is required.

When an external reference is used the connection between the error amplifier positive input and the Soft Start pin is lost and Soft Start will not function. It is recommended that the external reference voltage have an R-C time constant that will be long enough to allow the output capacitor to charge slowly.

For details on circuit operation, component selection , and other circuit configurations see the Microsemi LX1672 Data Sheet and LX1672 Product Design Guide or equivalent documents for the LX1671 and LX1673.

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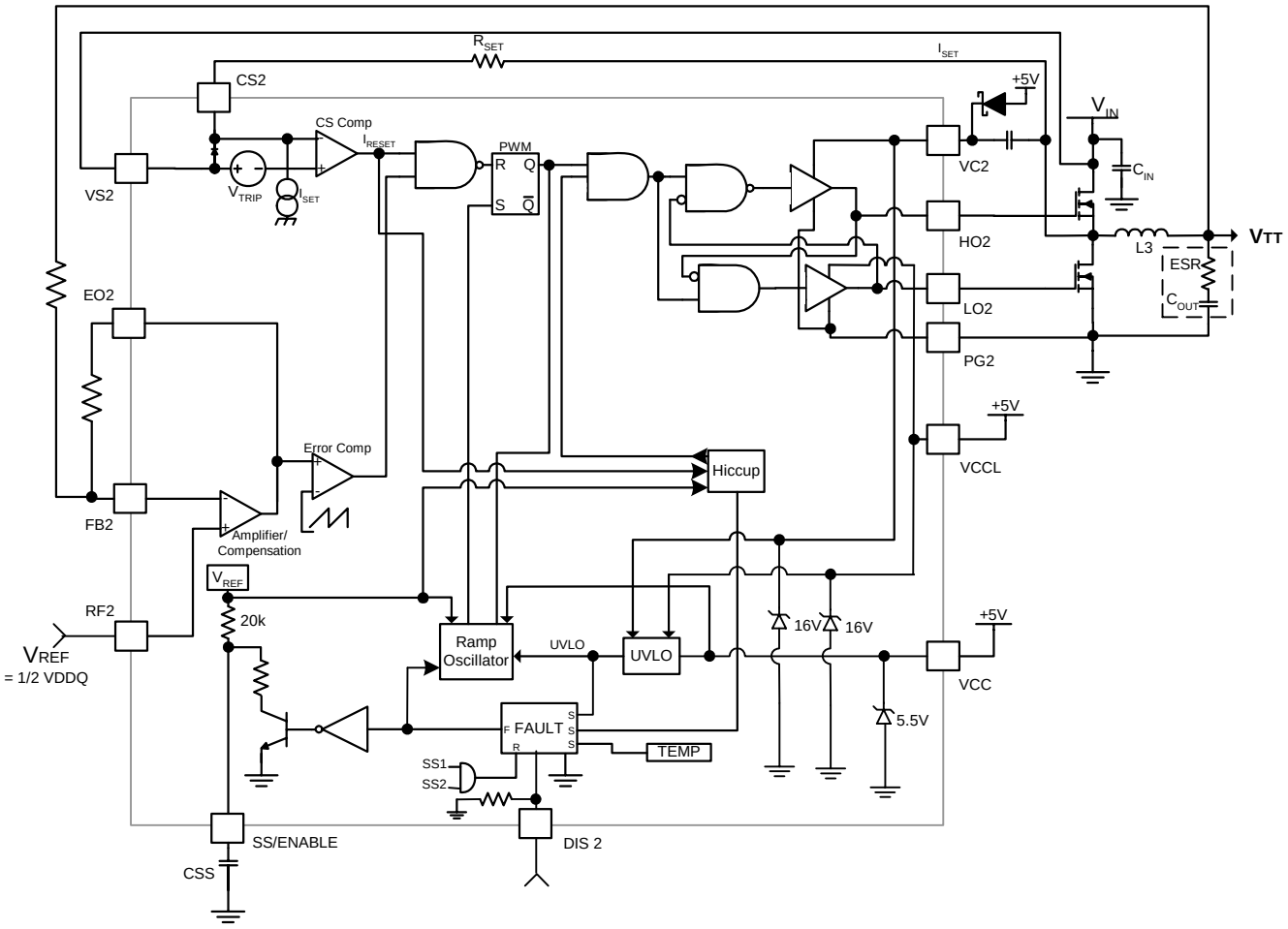

Figure 6 – LX1672 V_{TT} Supply Block Diagram

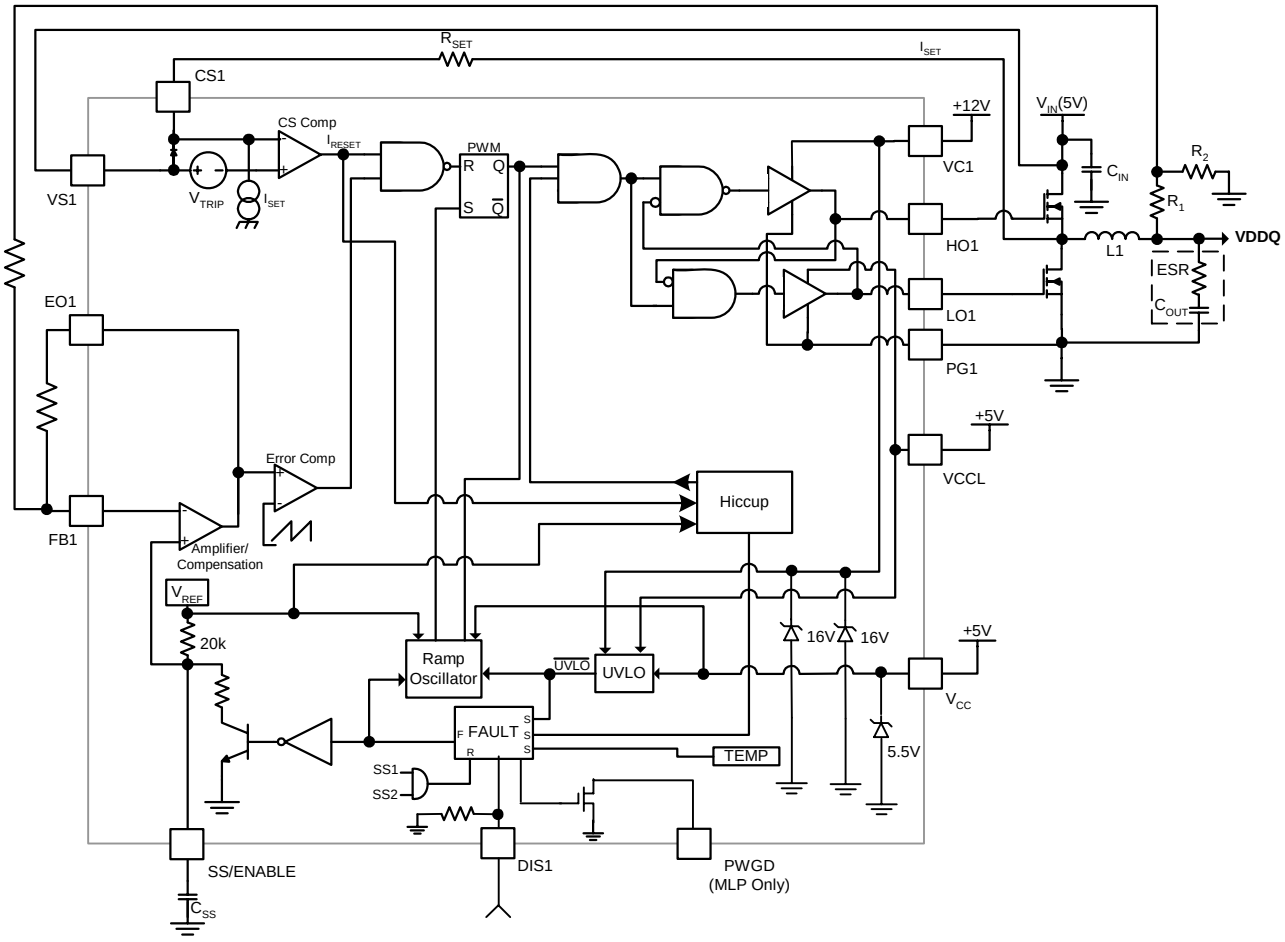

Figure 7 – LX1672 VDDQ Supply Block Diagram

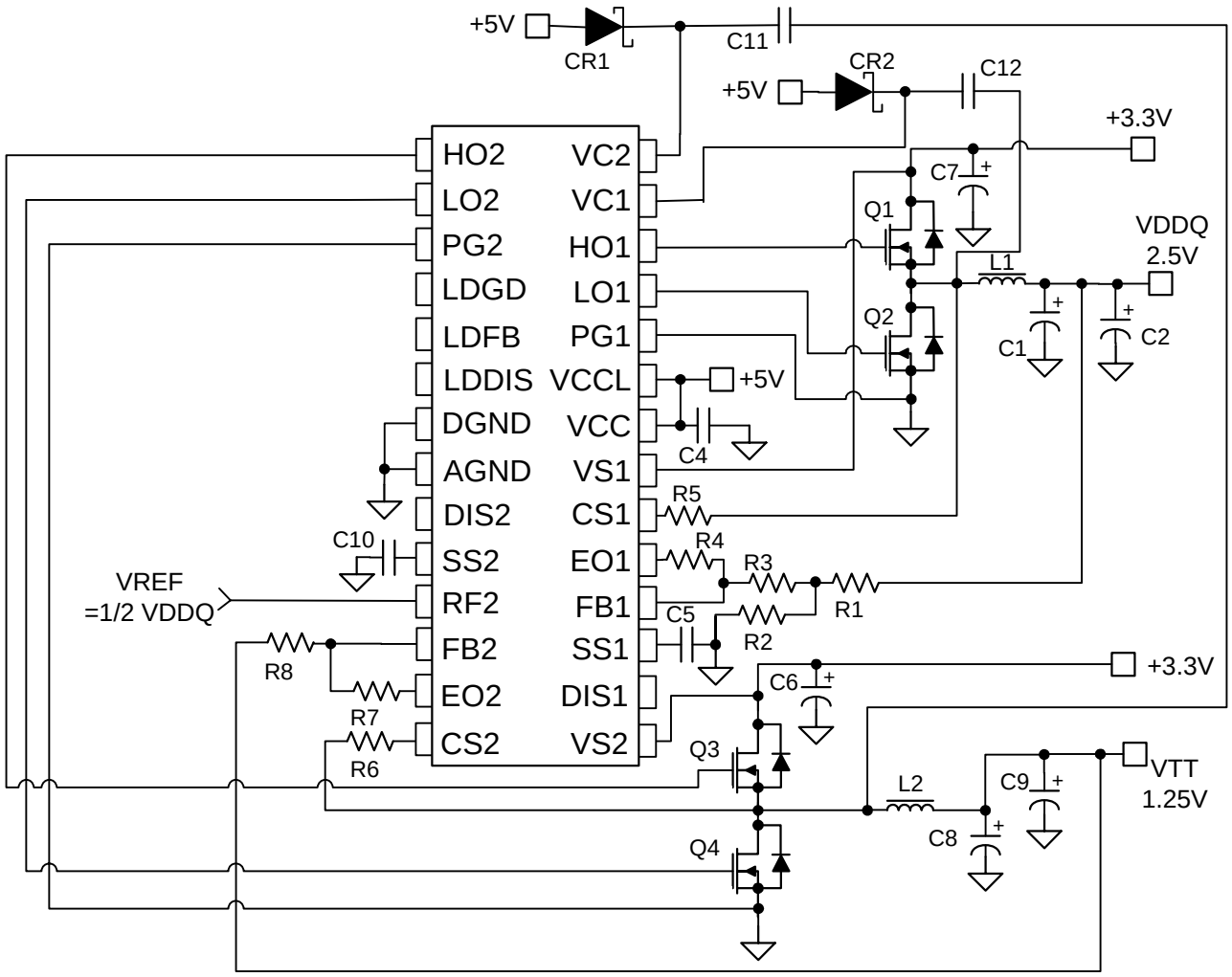

Figure 8 – Schematic LX1672 V_{TT} and VDDQ supply

MISCELLANEOUS COMPONENTS					
Line Item	**Part Description**	**Manufacturer & Part #**	**Case**	**Reference Designators**	**Qty**
1	PWM Controller	**MICROSEMI** LX1672-03CLQ	MLP	U1	1
2	MOSFET N Channel	**VISHAY** Si4842DY	SO-8	Q1 – Q4	4
3	Schottky Diode, 1A 20V	**MICROSEMI** UPS5817	PWRMITE	CR1, CR2	2
4	Inductor 5.0µH, 6.5A	**COOPER** CTX5-4A	SMD	L1, L2	2

CAPACITORS					
Line Item	**Part Description**	**Part Description**	**Case**	**Reference Designators**	**Qty**
1	180µF, 4V Polymer Electrolytic	**CDE** ESRE181M04B	D 7.3 x 4.3	C1, C2, C6, C7	4
2	270µF, 2V Polymer Electrolytic	**CDE** ESRE271M02B		C8, C9	2
3	0.1µF, 25V ±10%	**ROHM** MCH182CN104KK	0805	C5, C11, C12	3
4	0.22µF, 25V ±10%	**ROHM** MCH182CN224KK	0805	C10	1
5	4.7µF, 6.3V Ceramic	**MURATA** GMR219R60J475K	0805	C4	1

RESISTORS					
Line Item	**Part Description**	**Part Description**	**Case**	**Reference Designators**	**Qty**
1	2K 1% 1/8W	**ROHM** MCR10F2001	0805	R2, R3, R5, R6, R8	5
2	200K 1% 1/8W	**ROHM** MCR10F2003	0805	R4, R7	2
3	4.42K 1% 1/8W	**ROHM** MCR10F4421	0805	R1	1

Table 3 – Bill Of Material for LX1672 V_{TT} and VDDQ Supply

9.0 LX1673 CONTROLLER

The LX1673 single phase PWM controller may be used to generate two output voltages if the internal LDO controller is used. Figure 10 is a block diagram of the LX1673 showing its use as a single output V_{TT} supply. Figure 11 is a schematic of the LX1673 configured for a V_{TT} supply with the LDO feature not being used.

When an external reference is used the connection between the error amplifier positive input and the Soft Start pin is lost and Soft Start will not function. It is recommended that the external reference voltage have an R-C time constant that will be long enough to allow the output capacitor to charge slowly.

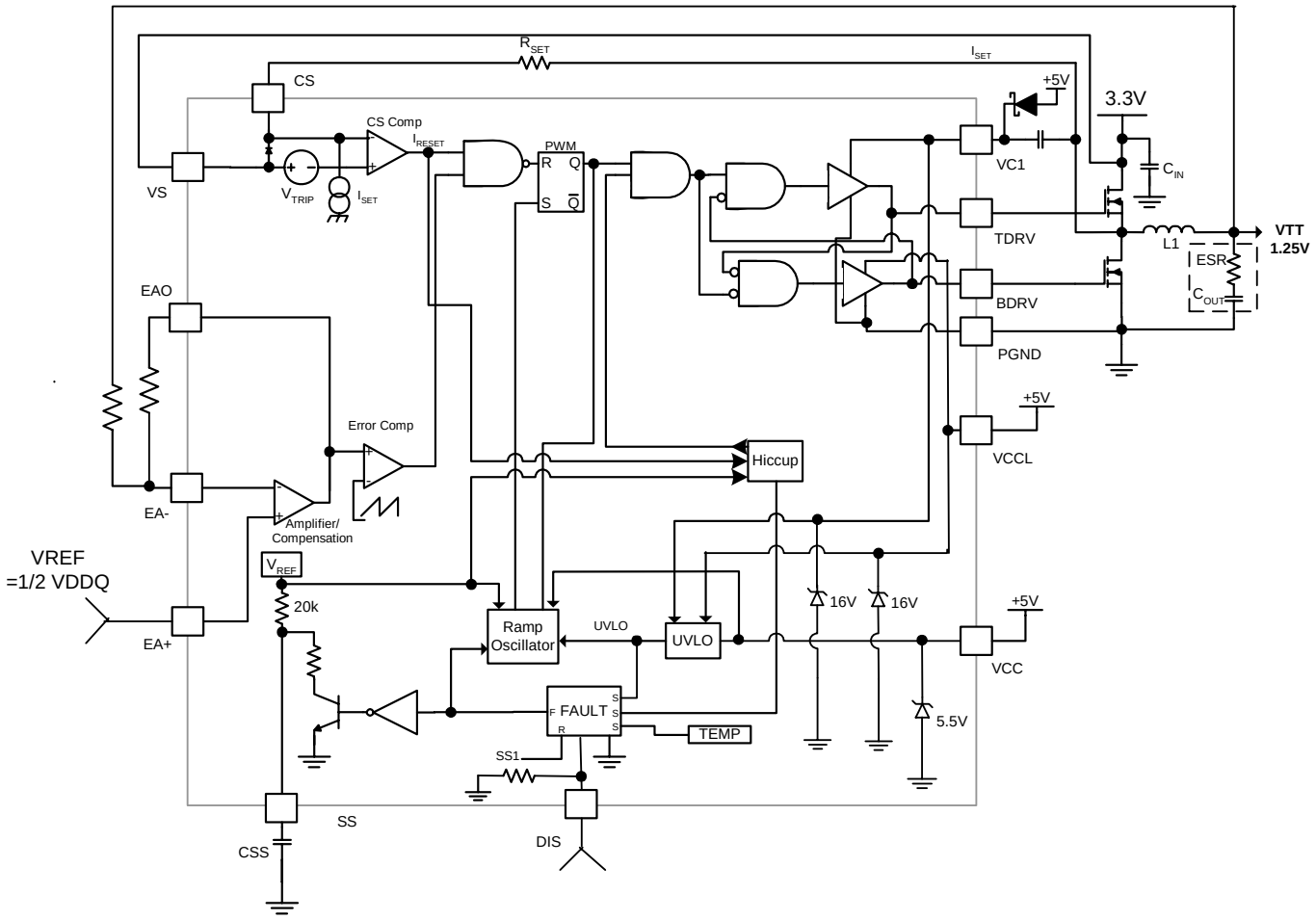

Figure10 – LX1673 V_{TT} Supply Block Diagram

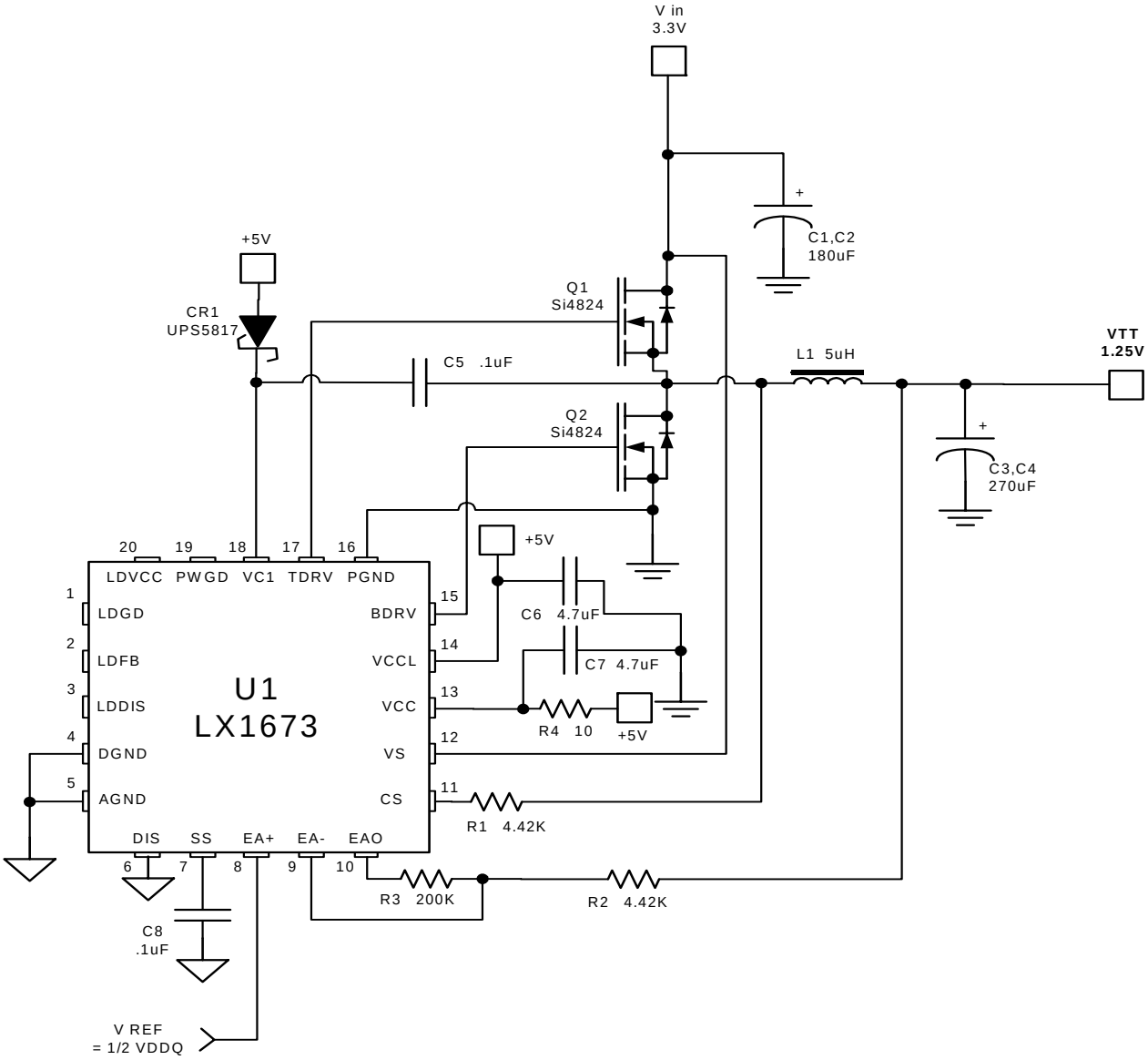

Figure 11 – Schematic LX1673 V_{TT} Supply (LDO not used)

MISCELLANEOUS COMPONENTS					
Line Item	**Part Description**	**Manufacturer & Part #**	**Case**	**Reference Designators**	**Qty**
1	PWM Controller	**MICROSEMI** LX1672-03CLQ	MLP	U1	1
2	MOSFET N Channel	**VISHAY** Si4842DY	SO-8	Q1 – Q2	2
3	Schottky Diode, 1A 20V	**MICROSEMI** UPS5817	PWRMITE	CR1	1
4	Inductor 5.0µH, 6.5A	**COOPER** CTX5-4A	SMD	L1	1

CAPACITORS					
Line Item	**Part Description**	**Part Description**	**Case**	**Reference Designators**	**Qty**
1	180µF, 4V Polymer Electrolytic	**CDE** ESRE181M04B	D 7.3 x 4.3	C1, C2	2
2	270µF, 2V Polymer Electrolytic	**CDE** ESRE271M02B		C3, C4	2
3	0.1µF, 25V ±10%	**ROHM** MCH182CN104KK	0805	C5, C8	2
4	4.7µF, 6.3V Ceramic	**MURATA** GMR219R60J475K	0805	C6, C7	2

RESISTORS					
Line Item	**Part Description**	**Part Description**	**Case**	**Reference Designators**	**Qty**
1	10 Ohm, 1% 1/8W	**ROHM** MCR10F10R0	0805	R4	1
2	200K 1% 1/8W	**ROHM** MCR10F2003	0805	R3	1
3	4.42K 1% 1/8W	**ROHM** MCR10F4421	0805	R1, R2	2

Table 4 – Bill Of Material for LX1673 V_{TT} Supply