MicroNote 117

Protecting USB Data I/O Ports

By Mel Clark and Kent Walters

Computers operating with two-wire USB systems transfer data at 12 Mbps, about 40 times faster than conventional PCs. This high speed is made possible with the use of CMOS ASIC interfacing devices. However, such components are inherently sensitive to electrostatic discharge (ESD), according to the Reliability Analysis Center in Rome, New York.

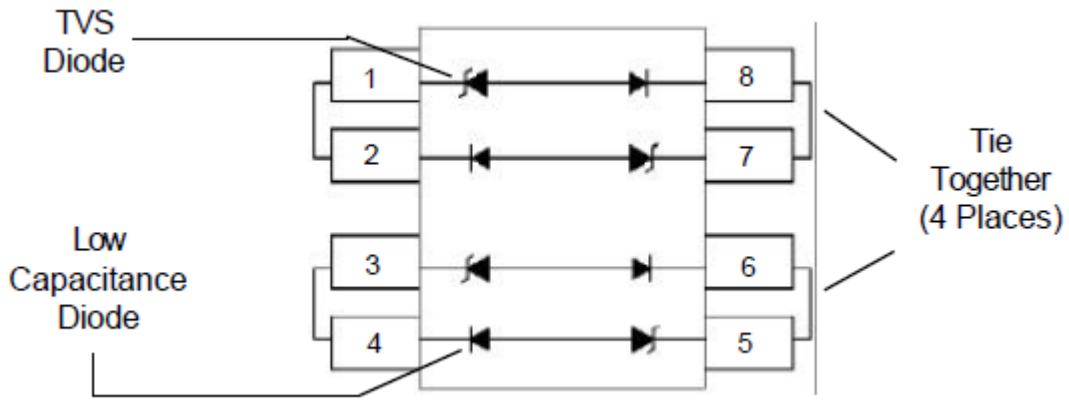
More than 90% of high speed CMOS devices fail at ESD thresholds of less than 2 kV. Because you can't feel this level of ESD with your fingertip, a device can be zapped without your knowledge.

Microsemi now offers a silicon transient voltage suppressor (TVS), the USB0805C, for ESD protection across sensitive USB data I/O ports. These TVS devices protect two-wire USB systems and are available in the SO-8 package for minimum size footprint. Major features of this TVS include:

- Capacitance of <5 pF per line
- Nanosecond response
- Low parasitic inductance
- 300 W peak pulse power at 8/20 µs
- Leakage <50 nA at 3.5 V

The electrical configuration of this TVS device is shown in the following illustration. A single-wire protector consists of two anti-parallel devices in parallel, as shown.

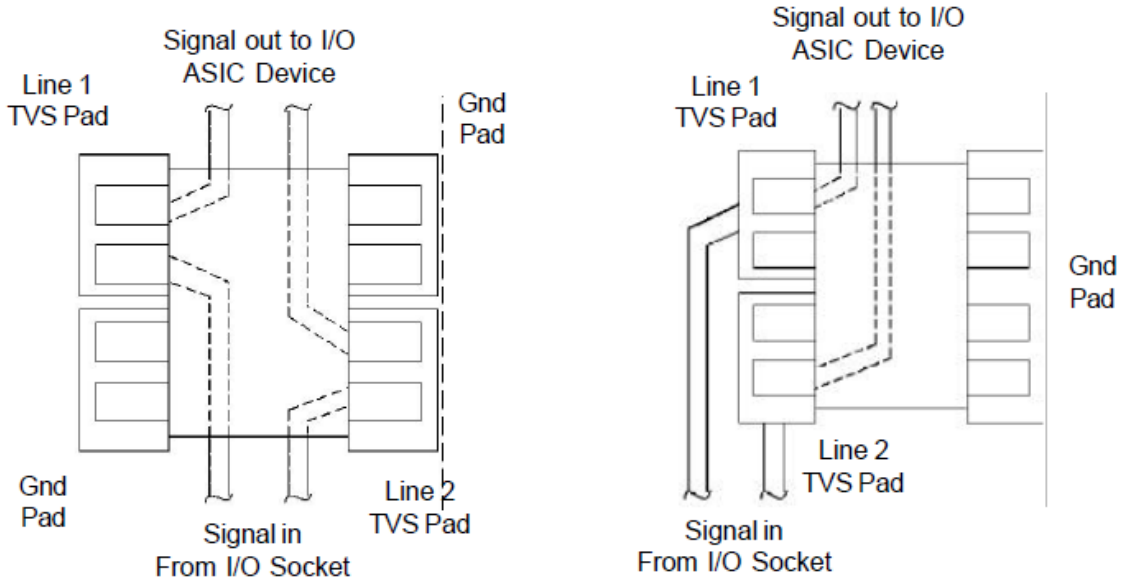
Electrical Configuration



The low-capacitance feature is achieved by placing a high-voltage rectifier chip—which inherently has a low capacitance—in series with the low-voltage TVS chip, which has a high capacitance. This combination will suppress only in one direction, making it necessary to place a second set of identical chips anti-parallel to the first. This requires pins 1 and 2 (as well as 7 and 8) be tied together to provide a single bidirectional protector. Pins 3 and 4 form a common tie point, along with 5 and 6, for the second protector in the package. For a single communication wire, each TVS has a capacitance of <5 pF per line, which is very low compared to MOV technology.

Because the TVS is electrically bidirectional, either end of the pair can be connected to the protected line. This provides the designer with flexibility of layout options. Two alternatives are shown in the following illustration.

Options for Board Mounting on Four Pads



Keep in mind that taking direct, connective paths to the suppressor mounting pads minimizes parasitic inductance in the surge current conductive path. This minimizes L(di/dt) effects, as described in MicroNote 111. Each trace effectively has a Kelvin contact with the pad to which the TVS is connected.

The ground termination pads should be connected directly to a ground plane on the board for optimum performance. A single trace ground conductor will not provide an effective path for fast rise-time transient events, including ESD, due to parasitic inductance.

Nominal inductive values of a PCB trace are approximately 20 nH/cm. This value may seem small, but an apparent short length of trace might be enough to produce significant L(di/dt) effects with fast rise-time ESD spikes.

Mount the TVS as close as possible to the I/O socket to reduce radiation originating from the transient as it is routed to ground.

Support

For additional technical information, please contact Design Support at:
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