DRF Series SPICE Models

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Introduction

This application note presents SPICE Models for DRF100, DRF1200 and DRF1300 and DRF1400. These models are presented in two forms. The first, most straightforward, form is in applications where node zero (0), (ground), is at zero volts at all times. **This form is written for Intusoft SPICE.** The second form is where the node zero (0), (ground), is not at zero volts and may have a high frequency component. **This form is valid for most SPICE platforms.**

DRF100 SPICE Model

This section discusses the three elements of the DRF100 SPICE Model: the symbol, the sub circuit, and the test circuit. Illustrated in Figure 1 is the DRF100 SPICE symbol. All pin locations, function and labeling are the same as the data sheet.

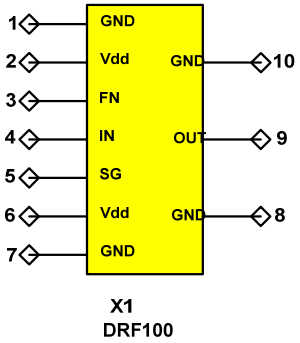

Figure 1 DRF100 SPICE Symbol. See Note 1.
Developed for Intusoft SPICE

DRF100 Sub Circuit Diagram

The DRF100 sub circuit diagram is illustrated in Figure 2. X2 the MAX9010 model is used as the input comparator, the switching speed is a close match to the DRF100 input; however the hysteresis has been altered to more closely model the DRF100 performance. The XNOR gate A1 is used to provide the invert function of the FN pin. Inverter A2 and Buffer A3 are used to create the device delay, and gates X3A and X3B provide the drive for the differential pair X7 and X5. These two devices provide the drive, level match and signal timing for the half-bridge output devices X1 and X6. L2, C3 and R11 model the output characteristics of the DRF100. All parameters of the DRF100 Model are accurate with respect to the device performance with the exception of the DC idle current. The specification is ≅ 2mA however the model idle current is ≅ 4mA.

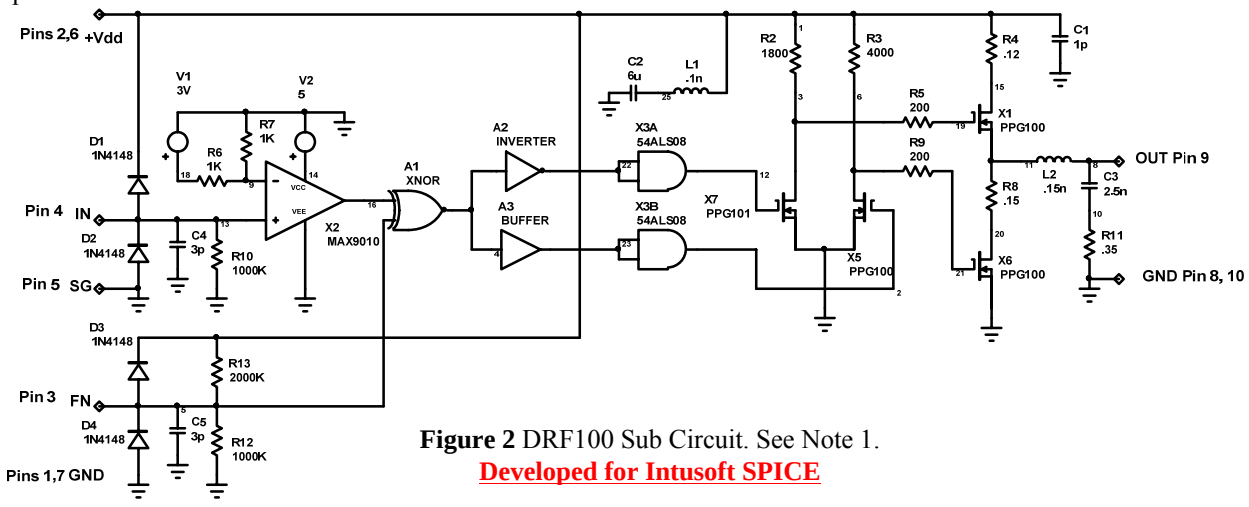

Figure 2 DRF100 Sub Circuit. See Note 1.
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DRF100 SPICE Test Circuit

The DRF100 SPICE test circuit is illustrated in Figure 3. The pulse generator V2 allows the model to be tested over the operating range as described in the data sheet. In actual circuit operation and PCB layout the FN pin may be left open if the inverting function is not used, however the SPICE Model requires that FN pin 3 be connected to at least 1 additional component, C3 a 1pF capacitor is used in the SPICE test circuit.

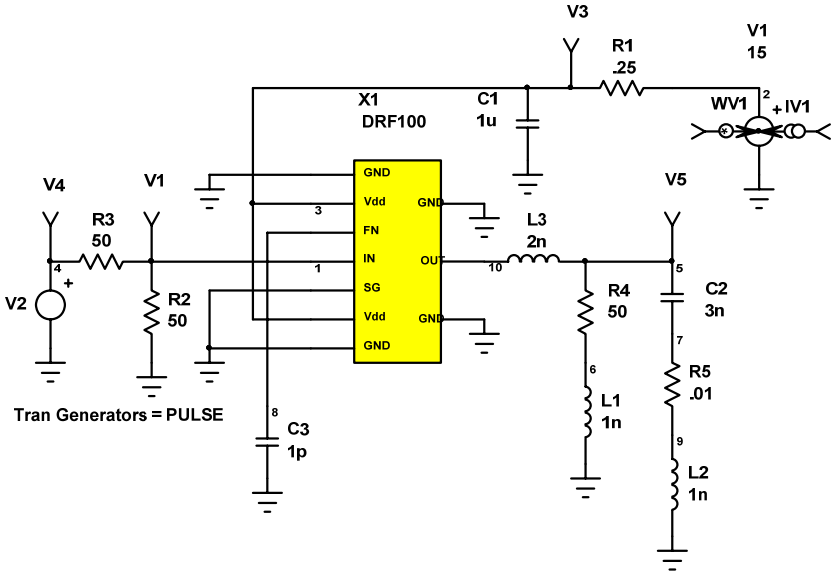

Figure 3 DRF100 SPICE Test Circuit. See Note 1.

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Note 1

The DRF100.DWG file is the sub circuit illustrated in Figure 2 and the symbol file in Figure 1. Both are necessary for all DRF100 modeling. Test circuit, Figure 3, is very useful for device evaluation. The DRF100 TEST.DGW file is the test circuit illustrated in Figure 3.

The DRF100 SPICE Model node (0) is limited to a fixed V=0 and ΔV=0 potential. The model will not function if node (0) is at a DC potential > 0 or a time varying signal that is not equal to zero. See next section.

DRF100 SPICE Model for Non-Zero Reference Planes.

Non Zero Reference Planes are defined as those Planes where node (0) is not 0V and may also be a time varying signal.

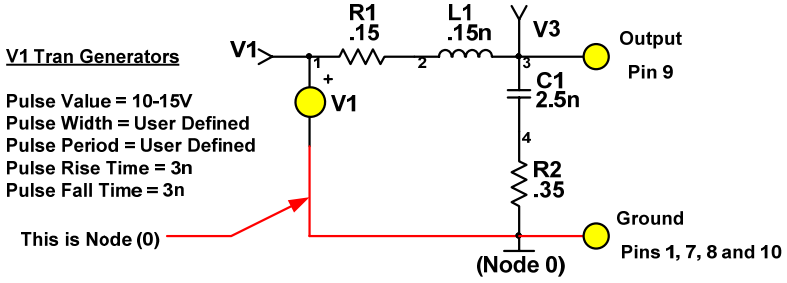

Figure 4 DRF100.

This Model should work with most SPICE platforms.

The Model illustrated in Figure 4 will operate correctly for any signal type or value at node (0).

Pulse value should be set to between 10V and 15V.

Pulse rise time and pulse fall time must be set at 3 ns (3 nano-seconds).

All other parameters should be set to circuit requirements, which are within the data sheet capabilities of the DRF100. Throughput delays are not incorporated in this model.

DRF1200 SPICE Model

This section discusses the three elements of the DRF1200 SPICE Model: the symbol, the sub circuit and the test circuit. Illustrated in Figure 5, is the DRF1200 SPICE symbol. All pin locations, function and labeling are the same as the data sheet.

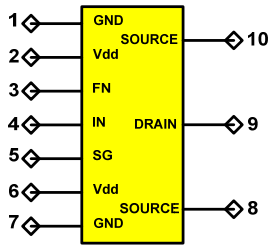

Figure 5 DRF1200 SPICE Symbol
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DRF1200 Sub Circuit Diagram

The DRF1200 series are single ended configurations of one power MOSFETs and one DRF100 driver. The DRF1200 sub circuit diagram is illustrated in Figure 6. X1 the MAX9010 model is used as the input comparator, the switching speed is a close match to the DRF1200 input; however the hysteresis has been altered to more closely model the DRF1200 performance. The XNOR gate A1 is used to provide the invert function of the FN pin. Inverter A2 and the Buffer A3 are used to create the device delay, and gates X6A and X7A provide the drive for the differential pair X9 and X5. These two devices provide the drive, level shifting and signal timing for the half-bridge output devices X2 and X6. L1, C1 and R6 model the output characteristics of the DRF100 Driver IC. X8, the ARF466 is the output power MOSFET used in the DRF1200. All parameters of the DRF1200 Model are accurate with respect to the device performance with the exception of the DC idle current. The specification is ≅ 2mA however the model idle current is ≅ 4mA. See Note 1.

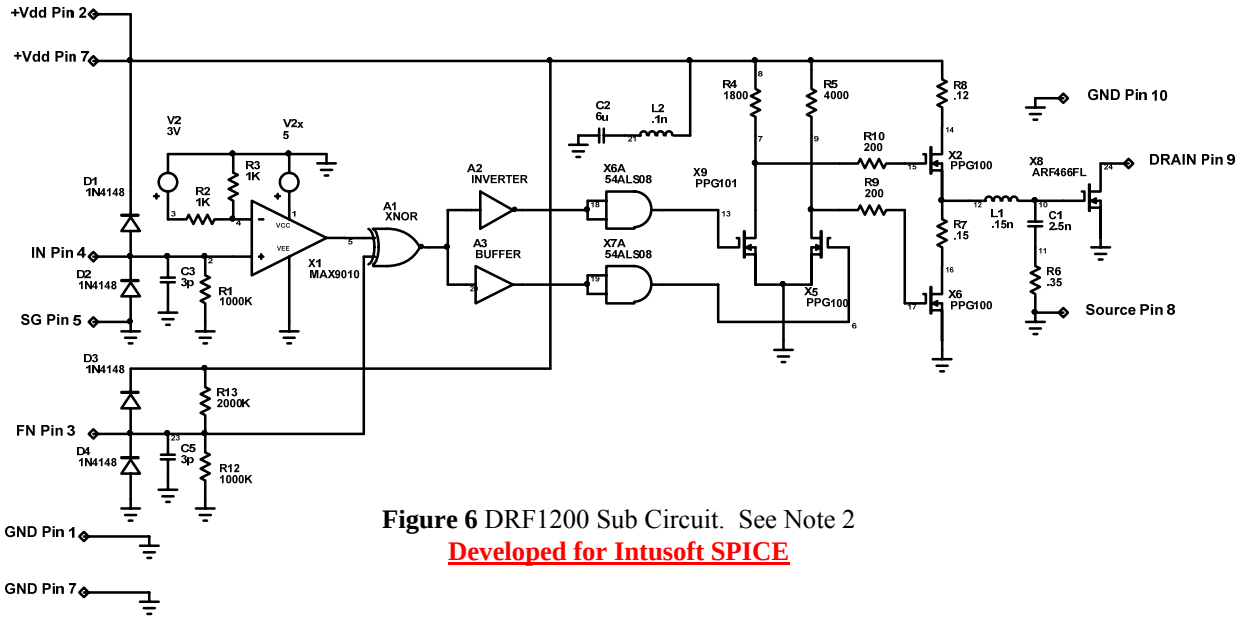

Figure 6 DRF1200 Sub Circuit. See Note 2
Developed for Intusoft SPICE

DRF1200 SPICE Test Circuit

The DRF1200 SPICE test circuit is illustrated in Figure 7. The pulse generator V2 allows the model to be tested over the operating range as described in the data sheet. In actual circuit operation and PCB layout the FN pin may be left open if the inverting function is not used, however the SPICE Model requires that FN pin 3 be connected to at least 1 additional component. In Figure 7, C2, a 1pF capacitor is used.

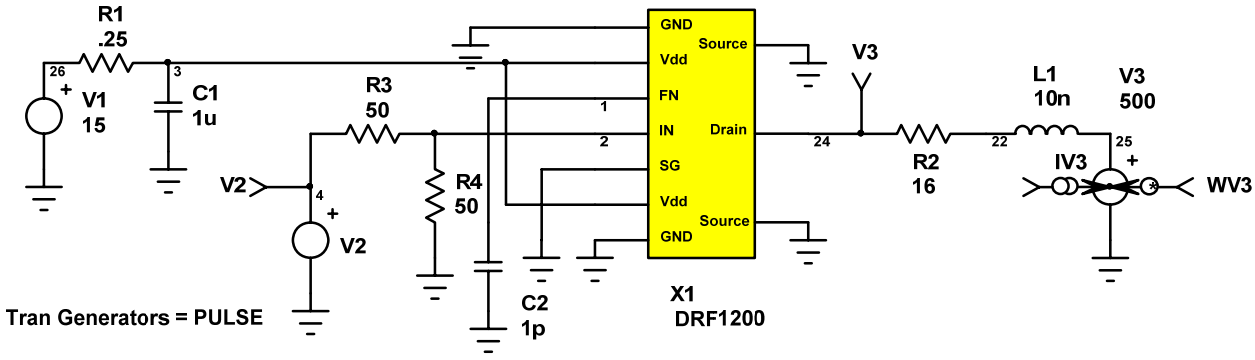

Figure 7 DRF1200 SPICE Test Circuit. See Note 2.

Developed for Intusoft SPICE

Note 2

The DRF1200.DWG file is the sub circuit illustrated in Figure 6 and the symbol file, Figure 5. Both are necessary for all DRF1200 modeling. Test circuit, Figure 7, is very useful for device evaluation. The DRF1200 TEST.DGW file is the test circuit illustrated in Figure 7.

The DRF1200 SPICE Model node 0 is limited to a fixed V=0 and ΔV=0 potential. The model will not function if node (0) is at a DC potential > 0, or a time varying signal that is not equal to zero. See next section.

DRF1200 SPICE Model for Non-Zero Reference Planes.

Non Zero Reference Planes are defined as those Planes where node (0) is not 0V and may also be a time varying signal.

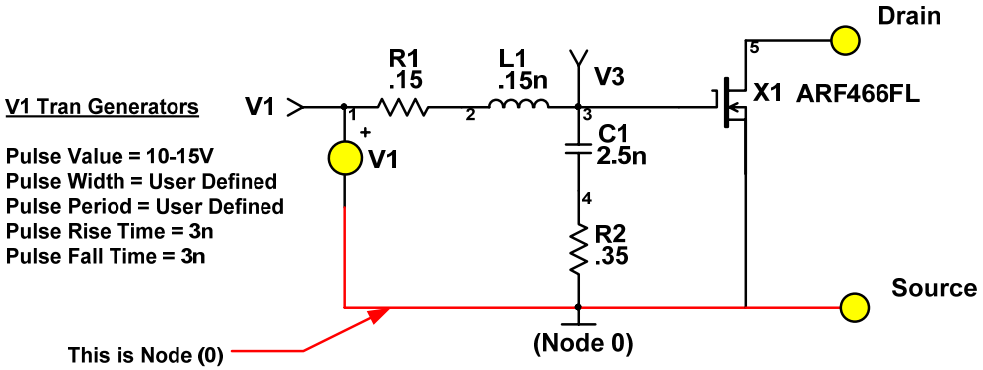

Figure 8 DRF1200

This Model should work with most SPICE platforms.

The Model illustrated in Figure 8 will operate correctly for any signal type or value at node (0).

Pulse value should be set to between 10V and 15V.

Pulse rise time and pulse fall time must be set at 3 ns (3 nano-seconds).

All other parameters should be set to circuit requirements, which are within the data sheet capabilities of the DRF1200. Throughput delays are not incorporated in this model.

DRF1300 SPICE Model

The DRF1300 series are push-pull configurations of two power MOSFETs and two DRF100 drivers. This section discusses the three elements of the DRF1300 SPICE Model: the symbol, the sub circuit, and the test circuit. Illustrated in Figure 9 is the DRF1300 SPICE symbol. All pin locations, function and labeling are the same as the data sheet.

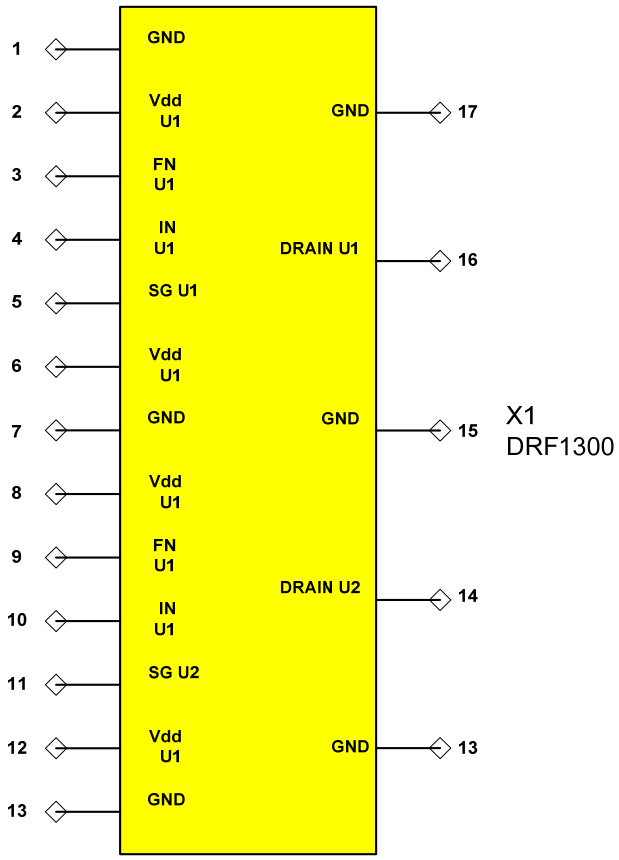

Figure 9 DRF1300 SPICE Symbol, See note 3

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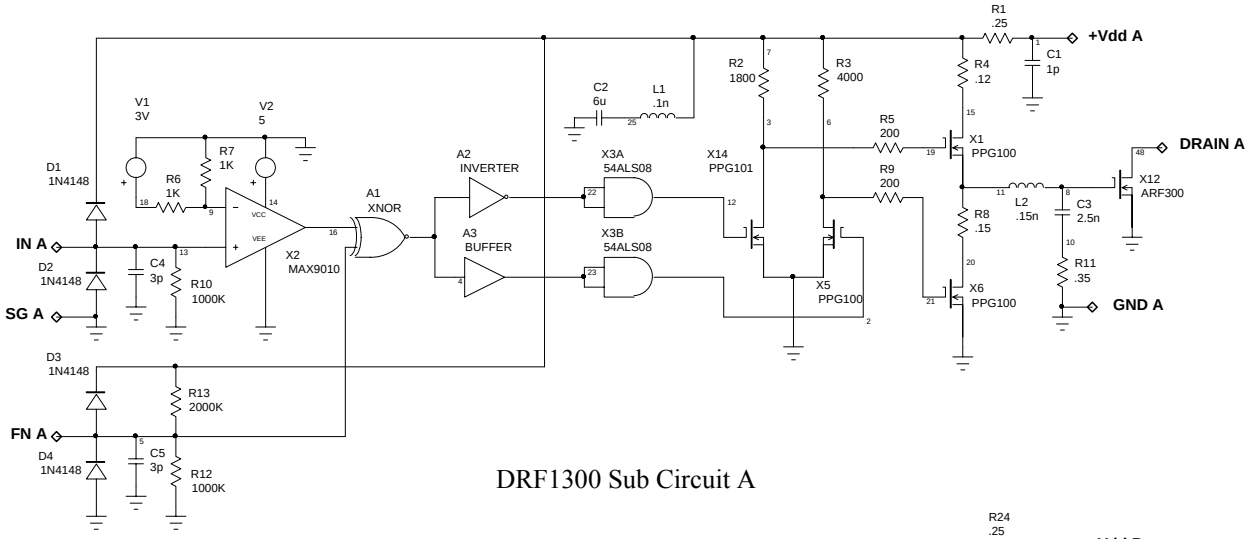
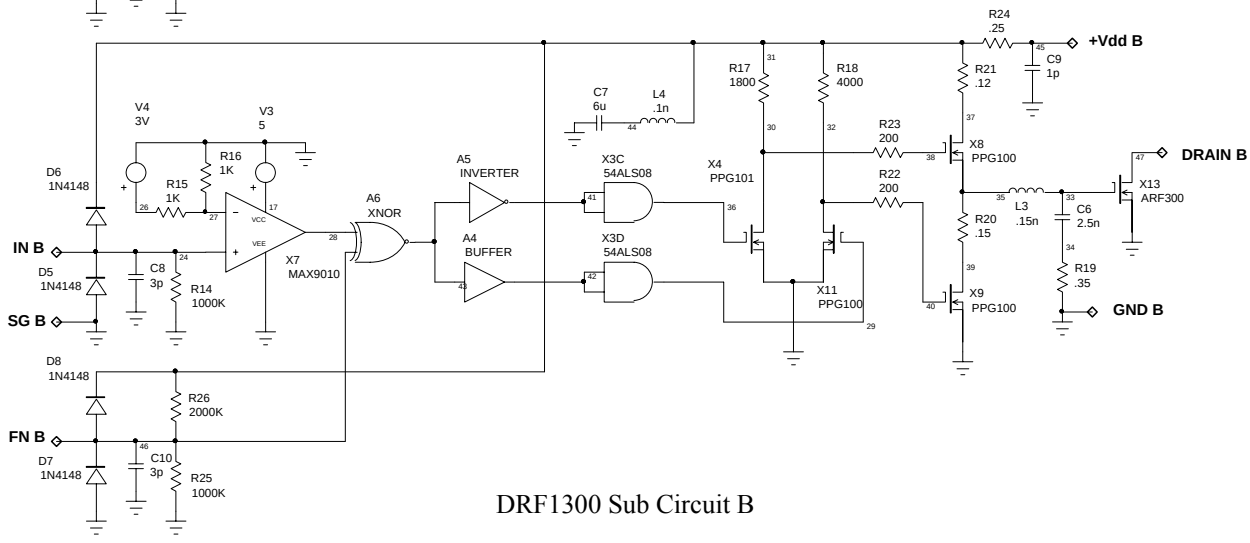
DRF1300 Sub Circuit Diagram A and B

The DRF1300 sub circuit diagram is illustrated in Figure 10. The DRF1300 contains two sub circuits: A and B. These two circuits are the identical topology used in the DRF1200. For this reason we will only follow the signal flow for sub circuit A. X2 the MAX9010 model is used as the input comparator, the switching speed is a close match to the DRF1300 input; however the hysteresis has been altered to more closely model the DRF1300 performance. The XNOR gate A1 is used to provide the invert function of the FN pin. Inverter A2 and buffer A3 are used to create the device delay, and gates X3A and X3B provide the drive for the differential pair X14 and X5. These two devices provide the drive, level match and signal timing for the half-bridge output devices X1 and X6. L2, C3 and R11 model the output characteristics of the Driver IC. All parameters of the DRF1300 Model are accurate with respect to the device performance with the exception of the DC idle current. The specification is ≅ 2mA however the model idle current is ≅ 4mA. See Note 1.



DRF1300 Sub Circuit A



DRF1300 Sub Circuit B

Figure 10 DRF1300 Sub Circuit. See Note 3.

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DRF1300 SPICE Test Circuit

The DRF1300 SPICE Test Circuit is illustrated in Figure 11. The pulse generator V2 allows the model to be tested over the operating range as described in the data sheet. In actual circuit operation and PCB layout the FN pin may be left open if the inverting function is not used, however the SPICE Model requires that FN pin 3 be connected to at least 1 additional component. C3, a 1pF capacitor, is used in the test circuit. R4 sets the drain current to 30A. L1 provides the affect of the circuit stray inductance in the test fixture. The lower half of the DRF1300 operates in the same fashion as the discussion for the U1 section above.

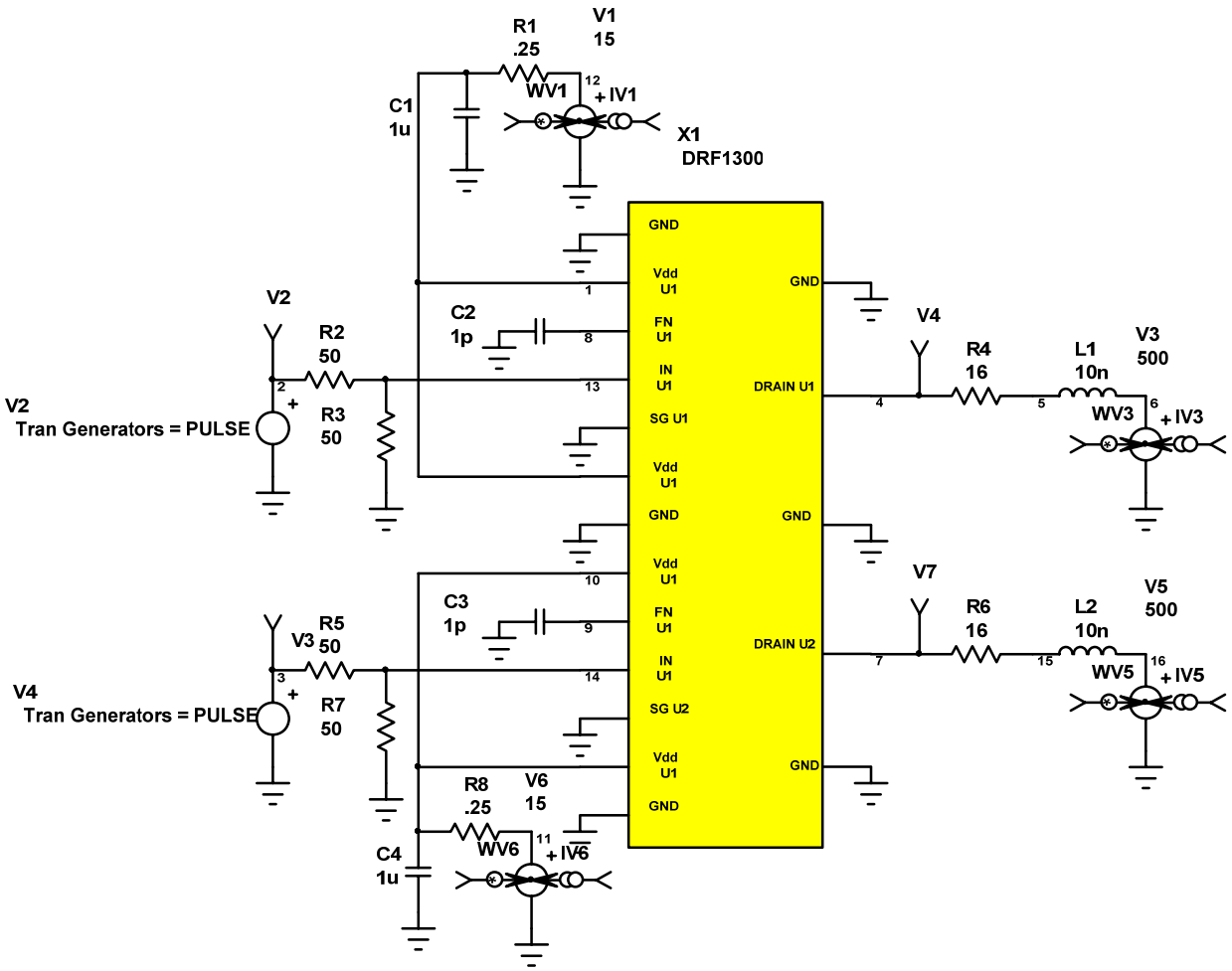

Figure 11 DRF1300 SPICE Test Circuit. See Note 3.

Developed for Intusoft SPICE

Note 3

The DRF1300.DWG file is the sub circuit illustrated in Figure 10 and the symbol file in Figure 9. Both are necessary for all DRF1300 modeling. Test Circuit, Figure 11, is very useful for device evaluation. The DRF1300 TEST.DWG file is the test circuit illustrated in Figure 11.

The DRF100 SPICE Model, node 0 is limited to a fixed V=0 and ΔV=0 potential. The model will not function if node (0) is at a DC potential > 0 or a time varying signal that is not equal to zero. See next section.

DRF1300 SPICE Model for Non-Zero Reference Planes.

Non Zero Reference Planes are defined as those Planes where node (0) is not 0V and may also be a time varying signal.

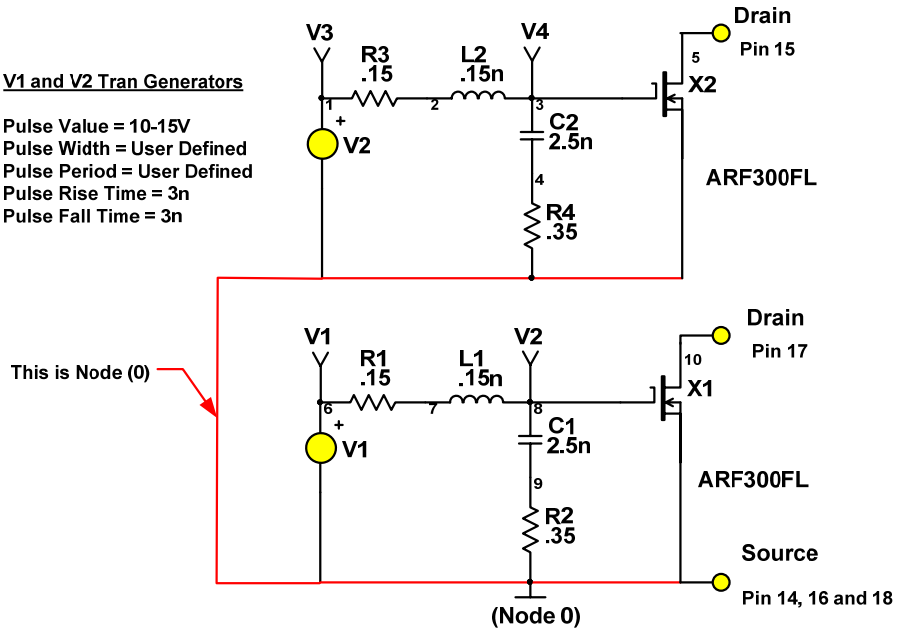

Figure 12 DRF1300

This Model should work with most SPICE platforms.

The Model illustrated in Figure 12 will operate correctly for any signal type or value at node (0).

Pulse value is set to between 10V and 15V.

Pulse rise time and pulse fall time must be set at 3ns (3 nano-seconds).

All other parameters should be set to circuit requirements, which are within the data sheet capabilities of the DRF1300. Throughput delays are not incorporated in this model.

DRF1400 SPICE Model for Non-Zero Reference Planes.

The DRF1400 series are half-bridge configurations of two power MOSFETs and two DRF100 drivers. Non-zero Reference Planes are defined as those Planes where node (0) is not 0V and may also be a time varying signal.

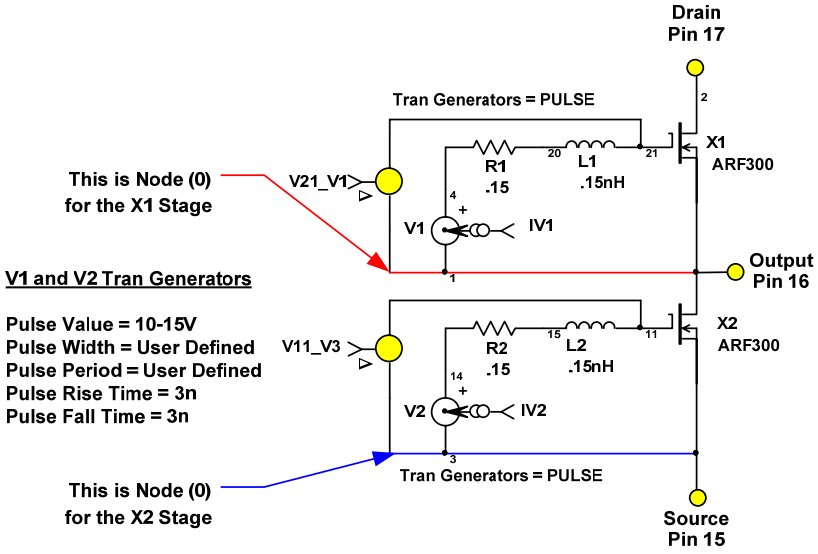

Figure 13 DRF1400

This Model should work with most SPICE platforms

The Model illustrated in Figure 13 will operate correctly for any signal type or value at node (0).

SPICE Files

These models were developed using Intusoft SPICE software, http://intusoft.com. All of the .lib files should work with any SPICE tool. The sub circuits and symbols may have to be recreated based on the simulation platform being used. These files are available on the Microsemi website.

MOSFET SPICE Models for Non-Zero Reference Planes

DRF Part Number	Output MOSFET	Configuration	Related Figure Number
DRF1200	ARF466	Single MOSFET die	See Figure 8
DRF1201	ARF467	Two die in parallel	See Figure 8
DRF1202	ARF300	Two die in parallel	See Figure 8
DRF1203	ARF467	Two die in parallel	See Figure 8
DRF1300	2 X ARF300	Two die in push-pull	See Figure 12
DRF1301	2 X ARF467	Two die in push-pull	See Figure 12
DRF1400	2 X ARF300	Two die in a half bridge	See Figure 13
DRF1401	2 X ARF467	Two die in a half bridge	See Figure 13
See Microsemi website for device SPICE models, .lib file			