GC4212-6LP

Datasheet

Control Devices–Surface Mount Input-Limiting Diode Element

Released

December 2017

Microsemi

Power Matters.™

Contents

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 was published in December 2017. It was the first publication of this document.

2 Product Overview

This SMT limiting diode element consists of a specially processed PIN diode packaged in a convenient, low-cost plastic outline suitable for standard or co-planar microstrip circuits. Featuring low loss, low turn-on, and high self-biased isolation, these devices are designed for use in passive or active limiters at frequencies through X band.

This surface-mount limiter meets RoHS requirements according to EU directives 2011/65/EC and 2002 /95 EC.

2.1 Applications

A diode limiter is a power-sensitive variable attenuator that uses the non-linear properties of the diode to provide an impedance mismatch when sufficient amounts of RF power are incident on the device. The output power is reduced to a level that will not overdrive a receiver, burn out a mixer, or otherwise compromise the device. For varying input power levels in excess of the diode's threshold level, the limiter's output power tends to remain constant.

A passive limiter is one in which the limiter diodes are turned on by the RF signal itself. An active limiter is one in which the limiter diodes are turned on primarily by an external bias current typically supplied by a Schottky detector diode that senses the incident signal.

Since limiter diodes are not designed to dissipate large amounts of power, the limiter must reflect or divert the excess incident power back to the source or to another load (through a circulator or a hybrid coupler, for example).

QFN limiting diode elements may be used in microstrip, co-planar microstrip, or other media. Single or cascaded devices may be used, depending on power levels.

2.2 Benefits

The CG4212-6LP device provides the following application benefits:

- Receiver protection circuits
- Amplifier protection

2.3 Key Features

The following are key features of the CG4212-6LP device:

- Small 1.6 mm × 1.6 mm QFN
- CG4212-6LP: Output PIN diode
- Low insertion loss: 0.2 dB at 3 GHz
- Multistage designs
  - GC4701-6LP: Input PIN diode
  - GC9952-6LP: Schottky driver
- Suitable for applications to 15 GHz
- Excellent flat leakage performance
- Moderate-P1dB compression point: 20 dBm
- RoHS compliant

3 Electrical Specifications

This section details the electrical specifications of the CG4212-6LP device.

3.1 Absolute Maximum Ratings

The following table shows the absolute maximum ratings of the CG4212-6LP device.

Table 1 • Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Maximum leakage current (at 80% of minimum-rated V_B)	I_R	500	nA
Operating temperature	T_{OP}	–55 to 150	°C
Storage temperature	T_{STG}	–65 to 150	°C
ESD sensitivity (HBM)		Class 1A	
Moisture sensitivity level		MSL 1	

3.2 Device Electrical Parameters

The following table shows the CG4212-6LP device electrical parameters at 25 °C.

Table 2 • Device Electrical Parameters

Parameter	Units	Condition	Min	Typ	Max
V_B	V	I_R = 10 µA	100	150	
I_R	nA	V_R = 80 V			500
V_F	V	I_F = 10 mA		0.95	1.2
C_T	pF	V_R = 0 V, f = 1 MHz		0.5	
C_T	pF	V_R = 10 V, f = 1 MHz		0.3	0.4
R_S	Ω	I_F = 10 mA, f = 1 GHz		1.0	1.5
T_L	ns	I_F = 10 mA, I_R = 6 mA		250	
Thermal resistance	°C/W	I heat = 0.5 A			50

3.3 Typical RF Performance

The following table shows the typical RF performance of the CG4212-6LP device at 25 °C.

Table 3 • Typical RF Performance

Parameter	Units	Condition	Min	Typ	Max
Peak power (P_{IN})	dBm	1 µs pulse width, 0.1% duty cycle			60
Leakage power (P_{OUT})	dBm	1 µs pulse width, 0.1% duty cycle		39	
Threshold	dBm	P1dB		20	
CW power (P_{IN})	dBm	Continuous			37

4 Small Signal Characteristics

The following graphs show the small signal characteristic curves of the CG4212-6LP device.

Figure 1 • GC4212-6LP Insertion Loss

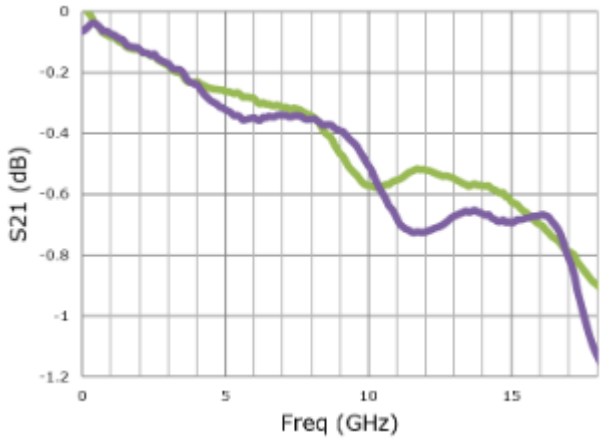


Figure 2 • GC4212-6LP Input Return Loss

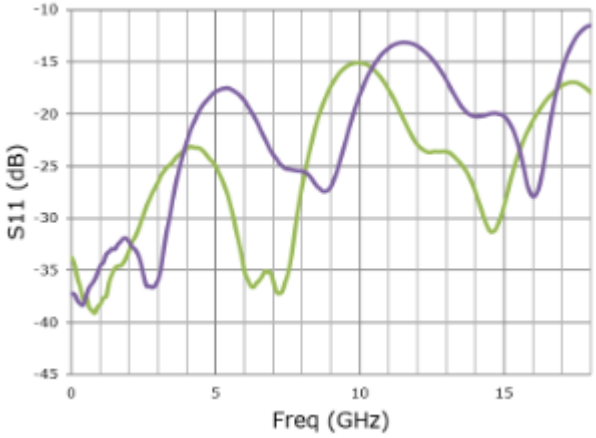


Figure 3 • GC4212-6LP/GC4701-6LP Insertion Loss

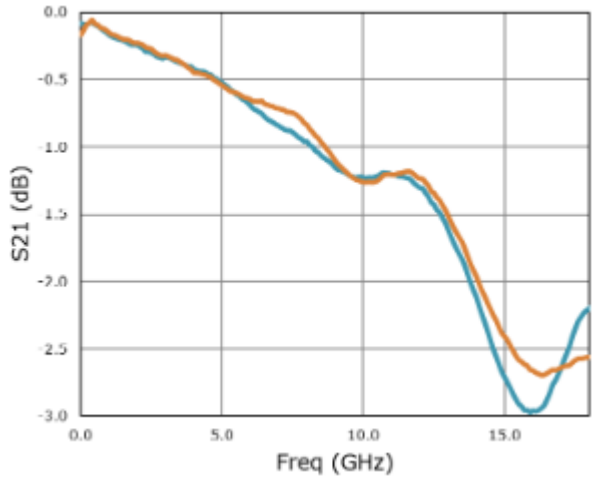


Figure 4 • GC4212-6LP/GC4701-6LP Input Return Loss

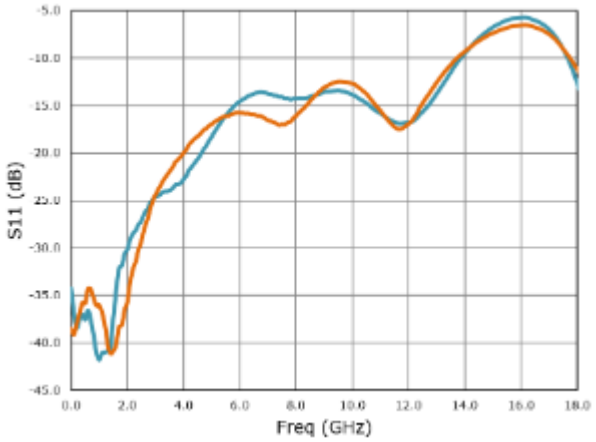


Figure 5 • GC4212-6LP/GC9952-6LP Insertion Loss

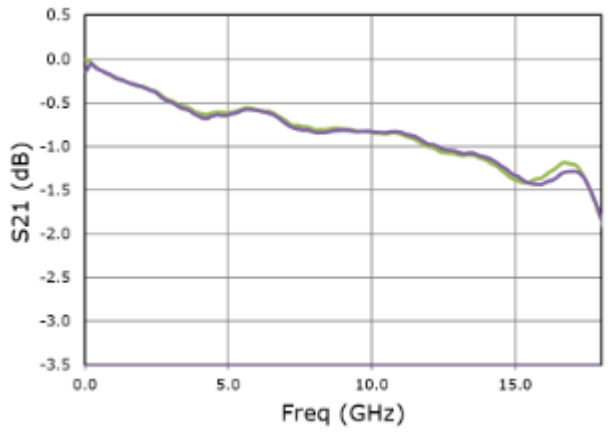


Figure 6 • GC4212-6LP/GC9952-6LP Input Return Loss

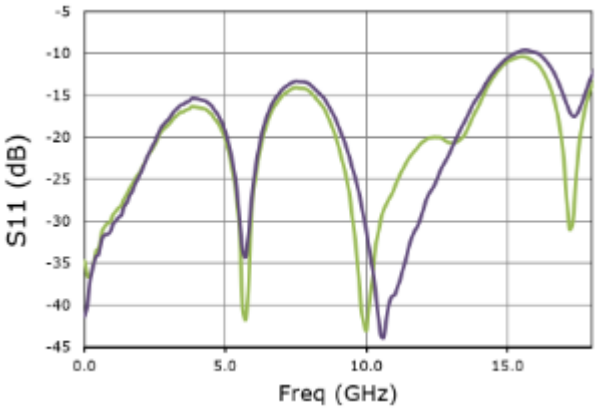


Figure 7 • GC4212-6LP/GC4701-6LP/GC9952-6LP Insertion Loss

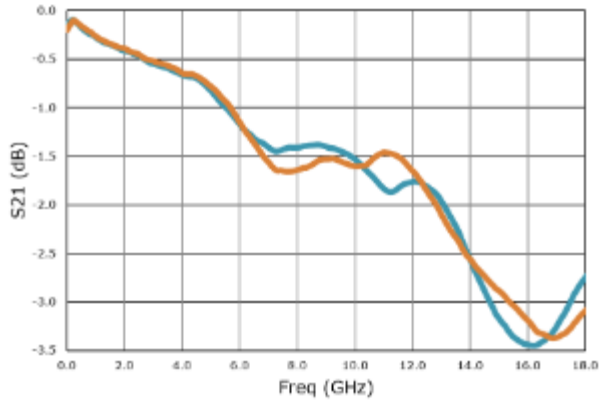
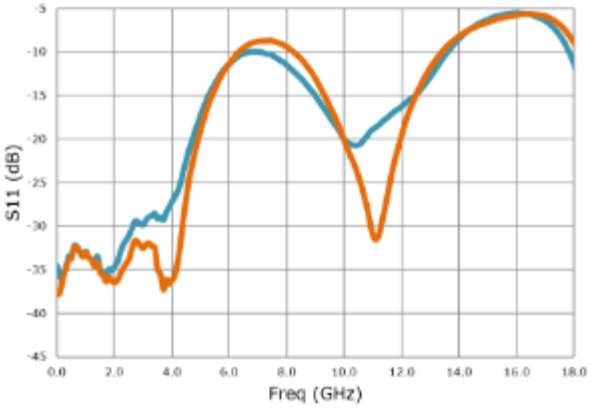


Figure 8 • GC4212-6LP/GC4701-6LP/GC9952-6LP Input Return Loss



5 Transfer Characteristics

The following graphs show the transfer characteristics of the CG4212-6LP device.

Figure 9 • CW Transfer Characteristics

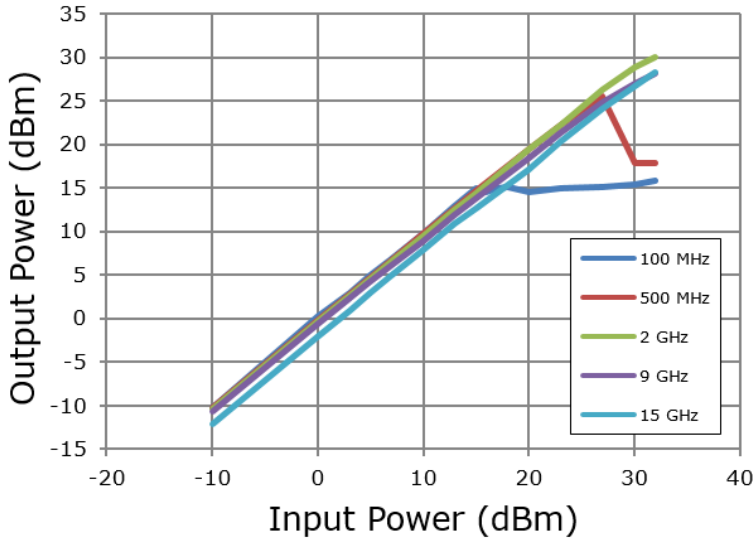
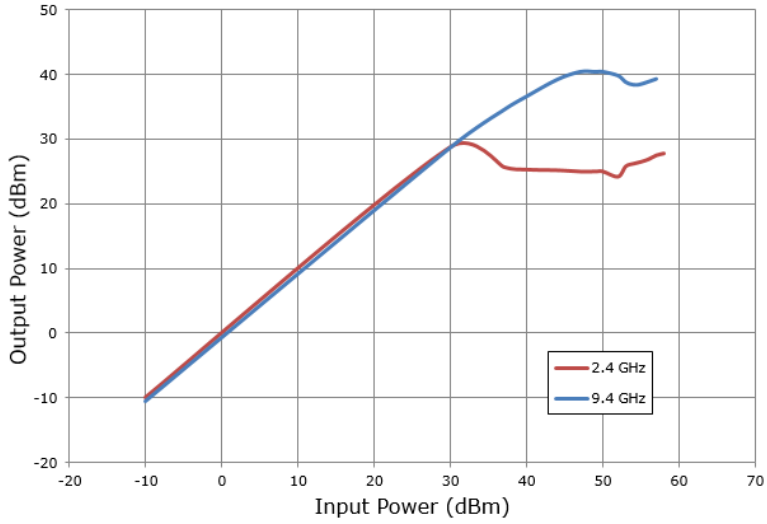


Figure 10 • Pulsed Power Transfer Characteristics (1 µs Pulse Width, 0.1% Duty Cycle)

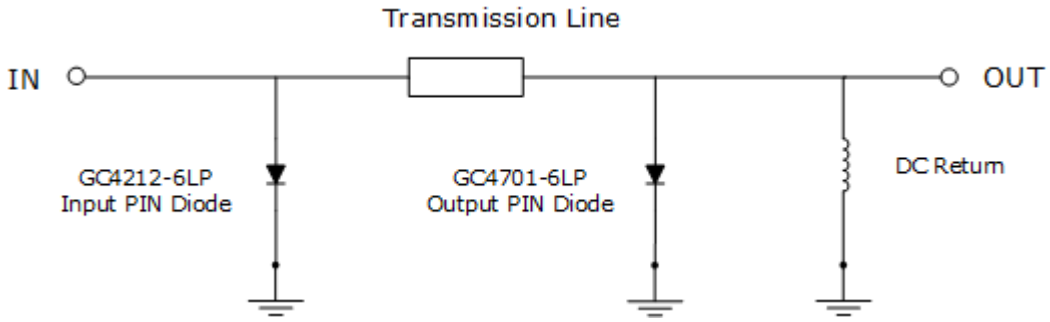


5.1 CW Multi-Stage Transfer Characteristics

This section details the CW multi-stage transfer characteristics of the CG4212-6LP device.

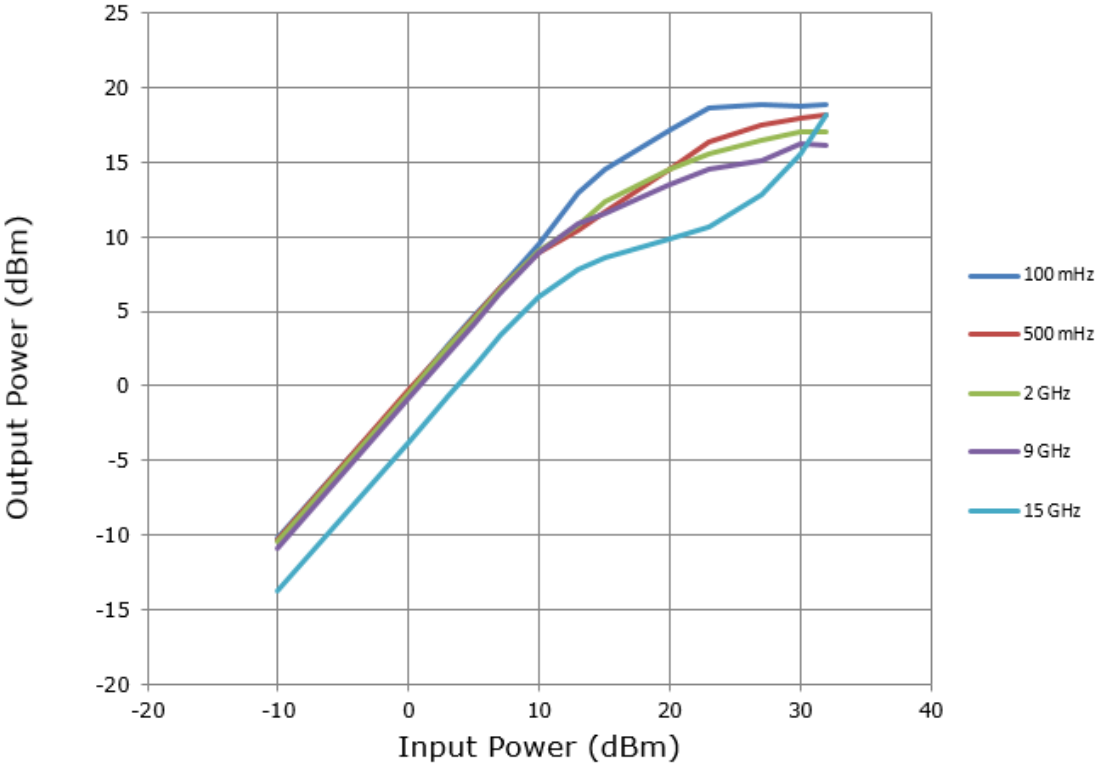
The following drawing shows the typical circuit layout of a two-stage limiter design utilizing the GC4212-6LP as the input stage and the GC4701-6LP as the output stage. An inductor element is included as a DC ground return.

Figure 11 • Two-Stage Limiter Circuit Layout



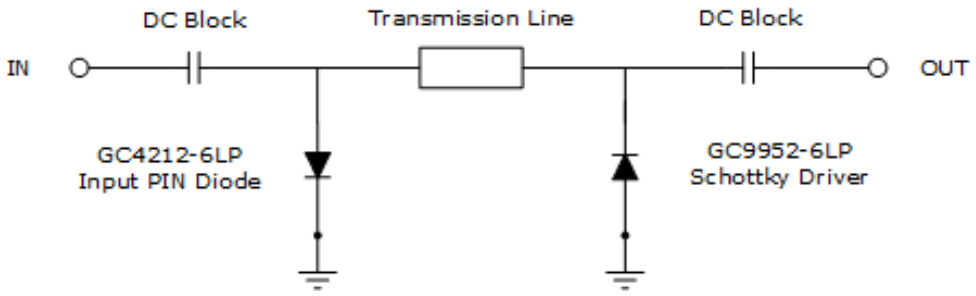
The following graph shows the CW multi-stage transfer characteristics of the GC4212-6LP and GC4701-6LP devices.

Figure 12 • GC4212-6LP and GC4701-6LP CW CW Multi-Stage Transfer Characteristics



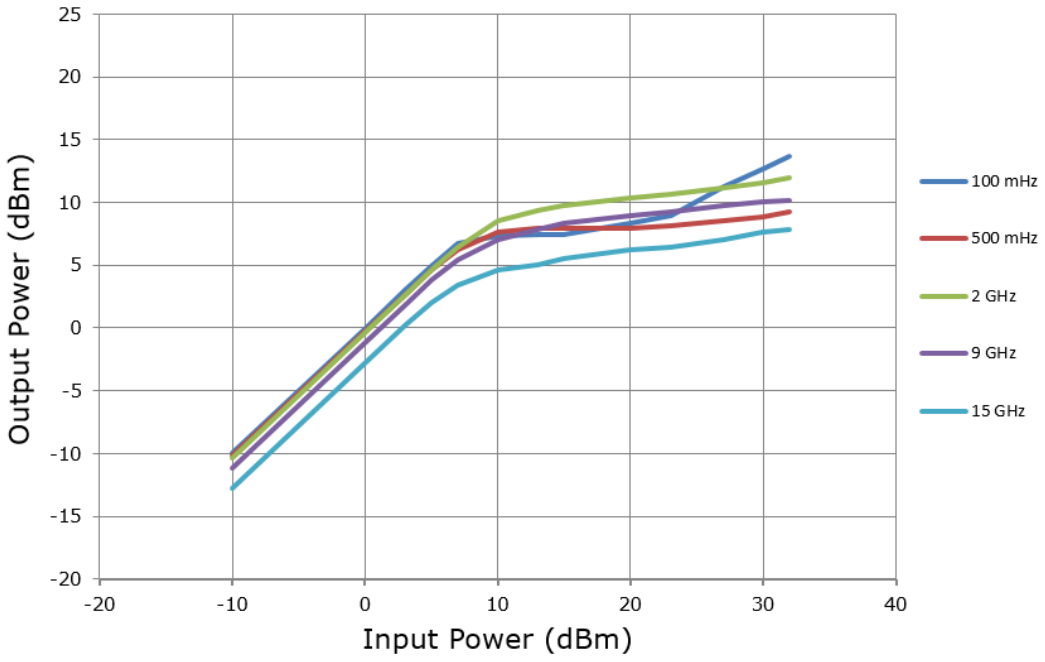
The following drawing shows the typical circuit layout of a two-stage limiter design utilizing the GC4212-6LP as the input stage and the GC9952-6LP as the Schottky driver. DC blocks are required with this design.

Figure 13 • Two-Stage Limiter Circuit Layout with Schottky Driver



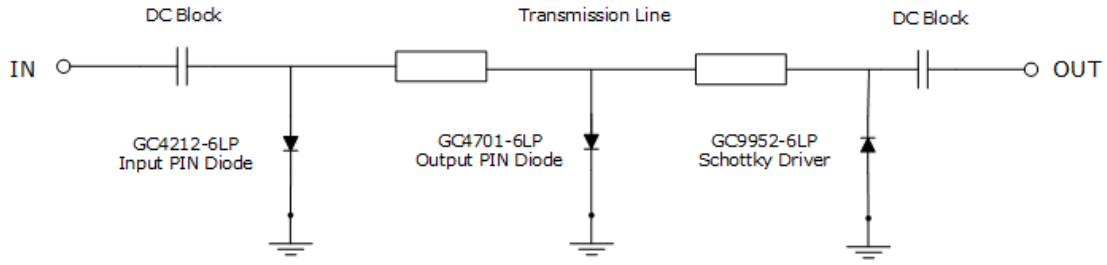
The following graph shows the CW multi-stage transfer characteristics of the GC4212-6LP and GC9952-6LP devices.

Figure 14 • GC4212-6LP and GC9952-6LP CW Multi-Stage Transfer Characteristics



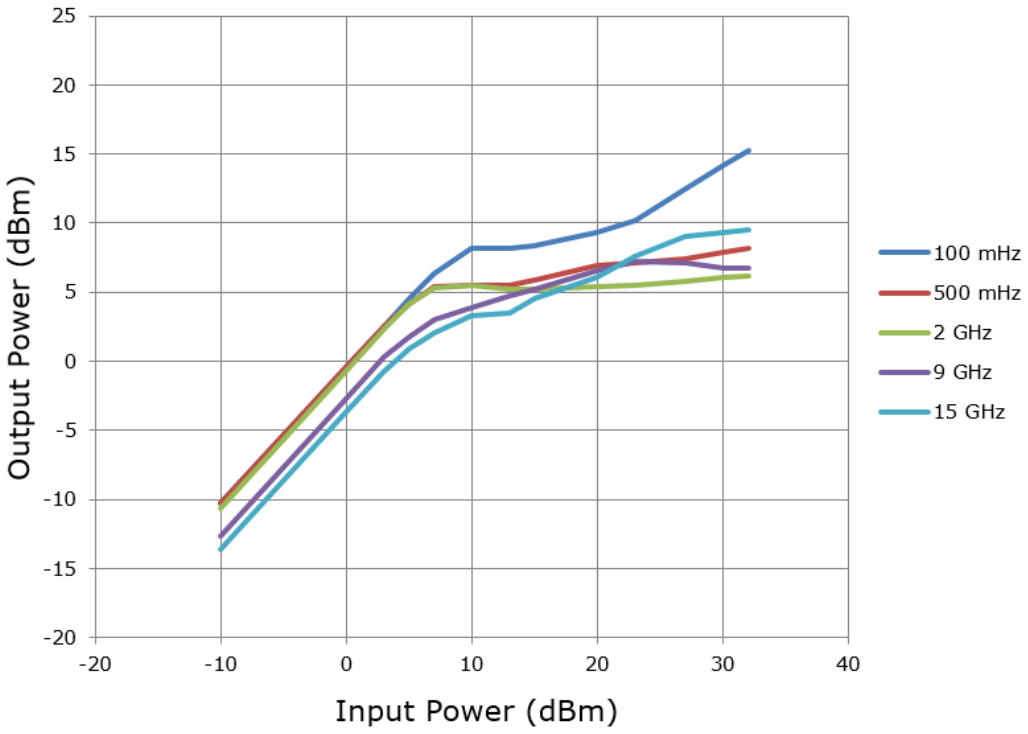
The following drawing shows the typical circuit layout of a three-stage limiter design utilizing the GC4212-6LP input PIN, the GC4701-6LP output PIN, and the GC9952-6LP as the Schottky driver. DC blocks are required with this design.

Figure 15 • Three-Stage Limiter Circuit Layout



The following graph shows the CW multi-stage transfer characteristics of the GC4212-6LP, GC4701-6LP, and GC9952-6LP devices.

Figure 16 • GC4212-6LP, GC4701-6LP, and GC9952-6LP CW Multi-Stage Transfer Characteristics

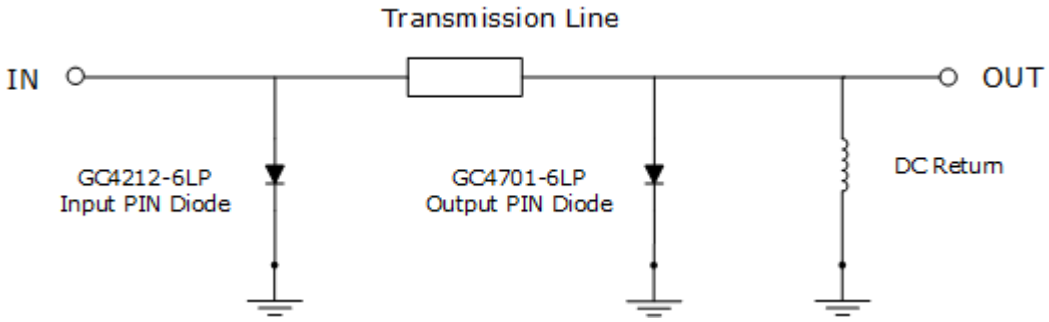


5.2 Pulsed Multi-Stage Transfer Characteristics

This section details the pulsed multi-stage transfer characteristics of the CG4212-6LP device (at 1 µs pulse width, 0.1% duty cycle).

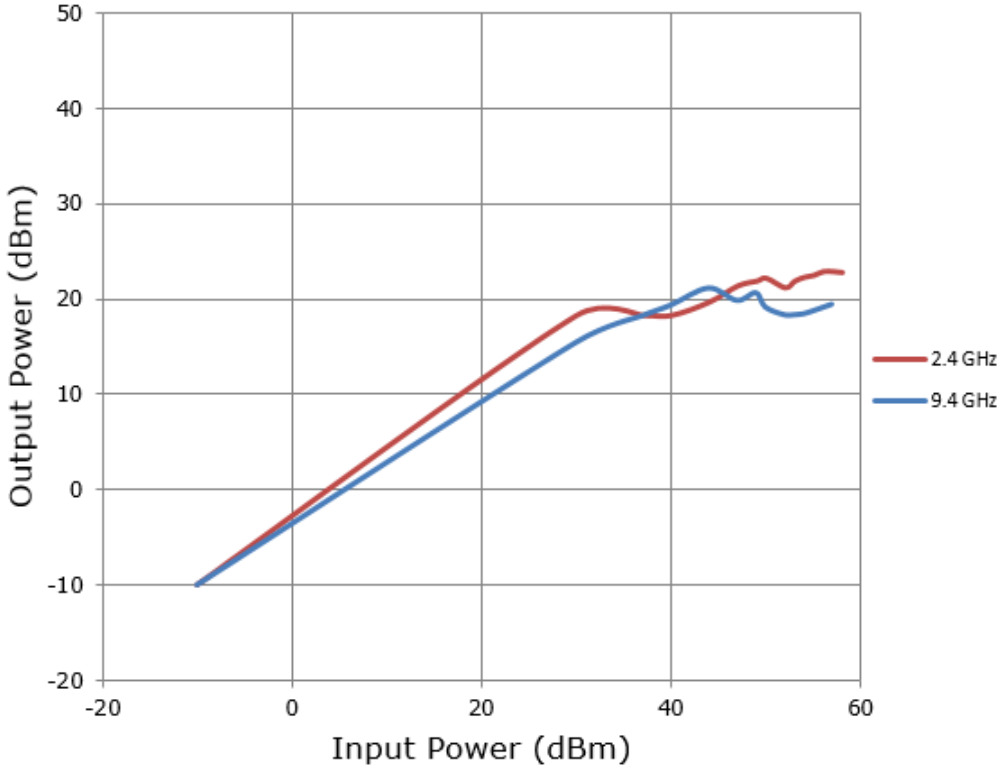
The following drawing shows the typical circuit layout of a two-stage limiter design utilizing the GC4212-6LP as the input stage and the GC4701-6LP as the output stage. An inductor element is included as a DC ground return.

Figure 17 • Two-Stage Limiter Circuit Layout



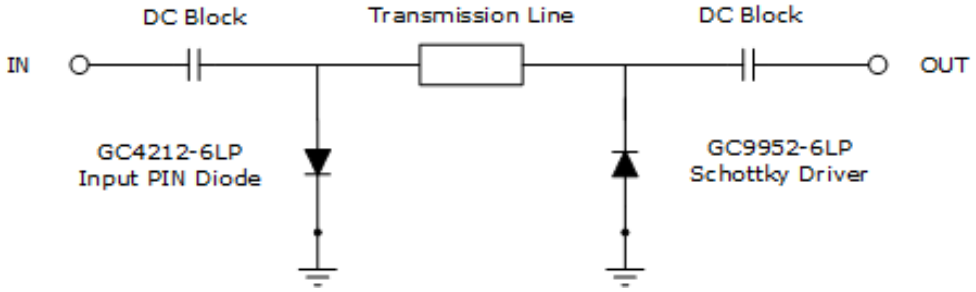
The following graph shows the pulsed multi-stage transfer characteristics of the CG4212-6LP and CG4701-6LP devices.

Figure 18 • CG4212-6LP and CG4701-6LP Pulsed Transfer Characteristics



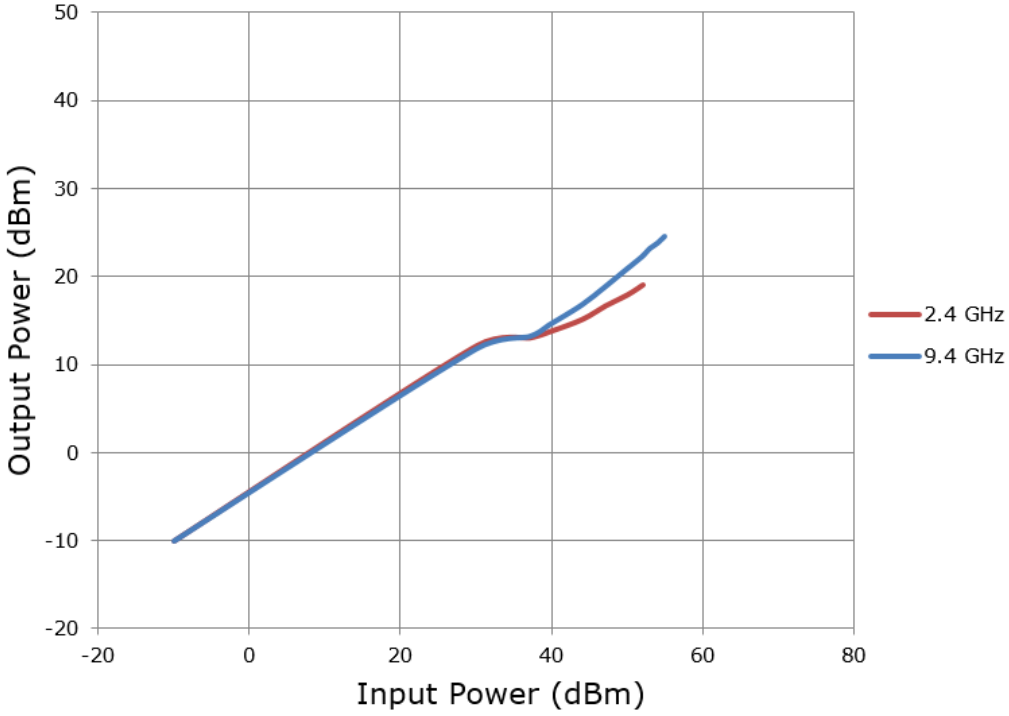
The following drawing shows the typical circuit layout of a two-stage limiter design utilizing the GC4212-6LP as the input stage and the GC9952-6LP as the Schottky driver. DC blocks are required with this design.

Figure 19 • Two-Stage Limiter Circuit Layout with Schottky Driver



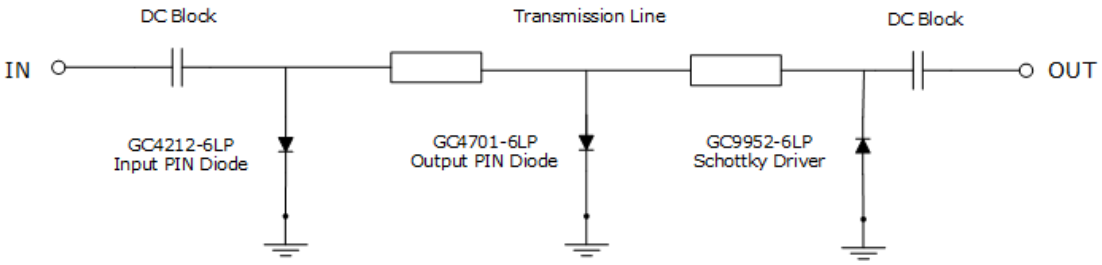
The following graph shows the CW multi-stage transfer characteristics of the CG4212-6LP and CG9952-6LP devices.

Figure 20 • CG4212-6LP and CG9952-6LP Pulsed Transfer Characteristics



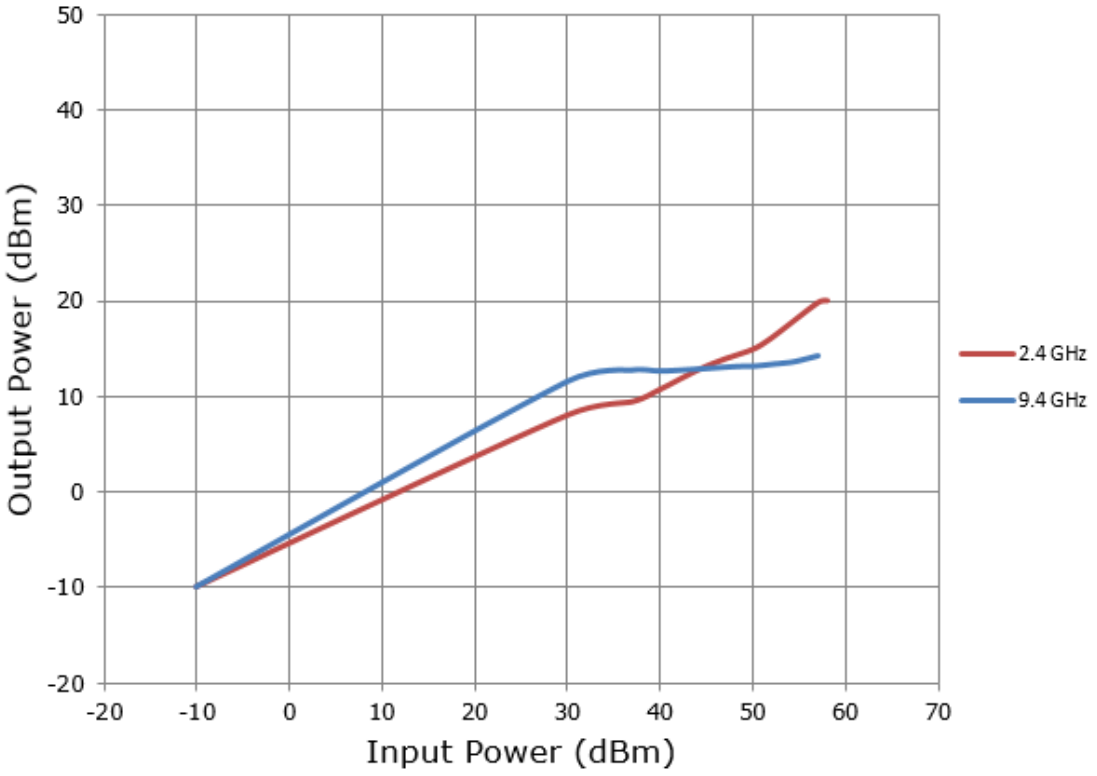
The following drawing shows the typical circuit layout of a three-stage limiter design utilizing the GC4212-6LP input PIN, the GC4701-6LP output PIN, and the GC9952-6LP as the Schottky driver. DC blocks are required with this design.

Figure 21 • Three-Stage Limiter Circuit Layout



The following graph shows the CW multi-stage transfer characteristics GC4212-6LP, GC4701-6LP, and GC9952-6LP devices.

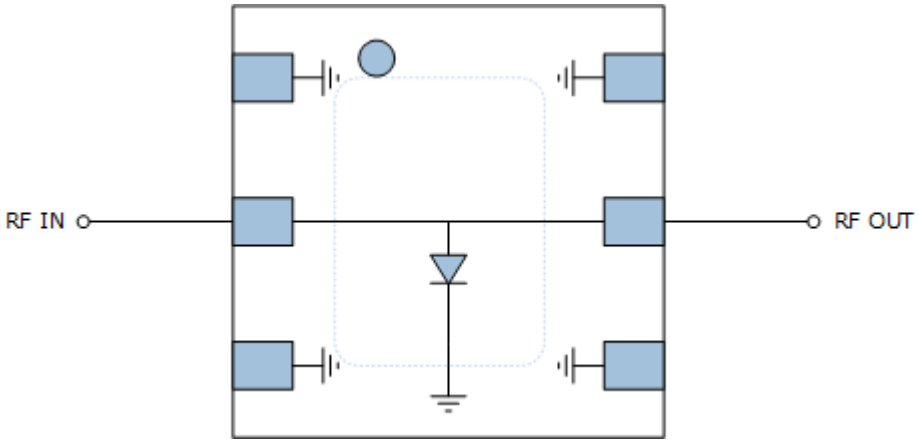
Figure 22 • GC4212-6LP, GC4701-6LP, and GC9952-6LP Pulsed Transfer Characteristics



6 Application Schematic and Recommended Board Layout

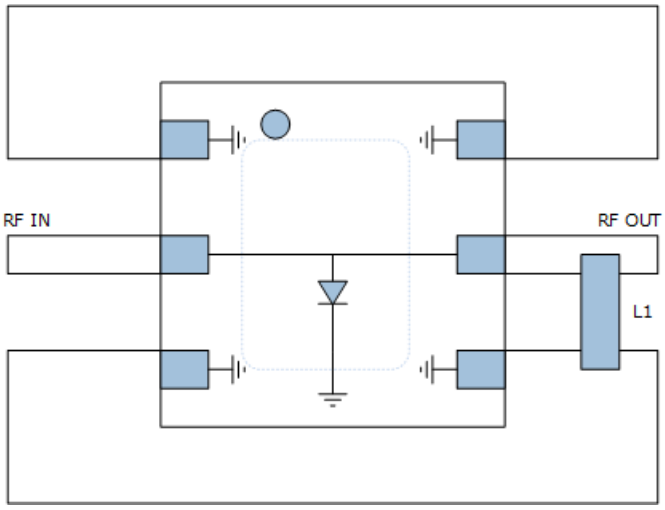
The following drawing shows the application schematic of the CG4212-6LP device.

Figure 23 • Application Schematic



The following drawing shows the recommended board layout of the CG4212-6LP device.

Figure 24 • Recommended Board Layout



The following table shows the L1 values in nH at different bandwidths.

Table 4 • L1 Values

Band Width (GHz)	L1 (nH)
1–2	40–50
2–4	20–25
4–8	10–20
8–15	8–12
1–12	40–50

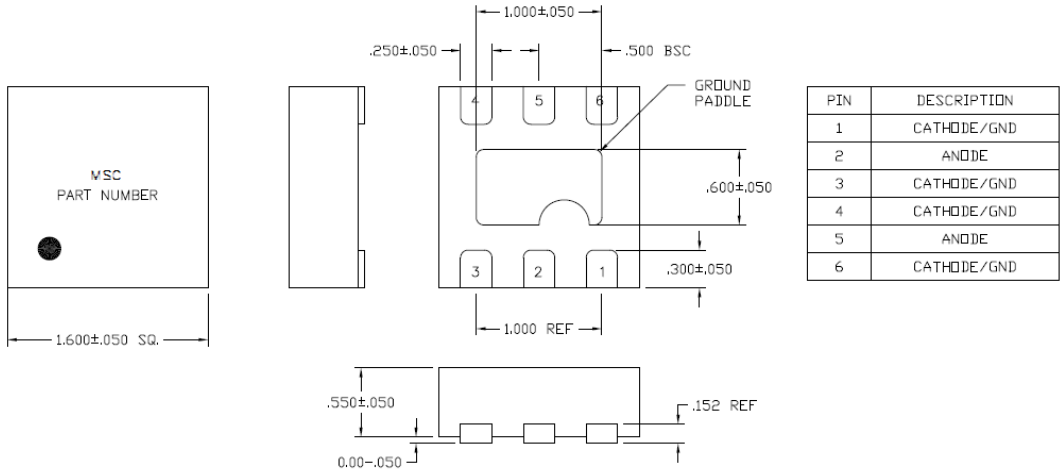
7 Package Specifications

This section details the package specifications of the CG4212-6LP device.

7.1 Package Dimensions

The following illustration shows the package outline of the CG4212-6LP device. Dimensions are in millimeters [inches].

Figure 25 • Package Dimensions

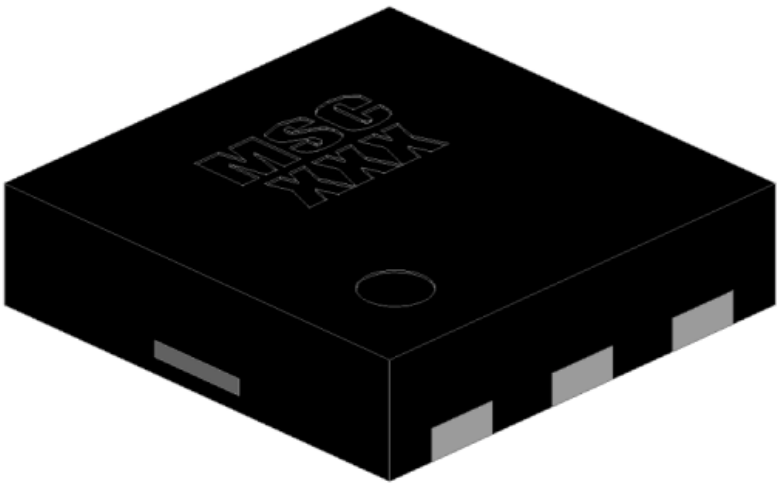


PIN	DESCRIPTION
1	CATHODE/GND
2	ANODE
3	CATHODE/GND
4	CATHODE/GND
5	ANODE
6	CATHODE/GND

7.2 Package Outline

The following illustration shows the package outline of the CG4212-6LP device. For additional packaging information, contact your Microsemi sales representative.

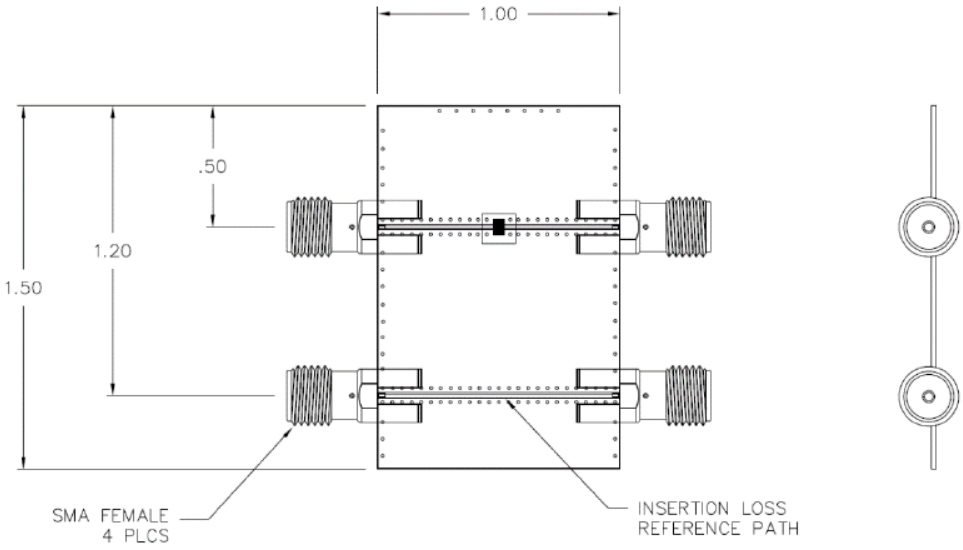
Figure 26 • Package Outline

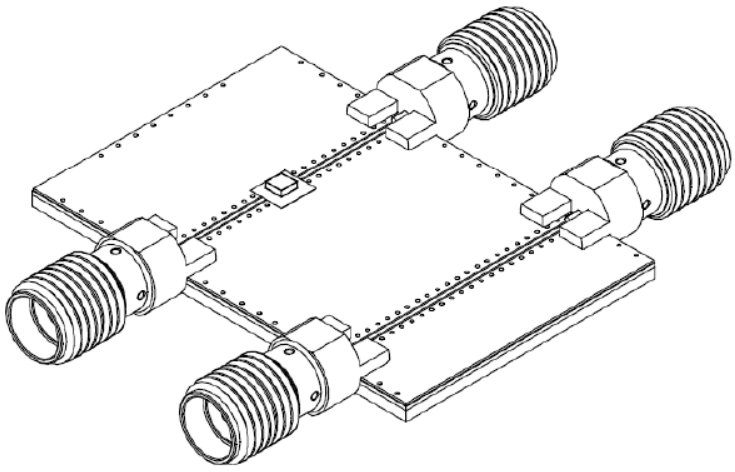


8 Evaluation Board Assembly

The following illustrations show the evaluation board assembly of the CG4212-6LP device (ordering part number: MSTF0012). The board material is 0.016 Rogers 4003, 0.5 oz. copper cladding on both sides (starting thickness). It has a full-metal backside and an electroless nickel immersion gold (ENIG) finish on both sides. Solder mask is applied to the topside only. Units are in inches.

Figure 27 • Evaluation Board Assembly

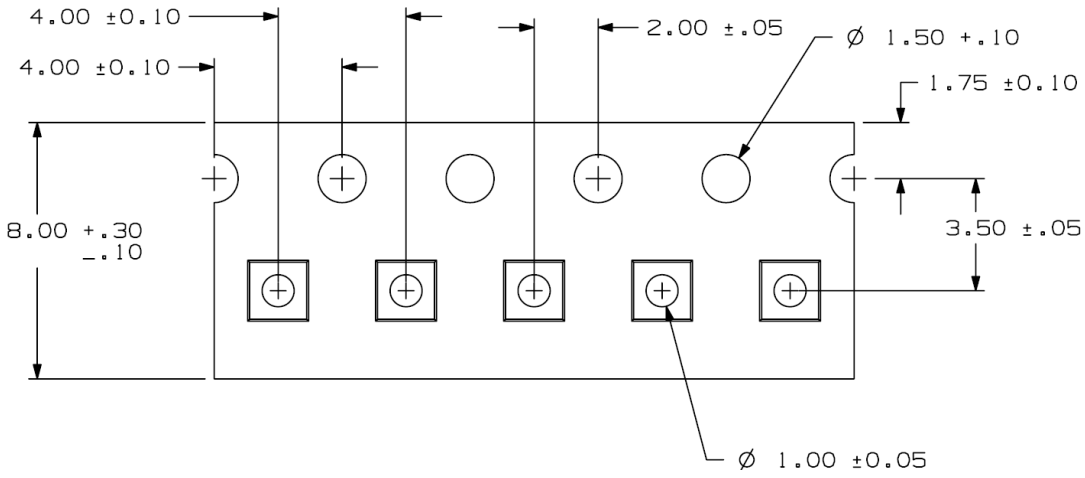




9 Tape-and-Reel Format

The following illustration shows the tape-and-reel format of the CG4212-6LP device.

Figure 28 • Tape-and-Reel Format



10 Ordering Information

The following table shows the ordering information for the CG4212-6LP device.

Table 5 • Ordering Information

Part Number	Package
GC4212	6LP 1.6 × 1.6 QFN

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
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