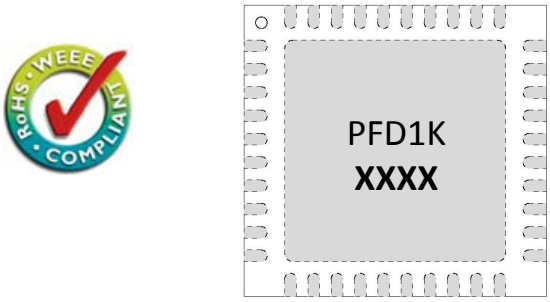
8 GHz Phase Frequency Detector IC with Dual 40 GHz Prescalers

Features

- Product Highlights
- 40 GHz Maximum Frequency
- 1-127 Variable Modulus Prescalers
- DC-8GHz Phase Detector Operation
- Single +3.3V Supply
- Single-Ended or Differential inputs and outputs
- Charge Pump digital control
- Charge Pump invert pin
- 6x6 Ceramic Leadless QFN
- Low Power Dissipation



Application

The PFD1K can be used as a general purpose phase frequency detector with integrated prescalers. It is ideally suited to phase locked loop applications. The prescalers can be programmed at a rate greater than 100MHz, which makes it an excellent choice for fractional-N digital frequency synthesizers.

Pad Metallization

The QFN package pad metallization consists of a 500-1000 micro-inch Sn63 automated solder dip process.

Description

The PFD1K is a high frequency phase frequency detector with fully differential inputs and outputs. It features dual 7 bit programmable high speed prescalers which allow the PFD1K to operate up to 40 GHz for the reference and voltage controlled oscillator input frequency. The 8 GHz phase-frequency detector allows operation at higher reference frequencies with concurrent lower phase noise and PLL figure of merit. The PFD1K operates with a single positive or negative 3.3V supply, and is packaged in a 40-pin, 6mm x 6mm ceramic leadless surface mount package.

Key Specifications (T = 25˚C):
Vcc=+3.3V, Zo=50Ω

Parameter	Description	Min	Typ	Max
Fref (GHz)	Input Reference Frequency[1]	0.01	-	40
Fvco (GHz)	Input VCO Frequency[1]	0.01	-	40
Pref (dBm)	Input Reference Power[2]	-10	0	+10
Pvco (dBm)	Input VCO Power[2]	-10	0	+10
Vout (mVp-p)	Differential Charge Pump Output[3]	-	400	-
PDC (mW)	DC Power Dissipation	-	1320	-
$\mathcal{L}$ (dBc/Hz)	SSB Phase Noise[4]	-	-153	-

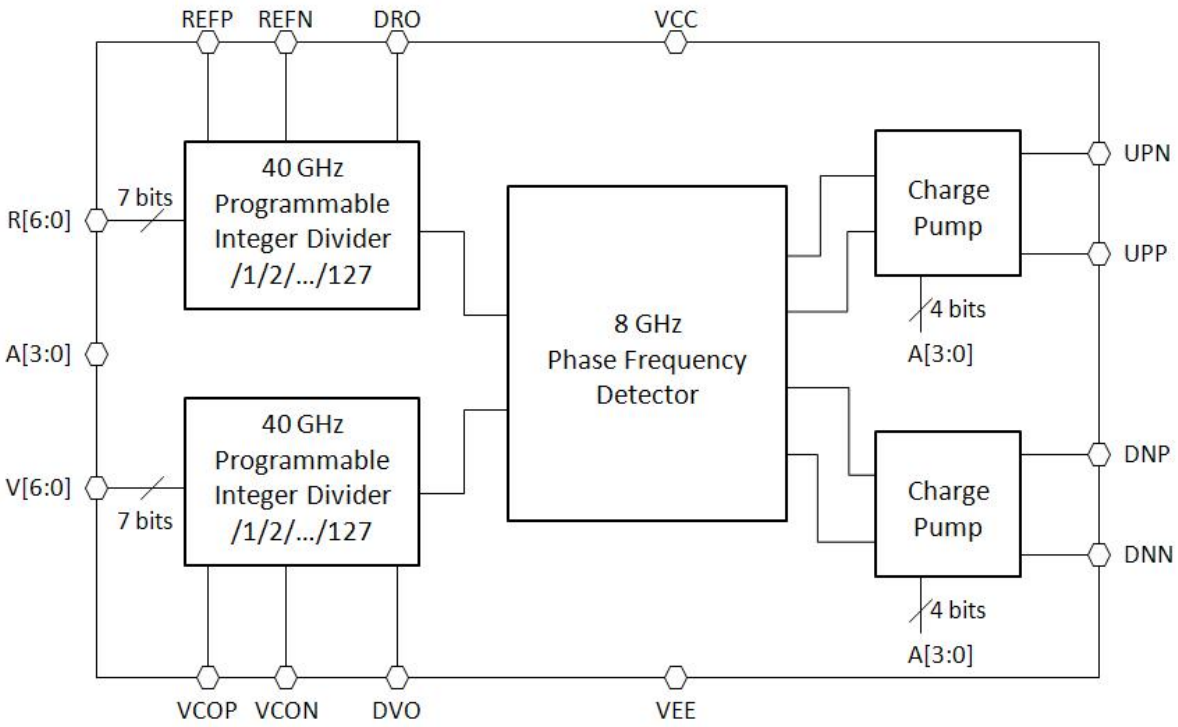
[1] Minimum input frequency values assume sine wave input and divide ratio set to 1.
[2] Input frequency=20 GHz
[3] Each side terminated into 50Ω
[4] 900 MHz PFD input; 10 KHz offset

Supplemental Characteristics (@ 25˚C):
Vcc=+3.3V, Pin = 0 dBm, Zo=50Ω

Parameter	Description	Min	Typ	Max
Vdro (mVp-p)	Reference Prescaler Output[1]	450	475	500
Vdvo (mVp-p)	VCO Prescaler Output[1]	450	475	500

[1] Measured over several frequencies and divide ratios.

Theory of Operation



Functional Block Diagram

Overview:

The functional block diagram for the PFD1K is shown above. It contains two parallel programmable prescalers which frequency divide the reference and VCO inputs to the phase frequency detector. Reference input divide ratio R is determined as follows:

$$R = R6 * 26 + R5 * 25 + R4 * 24 + R3 * 23 + R2 * 22 + R1 * 21 + R0 * 20$$

where R6 thru R0 have values of 0 or 1. (All bits set to 0 results in a divide ratio of 1). Similarly, the divide ratio for the VCO input is set by V6 thru V0.

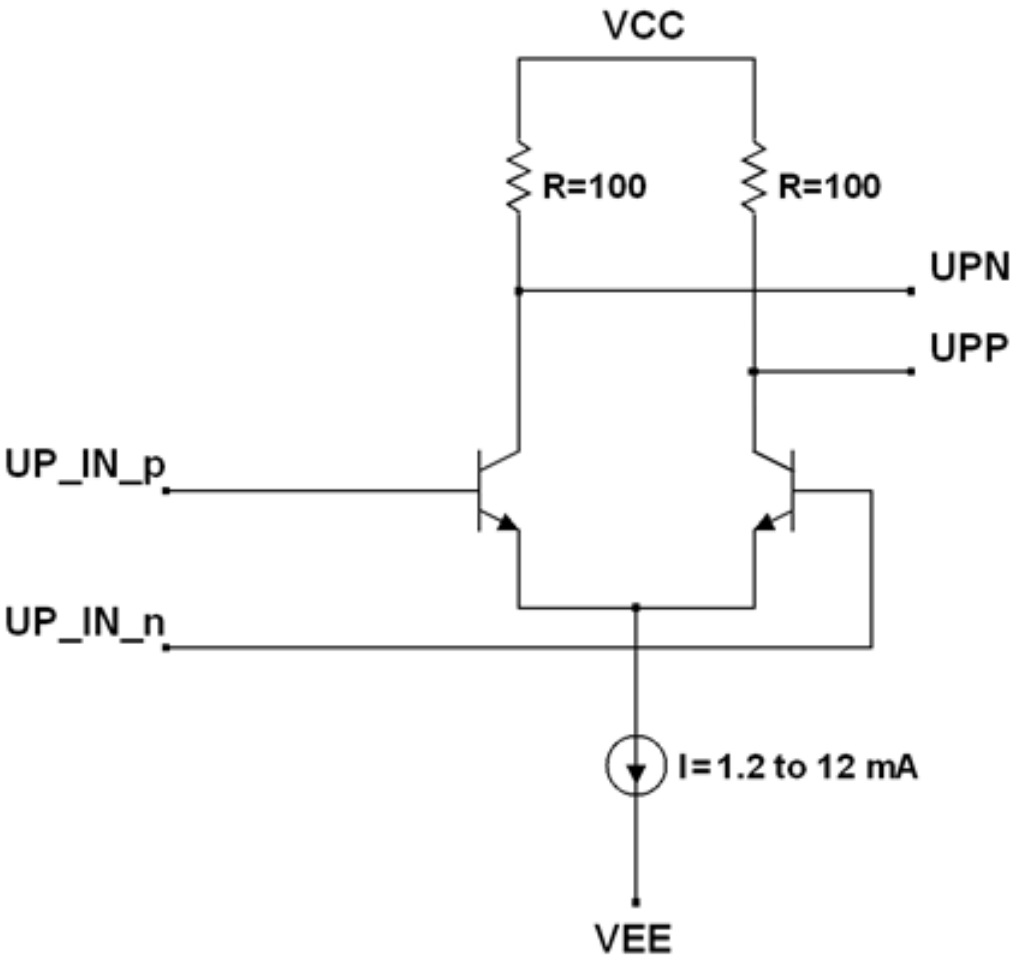
The core phase frequency detector can be operated up to a reference frequency of 8 GHz. The output of the phase frequency detector drives two programmable charge pumps. The amplitudes of the UP and Down pulses from the charge pumps can be controlled digitally by setting A[3:0]. There is also an analog adjustment at the VADJ* pin.

The divided reference and VCO signals may be monitored at the DRO and DVO outputs respectively. Analog adjustments, VADV* and VADR* can be used to control the amplitudes of DVO and DRO, or to disable DVO and DRO in order to reduce power consumption. With the exception of DRO and DVO, all of the RF inputs and outputs of the PFD1K are fully differential CML compatible levels so that they are easy to interface with other logic.

** VADJ, VADV and VADR are not shown in the block diagram.*

Charge Pump Control:

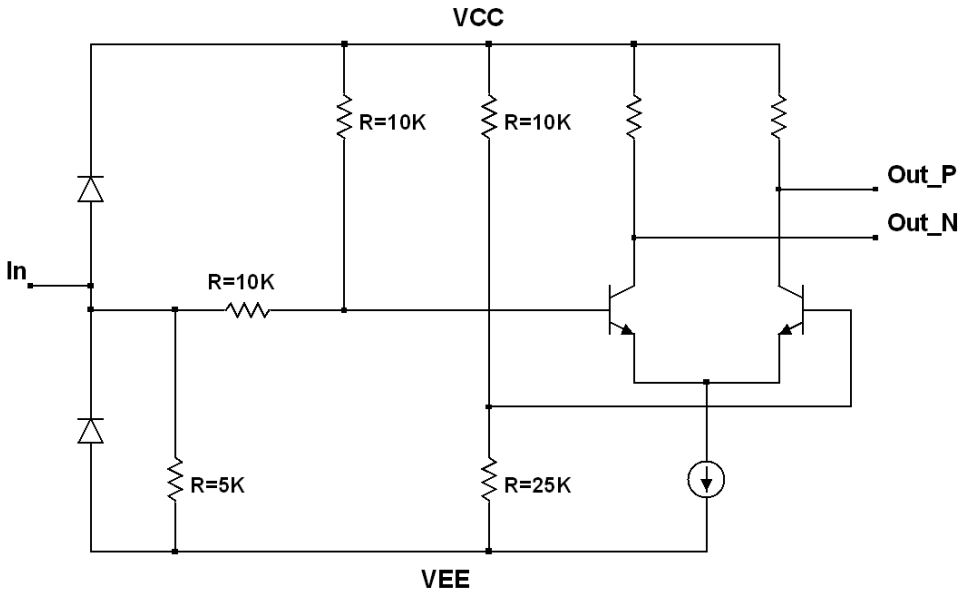
The PFD1K charge pump outputs are differential CML outputs with 100 ohm terminations. With this design the charge pump pulse width can be as small as 100 ps. The charge pump output pulses are digitally programmable with a 4 bit parallel interface. The maximum current output of the charge pump is 12 mA which will produce a pulse of 1200 mVpp into the internal 100 ohm termination resistor. When the charge pump outputs are terminated with a 50ohm load the parallel impedance of 100 ohms and 50 ohms results in a 33 ohm load, which reduces the output to 400mVpp. In addition to the digital control, there is an analog charge pump control voltage, VADJ, which can be used for fine control of the charge pump current. The maximum charge pump output of 12mA occurs when VADJ is set to VCC (which is the normal mode of operation). Logic 1 on the POL control input reverses the polarity of the charge pump outputs.



Simplified Charge Pump Output Circuit

Control Logic Circuitry:

The same circuitry is used for all control lines: A[0:3], R[0:6], V[0:6] and POL. A control pin left open defaults to logic 0.



Simplified Control Logic Input

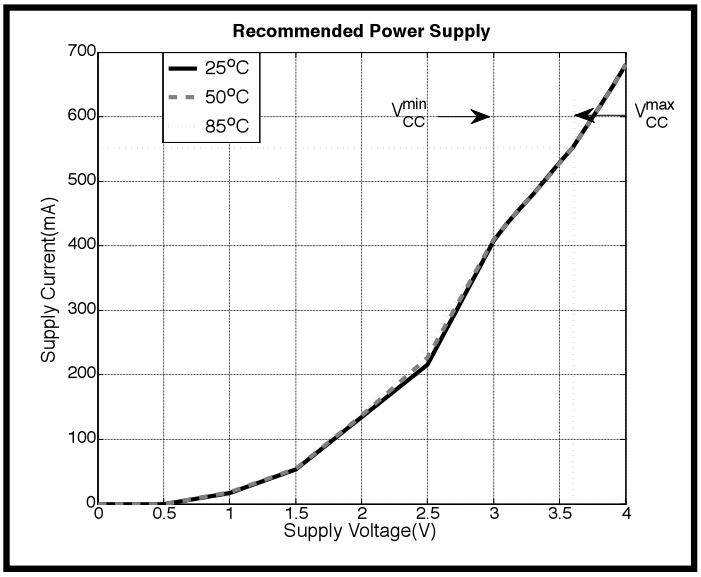
Table 1: Control Voltages (LVTTL Compatible)

Logic Level	Minimum	Typical	Maximum
1 (High)	VCC-1.3 V	VCC	VCC
0 (Low)	VEE	VEE	VEE+0.8 V

Analog Amplitude Controls:

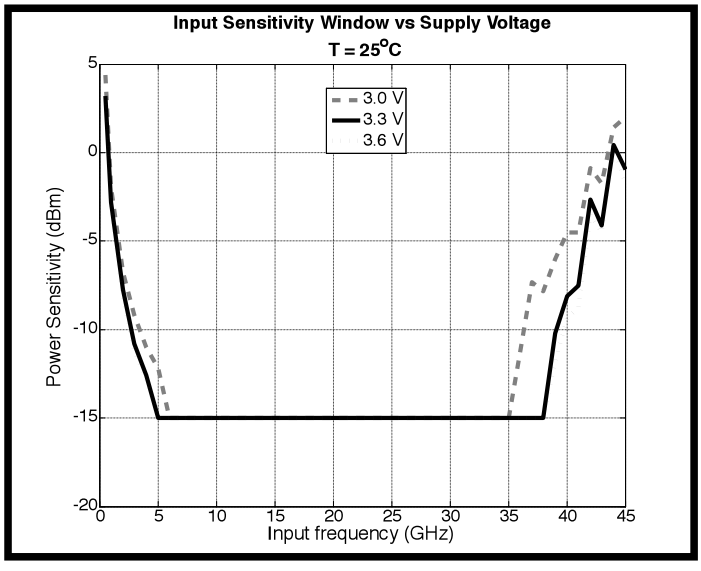
As was previously mentioned, VADJ can be used for fine tuning the charge pump current. Maximum current is achieved by setting VADJ to VCC. Similarly, the amplitudes of the prescaler outputs at DRO and DVO can be controlled with analog voltages VADR and VADV, respectively. As with VADJ, setting VADR and VADV to VCC results in maximum output amplitude.

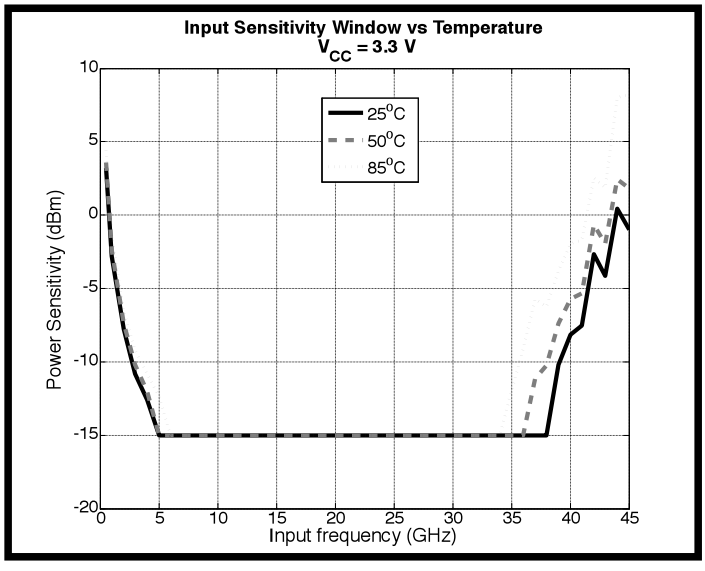
Power Supply Current



Power Supply Current

Prescaler Characteristics

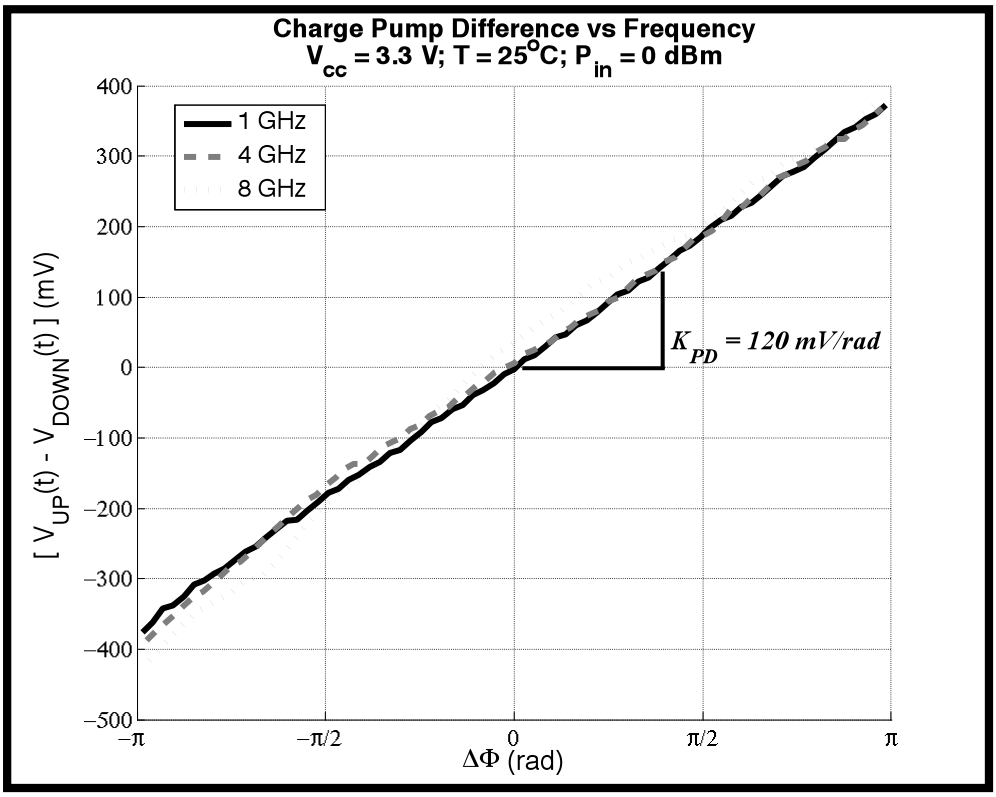


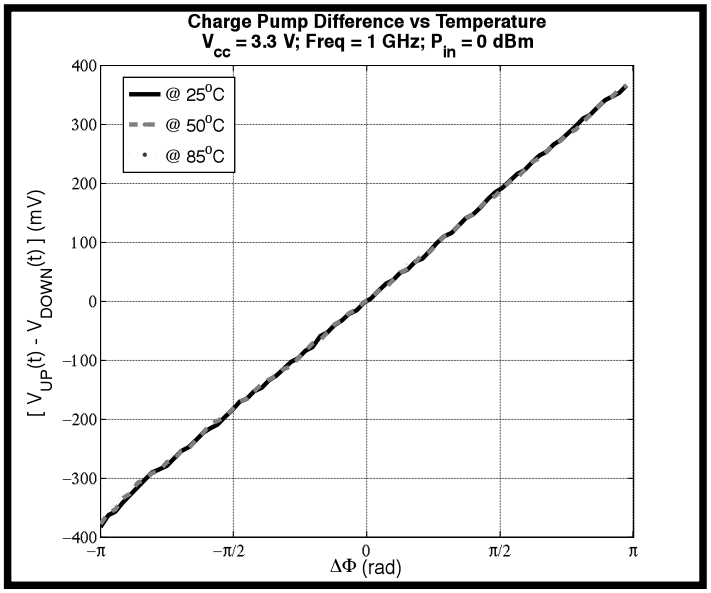


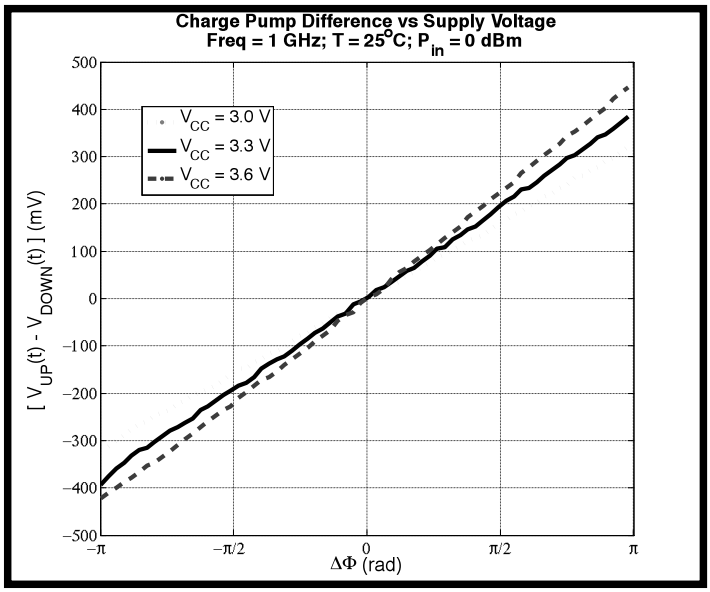
Prescaler Input Sensitivity

Phase Detector Characteristics

Divide Ratios: R = V = 1



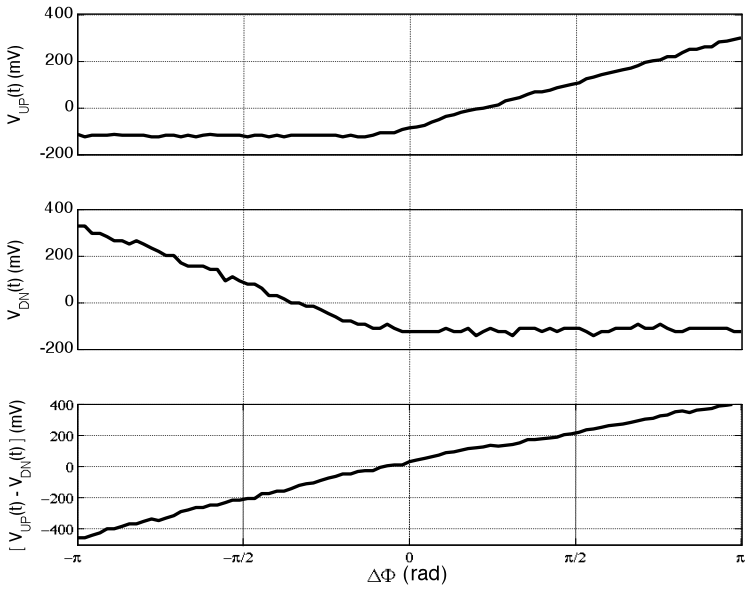




Phase Detector Characteristics

REF leads VCO

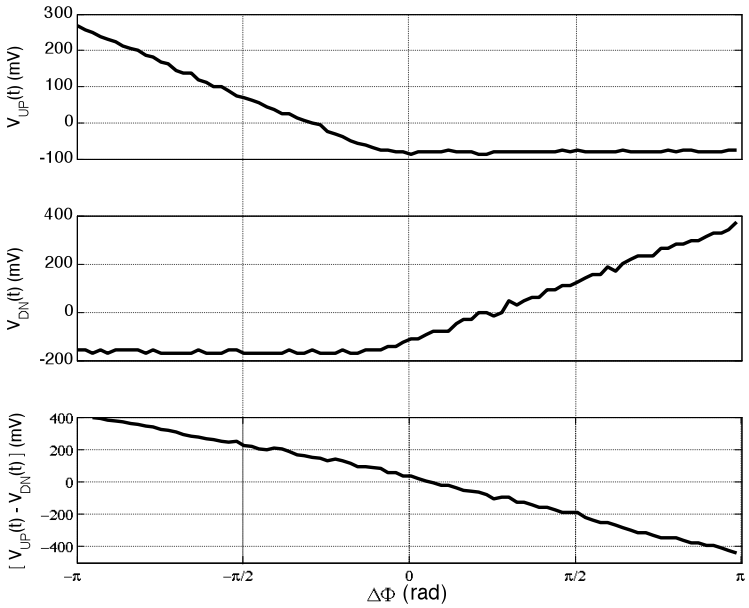
$f_{REF} > f_{VCO}$; f_{REF} = 5 GHz; V_{CC} = 3.3 V; T = 25oC; P_{in} = 0 dBm; POL = open



Charge pump outputs for REF leading VCO

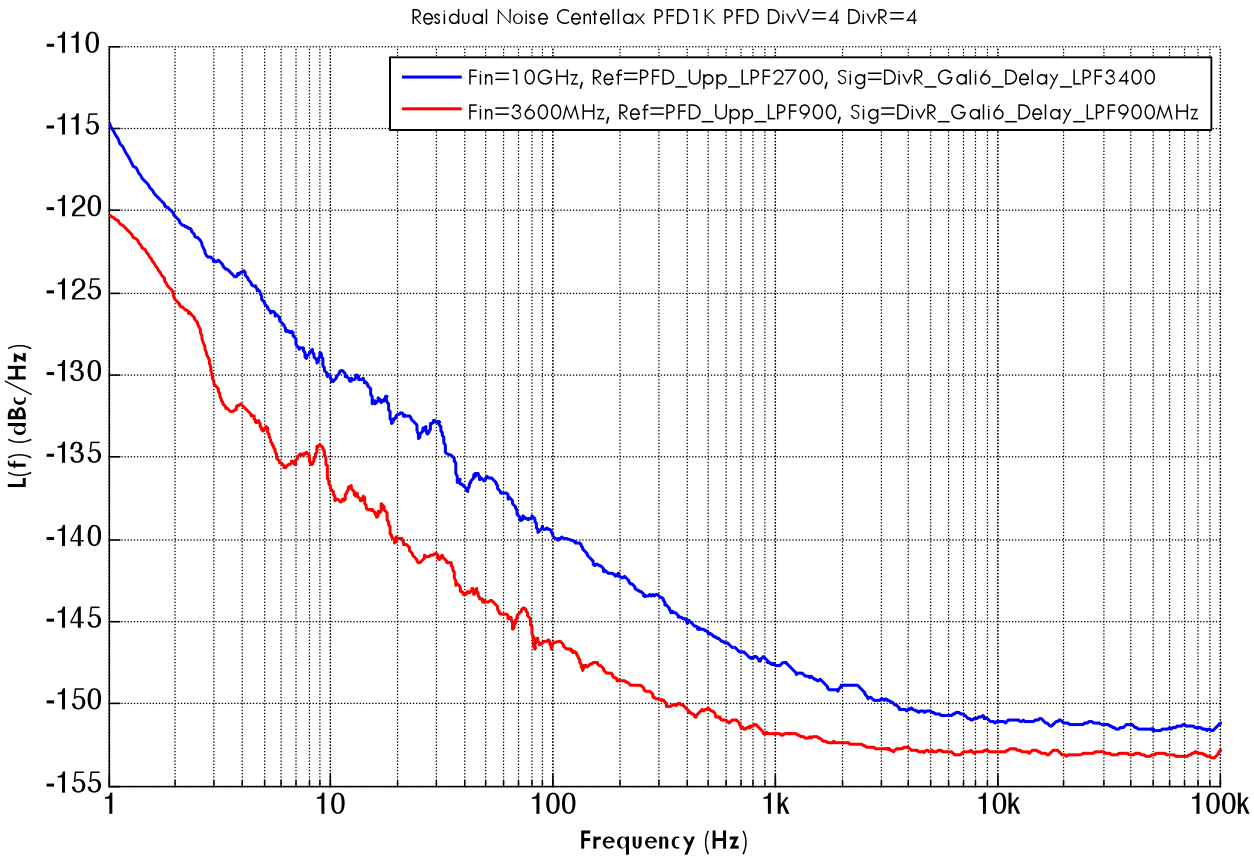
REF lags VCO

$f_{VCO} > f_{REF}$; f_{REF} = 5 GHz; V_{CC} = 3.3 V; T = 25oC; P_{in} = 0 dBm; POL = open



Charge pump outputs for REF lagging VCO

SSB Phase Noise Performance



SSB Phase Noise Performance

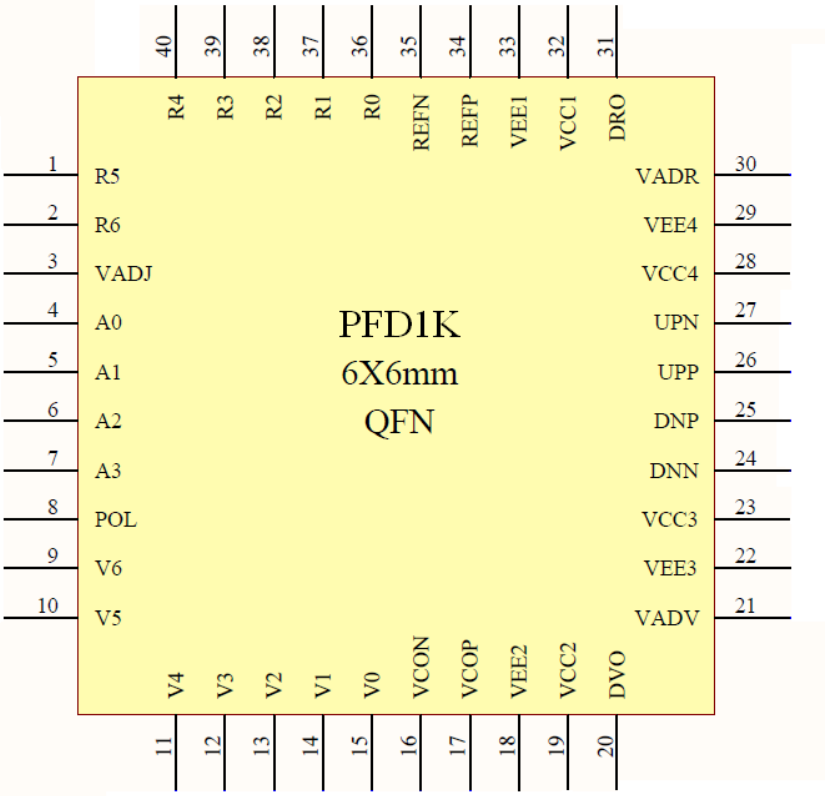
Table 2: RF Pin Description

Port Name	Description	Notes
REFP	Reference RF input, positive terminal	CML signal levels
REFN	Reference RF input, negative terminal	CML signal levels
VCOP	VCO RF input, positive terminal	CML signal levels
VCON	VCO RF input, negative terminal	CML signal levels
UPP	Up Charge Pump output, positive terminal	CML output level set by charge pump gain
UPN	Up Charge Pump output, negative terminal	CML output level set by charge pump gain
DNP	Down Charge Pump output, positive terminal	CML output level set by charge pump gain
DNN	Down Charge Pump output, negative terminal	CML output level set by charge pump gain
DRO	Divided Reference Output (single ended)	CML output level, requires DC pullup
DVO	Divided VCO Output (single ended)	CML output level, requires DC pullup

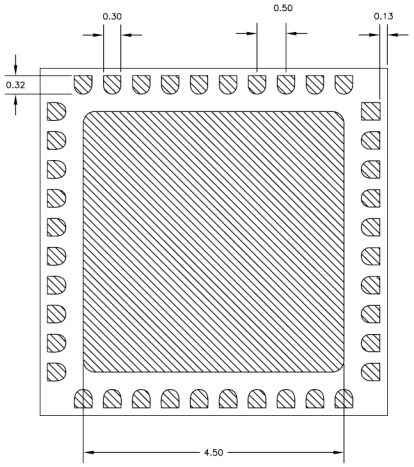
Table 3: DC Pin Descriptions

Port Name	Description	Notes
POL	Polarity of Phase Detector	3.3 V CMOS levels, defaults to logic 0 if open
R[6:0]	Reference Prescaler Divide Ratio	3.3 V CMOS levels, defaults to logic 0 if open
V[6:0]	VCO Prescaler Divide Ratio	3.3 V CMOS levels, defaults to logic 0 if open
A[3:0]	Charge Pump Gain Control	3.3 V CMOS levels, defaults to logic 0 if open
VADJ	Charge Pump Gain Analog Control	From VEE to VCC , VCC for max output
VADR	Divided Reference Output Level Control	From VEE to VCC , VCC for max output
VADV	Divided VCO Output Level Control	From VEE to VCC , VCC for max output
VCC1-4	Positive power supply	+3.3 V @ 500 mA
VEE1-4	Negative power supply	Ground

Pinout Diagram



UXN40M7K Physical Characteristics



Pkg Size:	6.00 x 6.00 mm
Pkg Thickness:	1.1 mm
Pad Dimensions:	0.30 x 0.32 mm
Center Paddle:	4.5 x 4.5 mm
JEDEC Designator:	MO-220
JEDEC designator:	MO-220

Bottom View

Table 4: Absolute Maximum Ratings

Parameter	Value	Unit
Supply Voltage (VCC-VEE)	4	V
RF Input Power (INP, INN)	10	dBm
Operating Temperature	-40 to 85	ºC
Storage Temperature	-85 to 125	ºC
Junction Temperature	125	ºC

ESD Sensitivity:

Although SiGe IC's have robust ESD sensitivities, preventive ESD measures should be taken while storing, handling, and assembling. Inputs are more ESD susceptible as they could expose the base of a BJT or the gate of a MOSFET. For this reason, all the low frequency inputs are protected with ESD diodes. These inputs have been tested to withstand voltage spikes up to 400 V. For performance reasons the RF inputs are not protected with ESD diodes and the ESD sensitivity is higher.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo CA 92656 USA
Within the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense and security, aerospace, and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs, and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif. and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.