

POLARFIRE SPLASH KIT

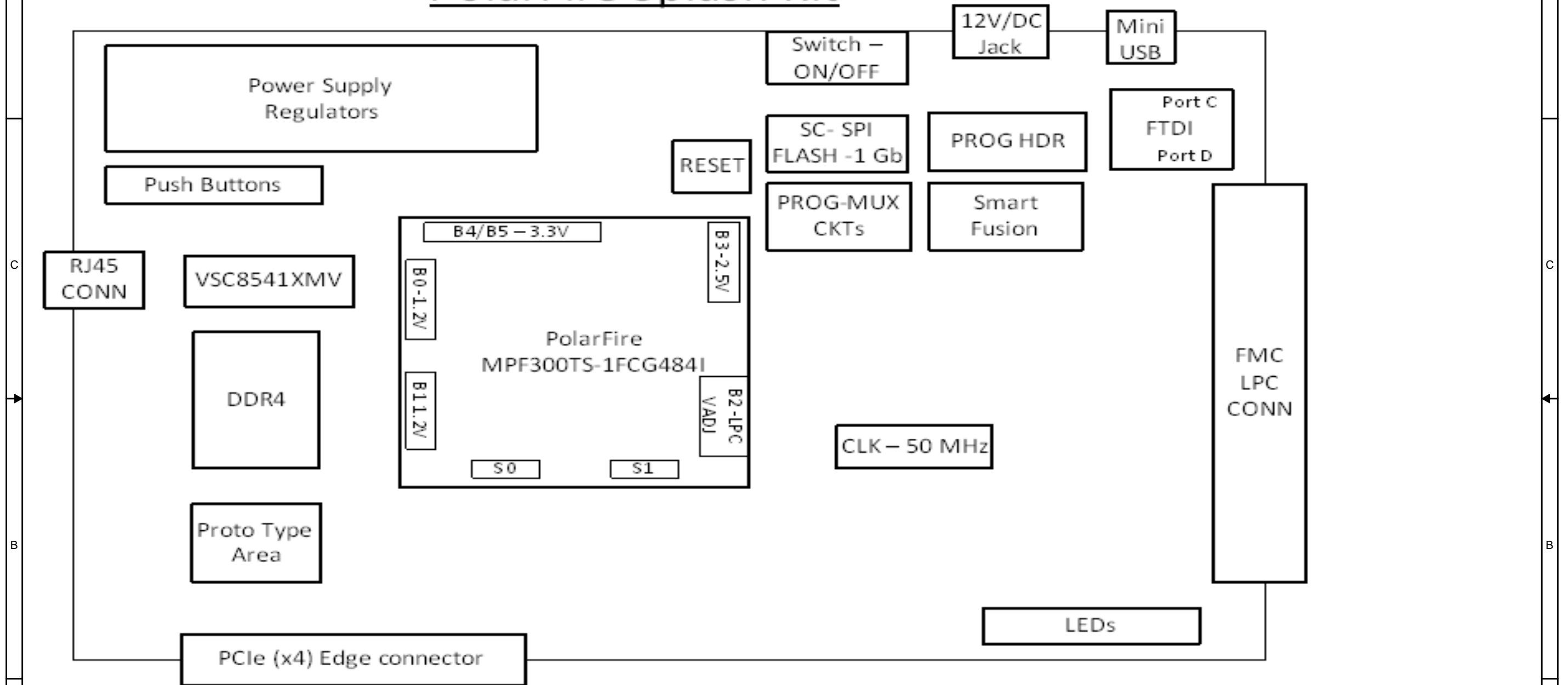
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Project Name:		POLARFIRE SPLASH KIT	
Rev	Part Number:		
2	MICROSEMI DVP-100-000496-001	PACTRON:	305-PD-17-0043
Originator:		GHURU KUMARAVELU	
Size	Date:		
Custom	Monday, October 16, 2017	Sheet	1 of 32

BLOCK DIAGRAM

PolarFire Splash Kit

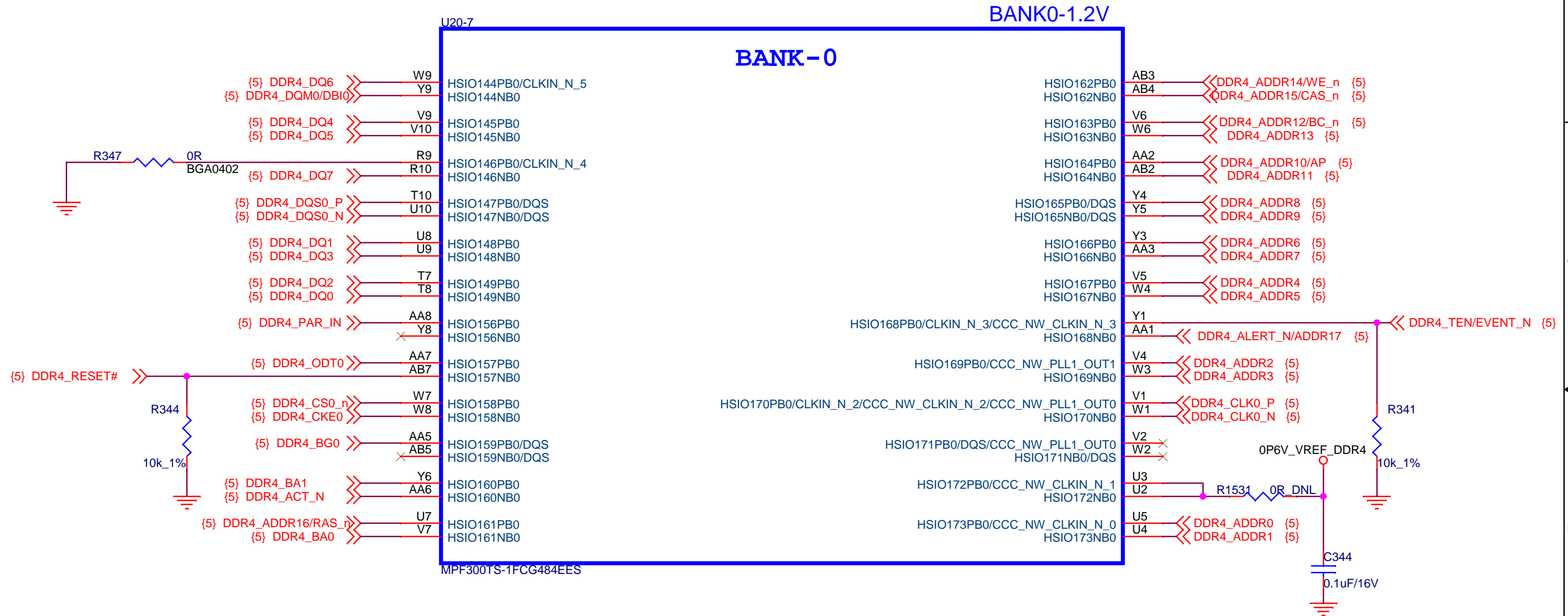


standard height half-length card



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BANK-0-DDR4



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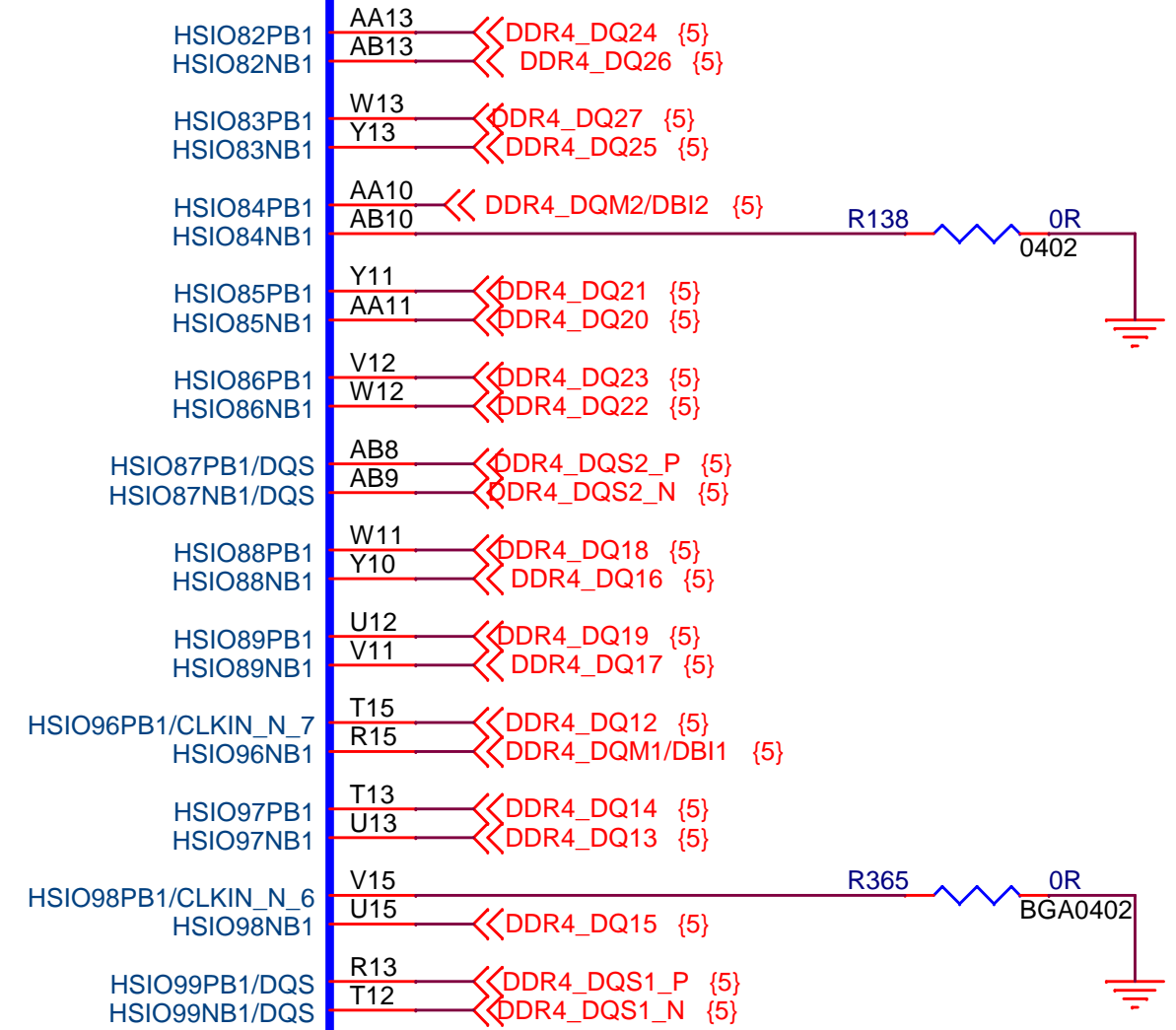
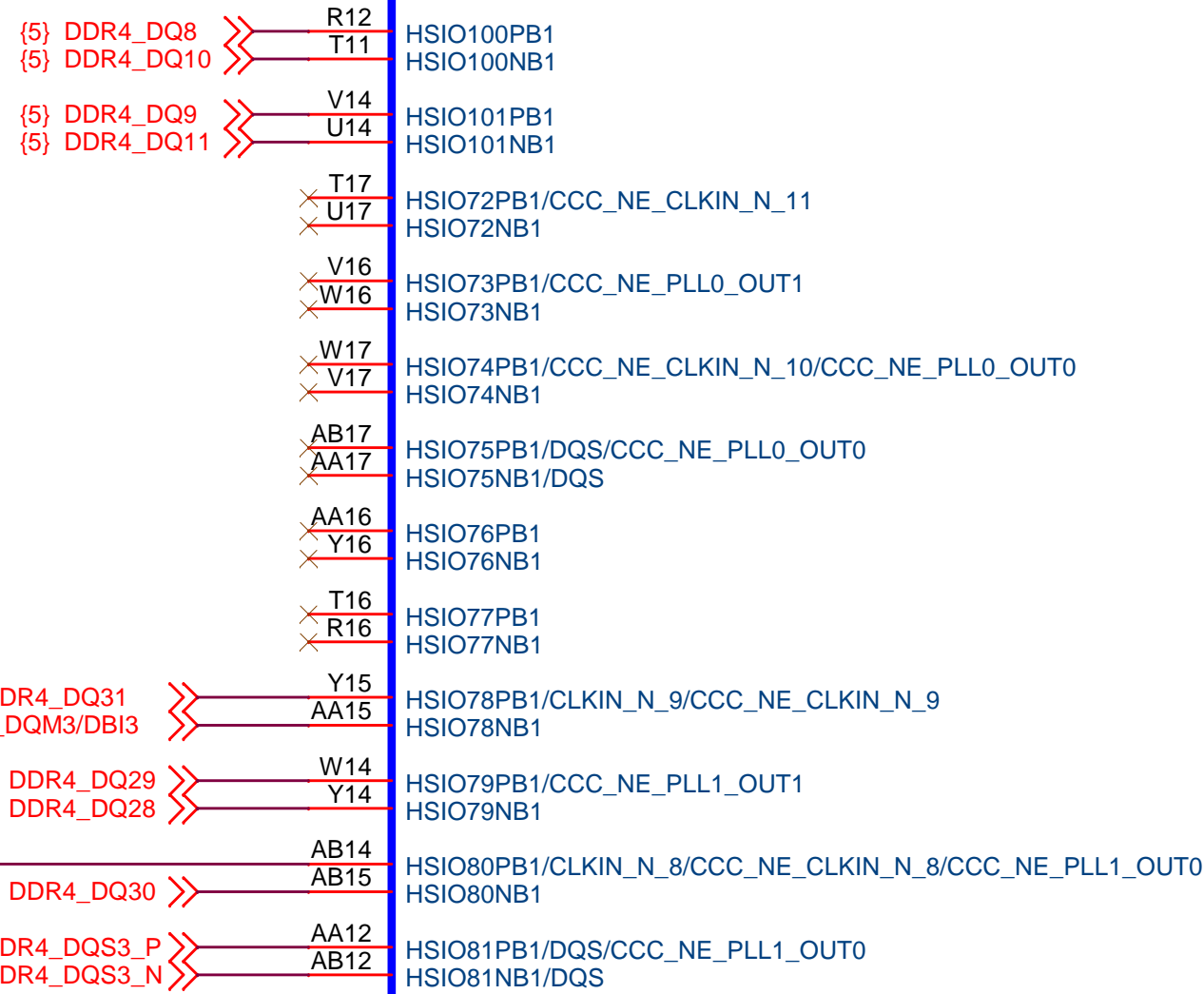
BANK-1-DDR4

BANK1-1.2V

BANK-1

U20-8

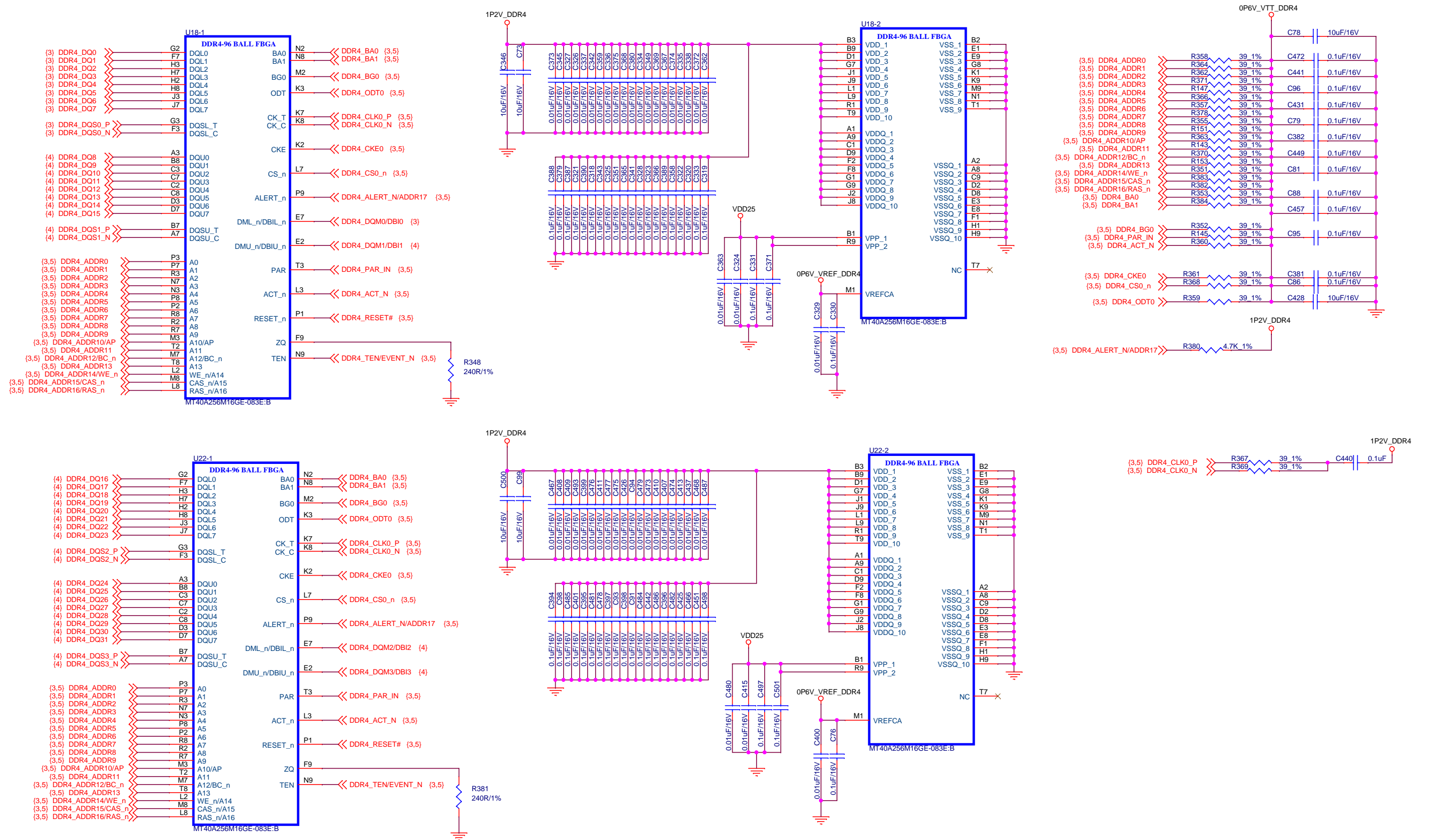
MPF300TS-1FCG484EES



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DDR4 MEMORY -BANK0 & 1

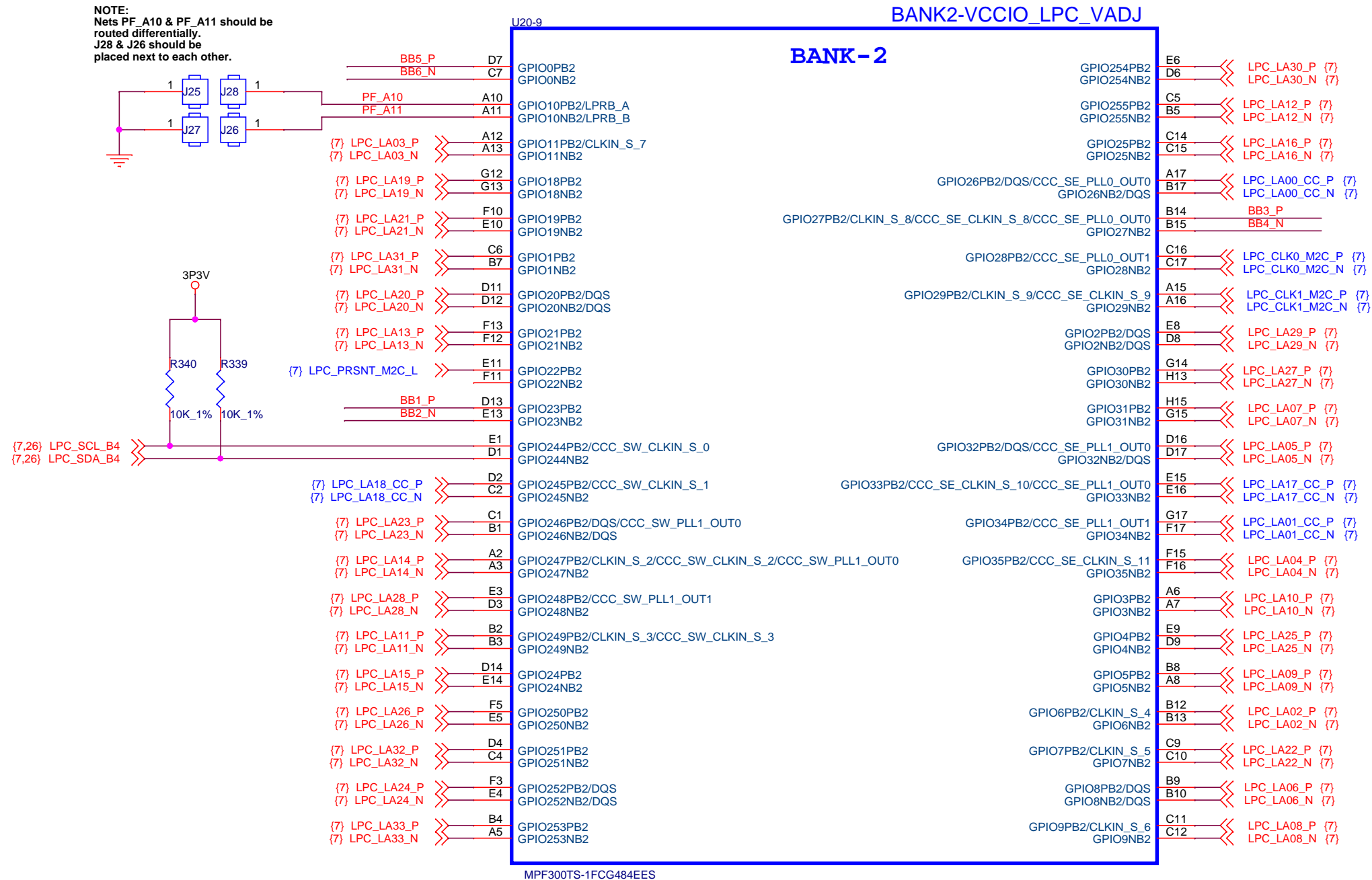


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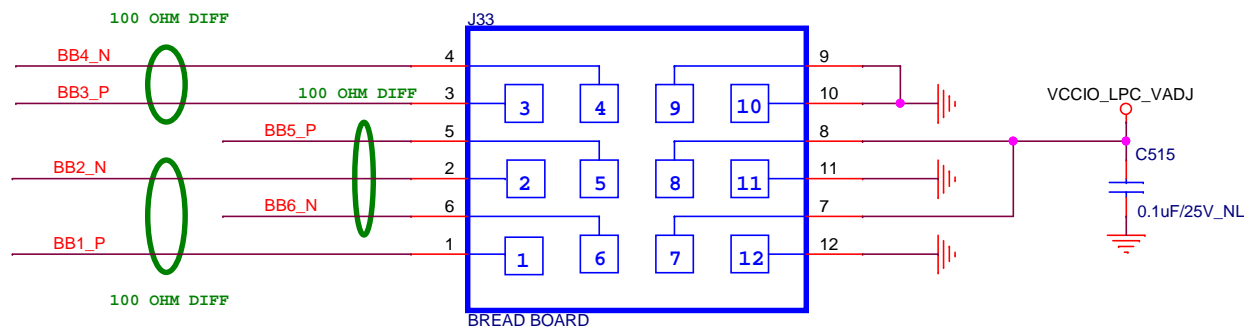


BANK2-LPC & BREAD BOARD

NOTE:
Nets PF_A10 & PF_A11 should be routed differentially.
J28 & J26 should be placed next to each other.



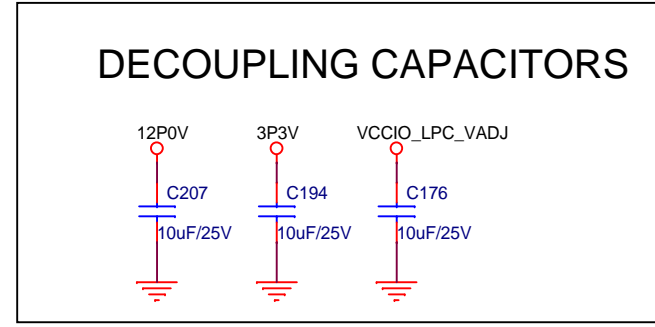
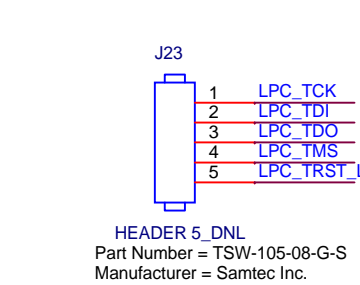
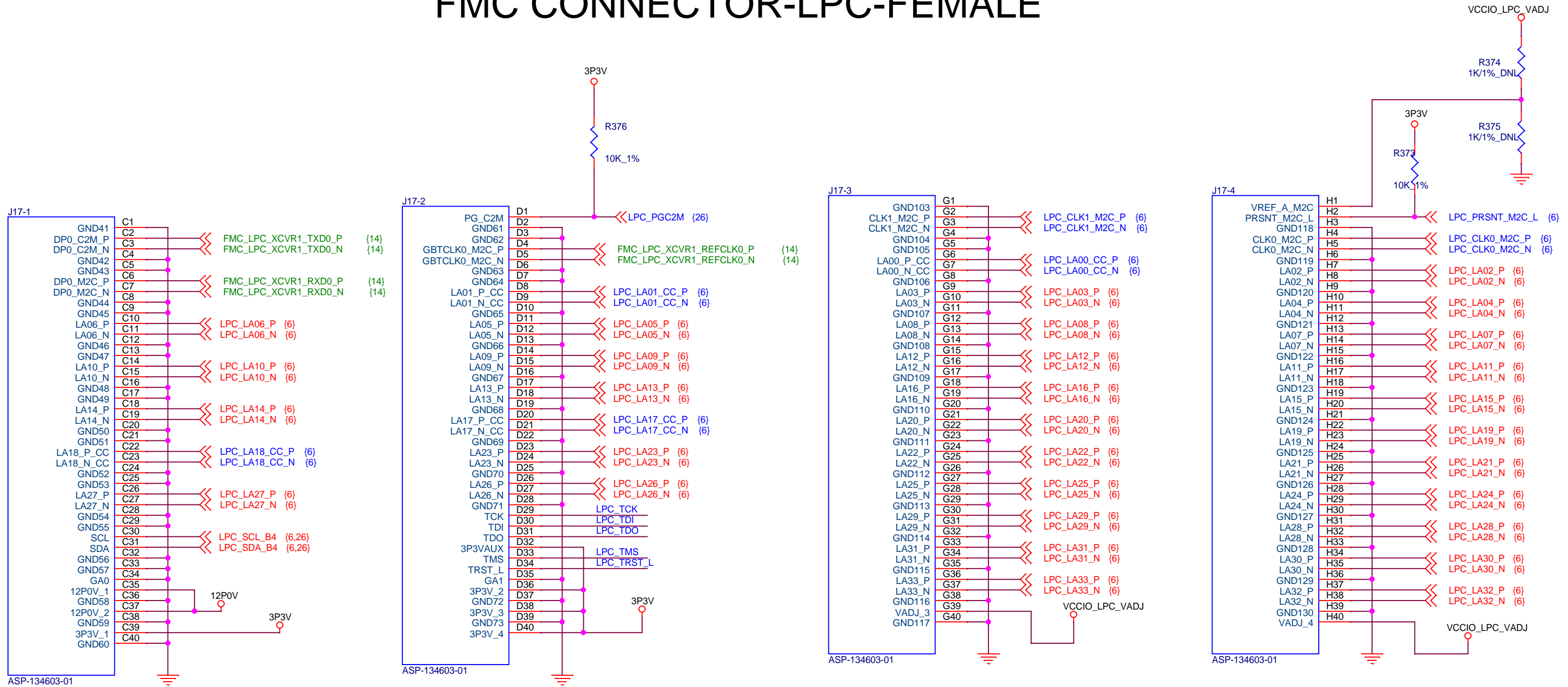
BREAD BOARD



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FMC CONNECTOR-LPC-FEMALE



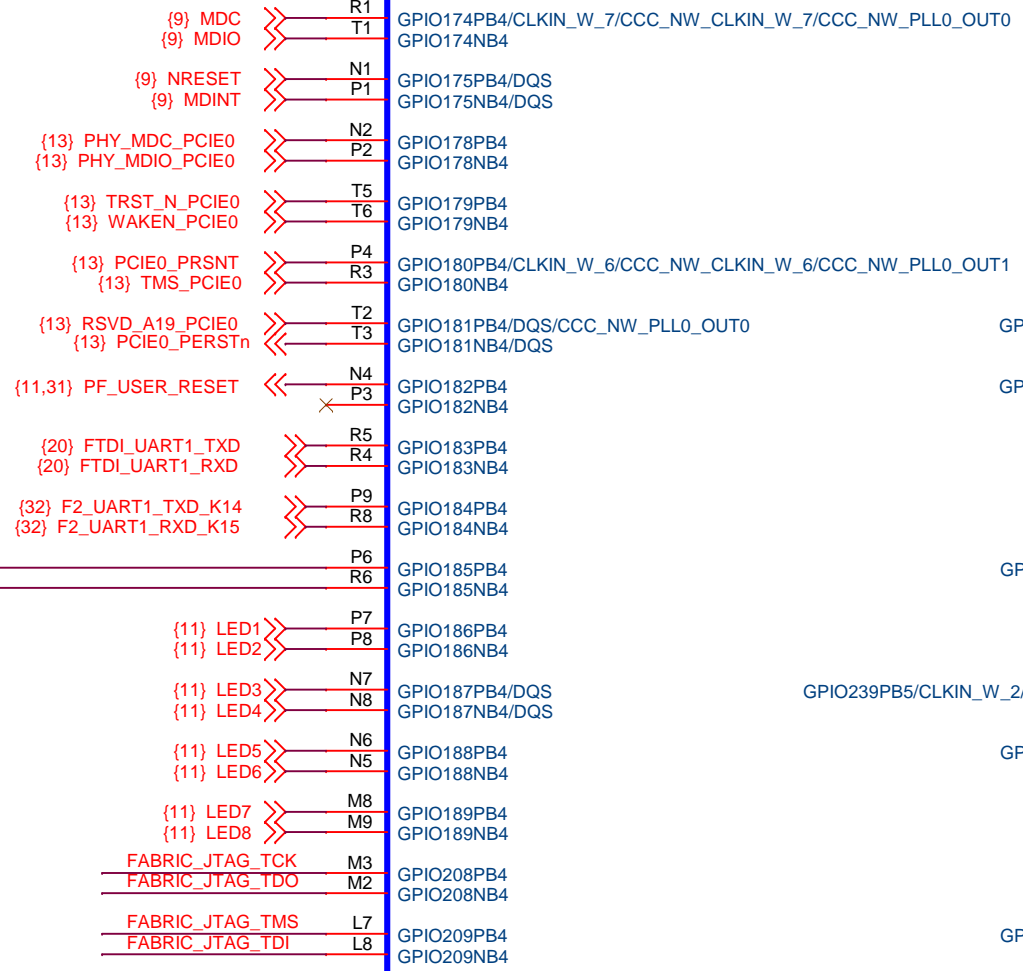
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BANK-4-VSC RGMII, Debug, UART

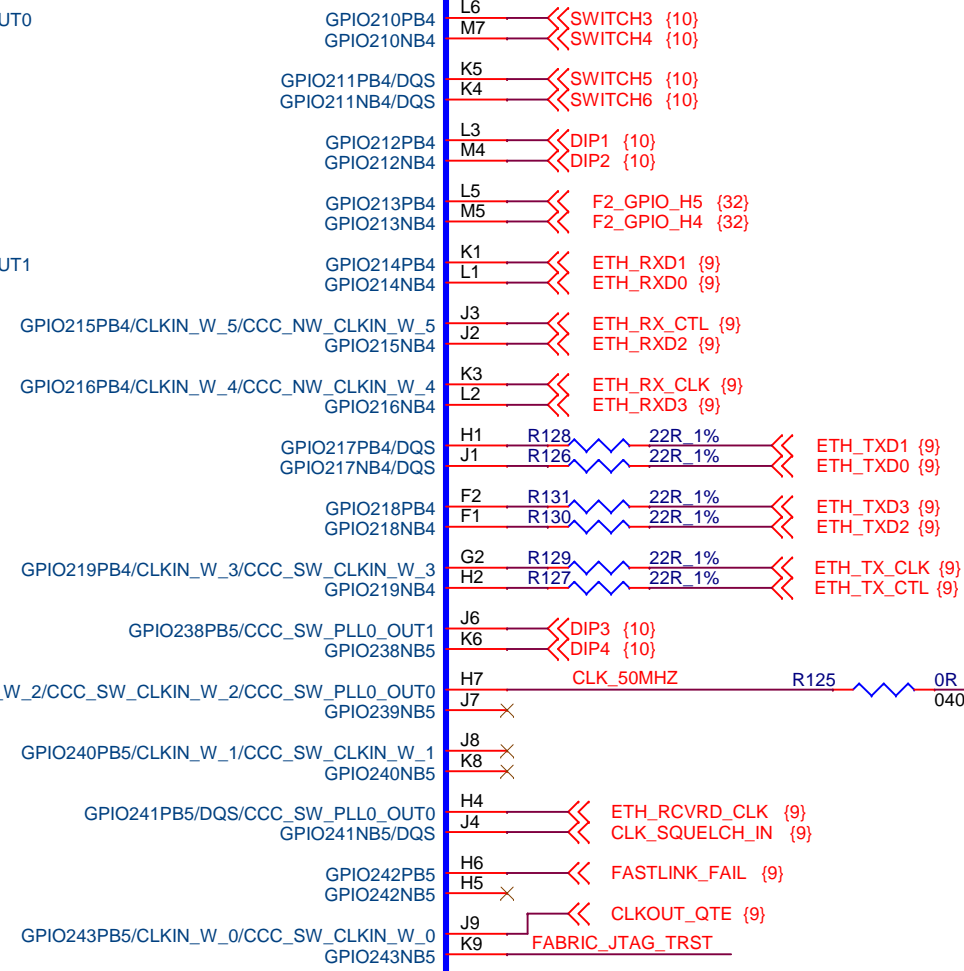
BANK4-3.3V

U20-10

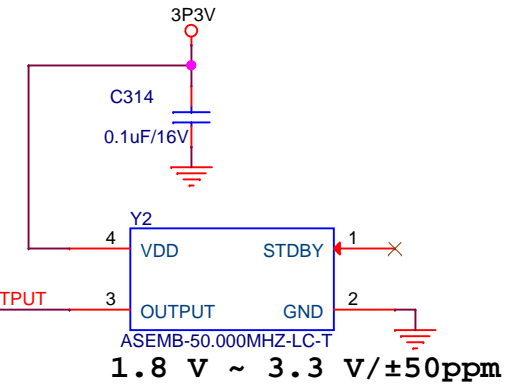
BANK-4



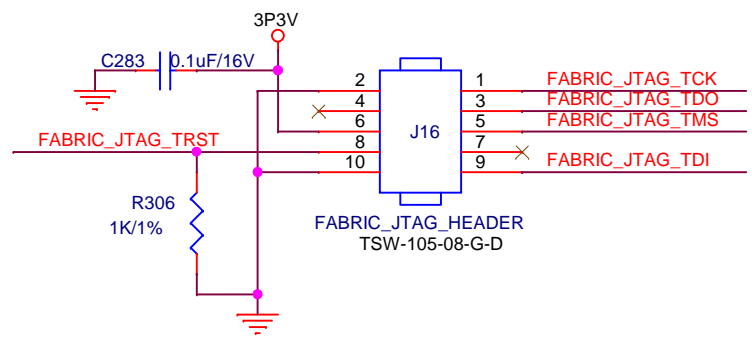
PLACED FOR INTERNAL DEBUGGING PURPOSE ONLY



CLK -50MHz



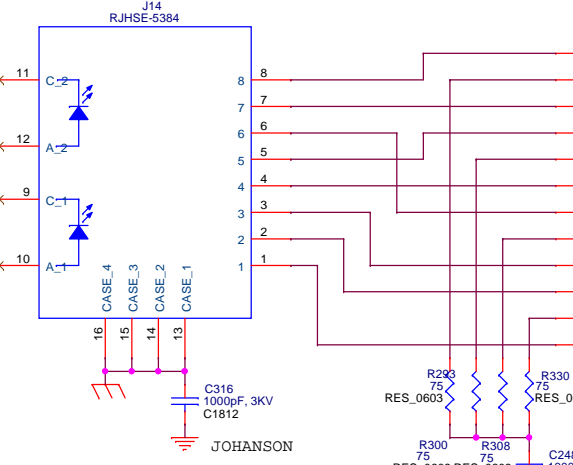
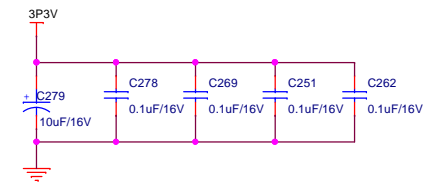
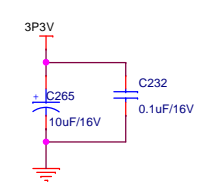
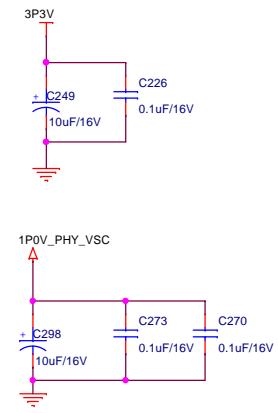
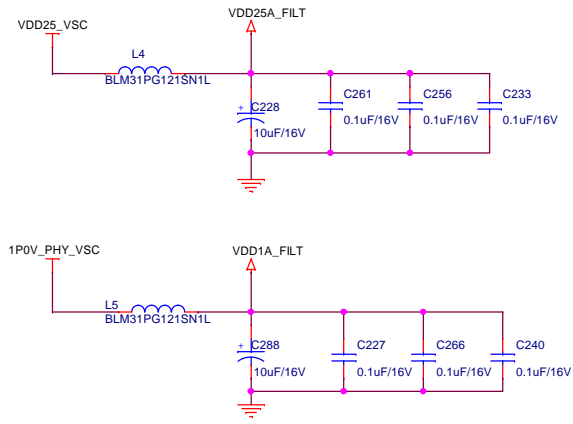
FABRIC_JTAG_HEADER



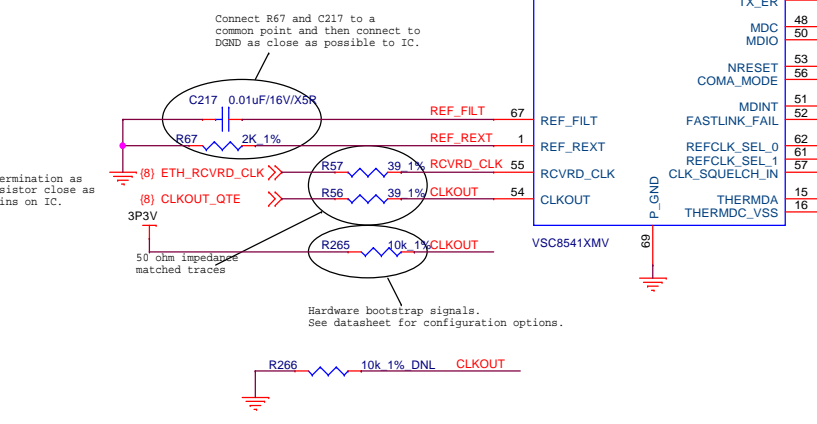
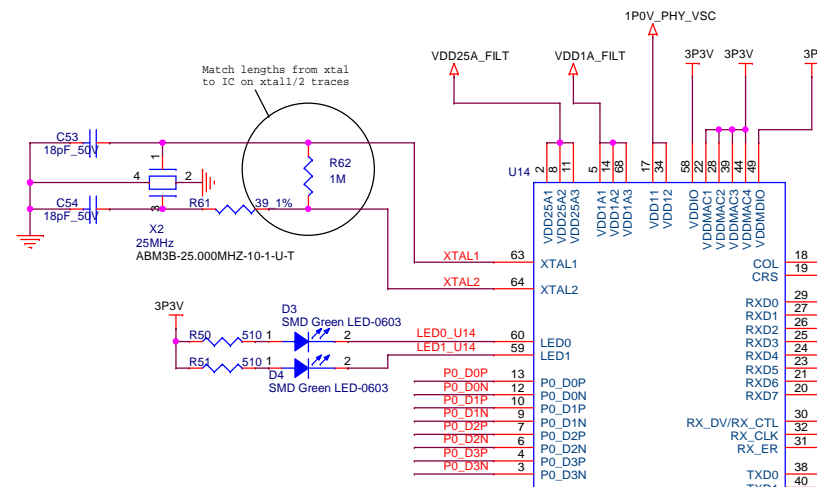
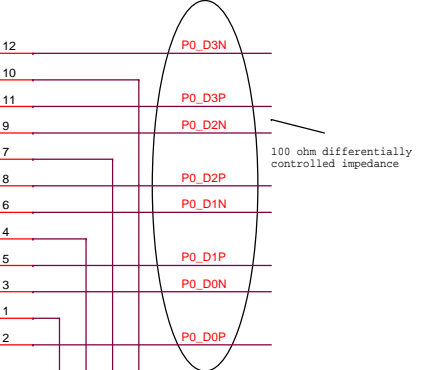
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VSC8541XMV

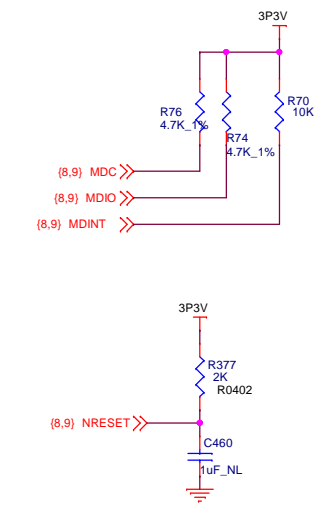
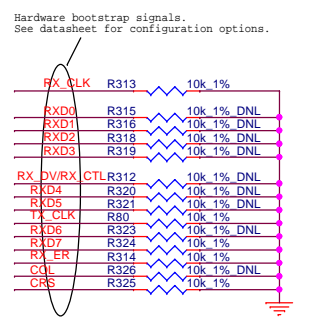
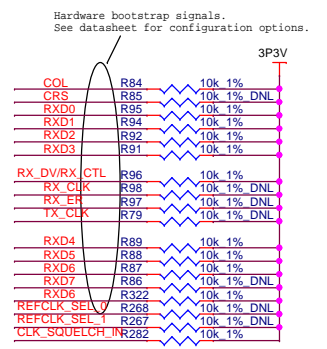
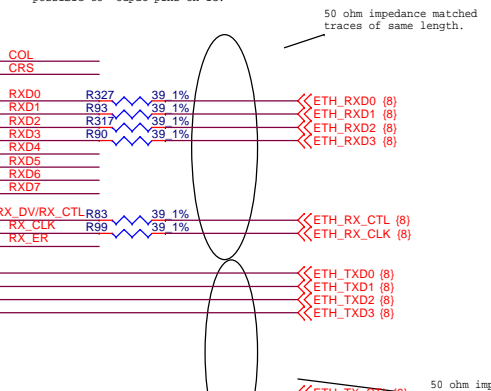
Place 0.1uF 0402 decoupling caps as close as possible to IC power pins.



LAYOUT NOTE:
VSC8541 copper MDI signals to PHY-side of transformers: 100 Ohm differentially routed impedance



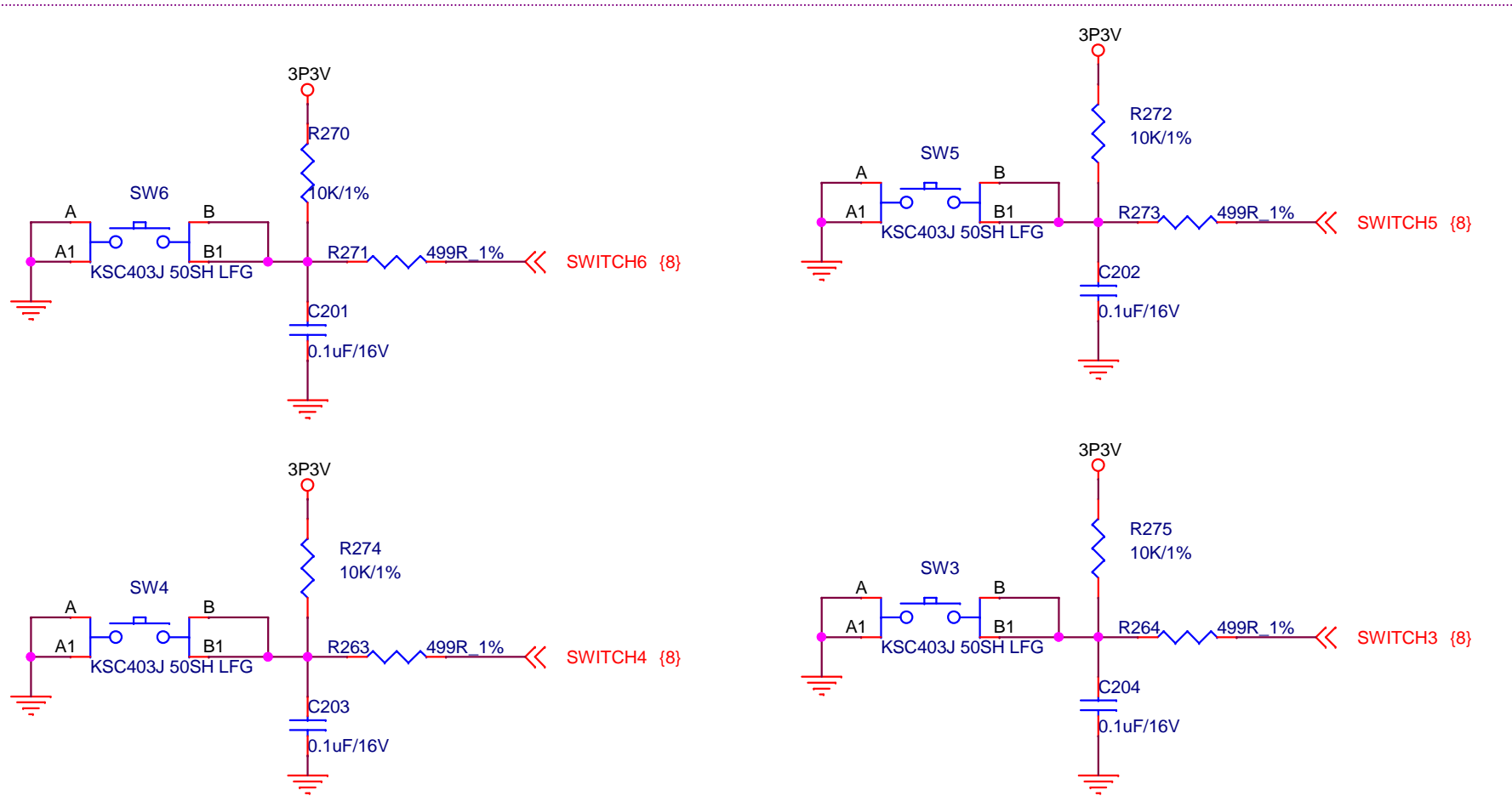
Select series termination resistors to match MAC output resistance of IC based on choice of VDDMAC supply. See PCB guidelines and datasheets for recommended values.
Place 39ohm series termination as and 10k bootstrap resistor close as possible to output pins on IC.



Place 39ohm series termination as and 10k bootstrap resistor close as possible to output pins on IC.

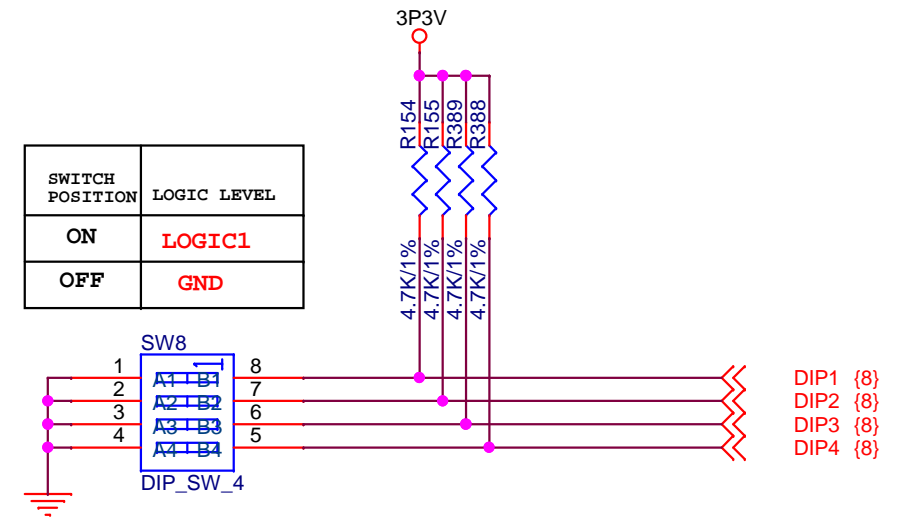
Hardware bootstrap signals. See datasheet for configuration options.

DEBUG CIRCUITRY



PUSH BUTTON SWITCH CONNECTION TABLE

NET NAME	FPGA PIN NO	FPGA PIN NAME	BANK
SWITCH3	L6	GPIO210PB4	BANK-4
SWITCH4	M7	GPIO210NB4	BANK-4
SWITCH5	K5	GPIO211PB4/DQS	BANK-4
SWITCH6	K4	GPIO211NB4/DQS	BANK-4



SWITCH POSITION	LOGIC LEVEL
ON	LOGIC1
OFF	GND

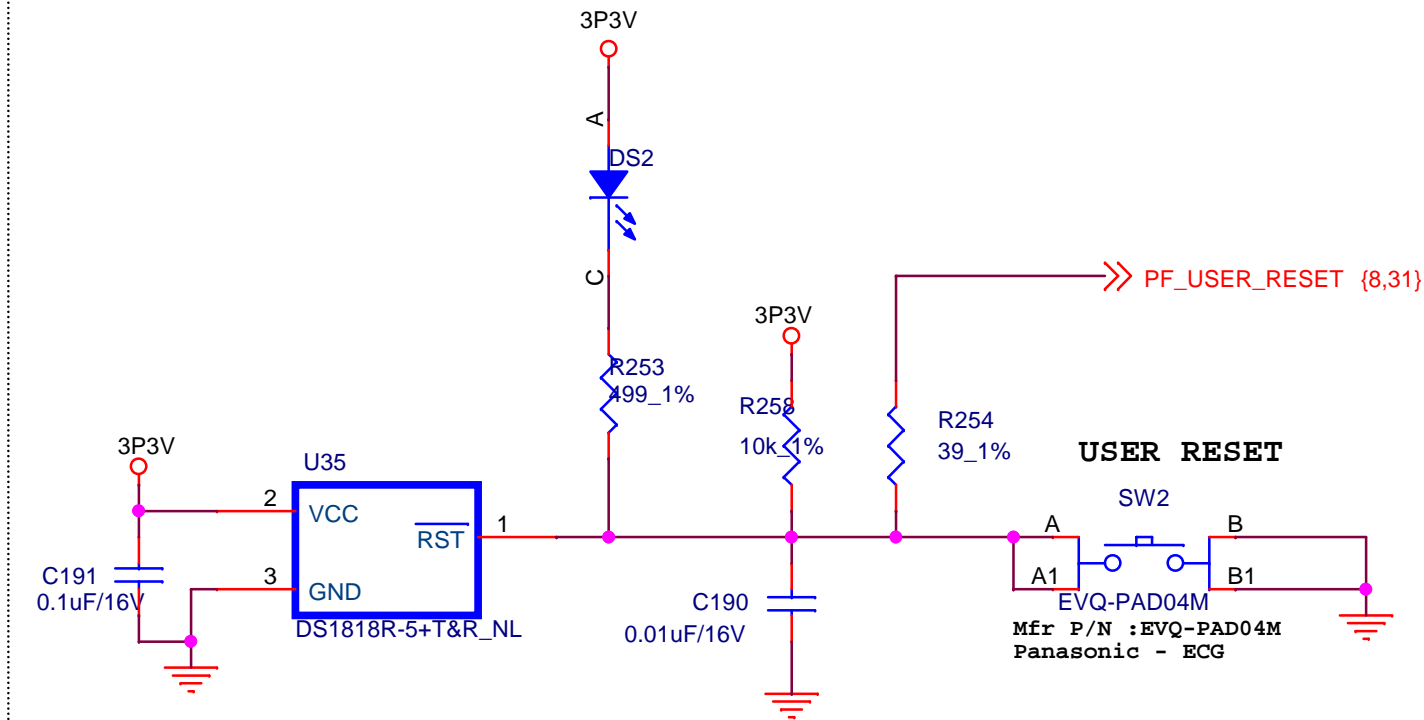
DIP SWITCH CONNECTION TABLE

NET NAME	FPGA PIN NO	FPGA PIN NAME	BANK
DIP1	L3	GPIO212PB4	BANK-4
DIP2	M4	GPIO212NB4	BANK-4
DIP3	J6	GPIO238PB5/CCC_SW_PLL0_OUT1	BANK-4
DIP4	K6	GPIO238NB5	BANK-4



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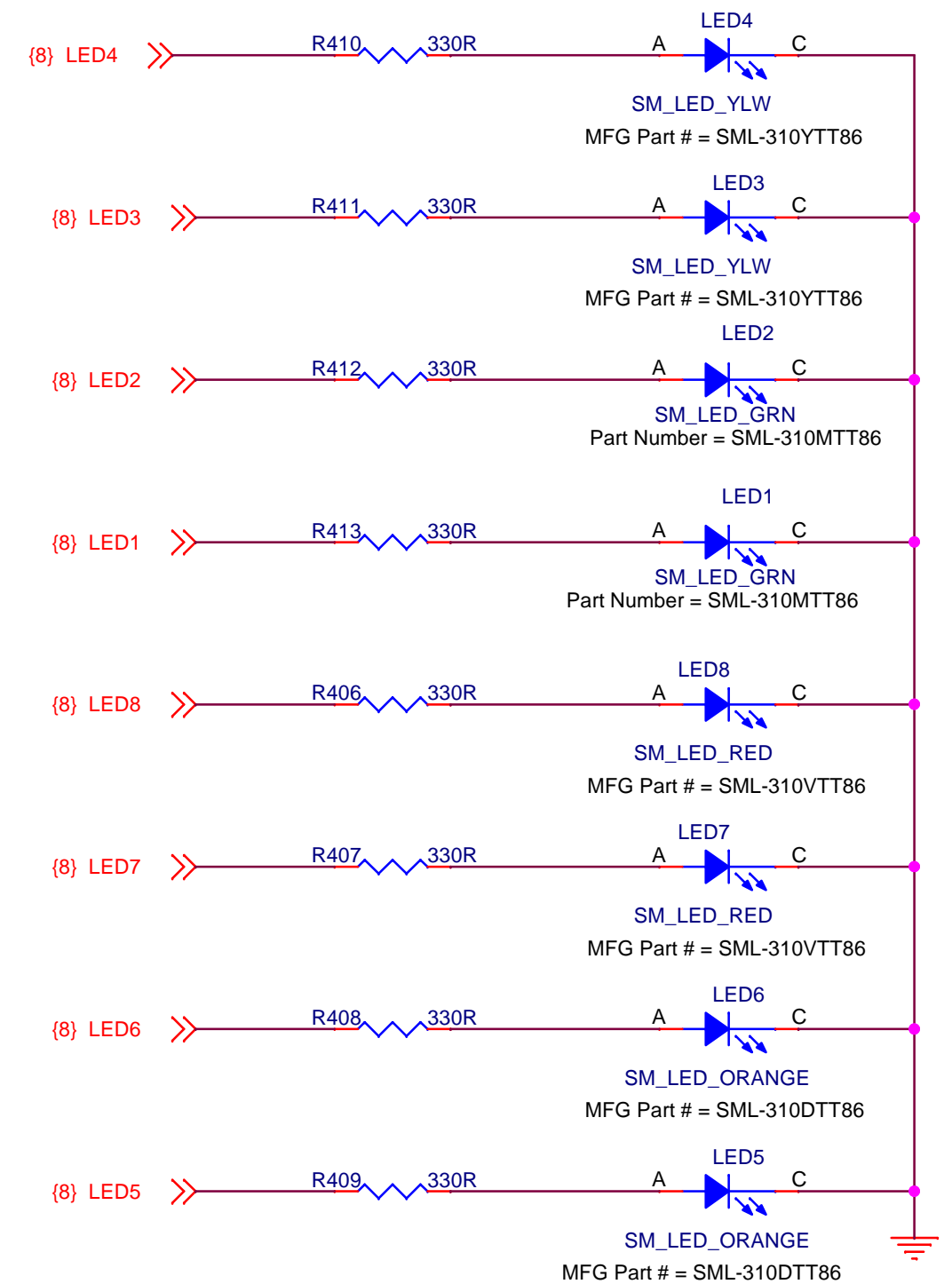
PolarFire_USER_RESET



LED CONNECTION

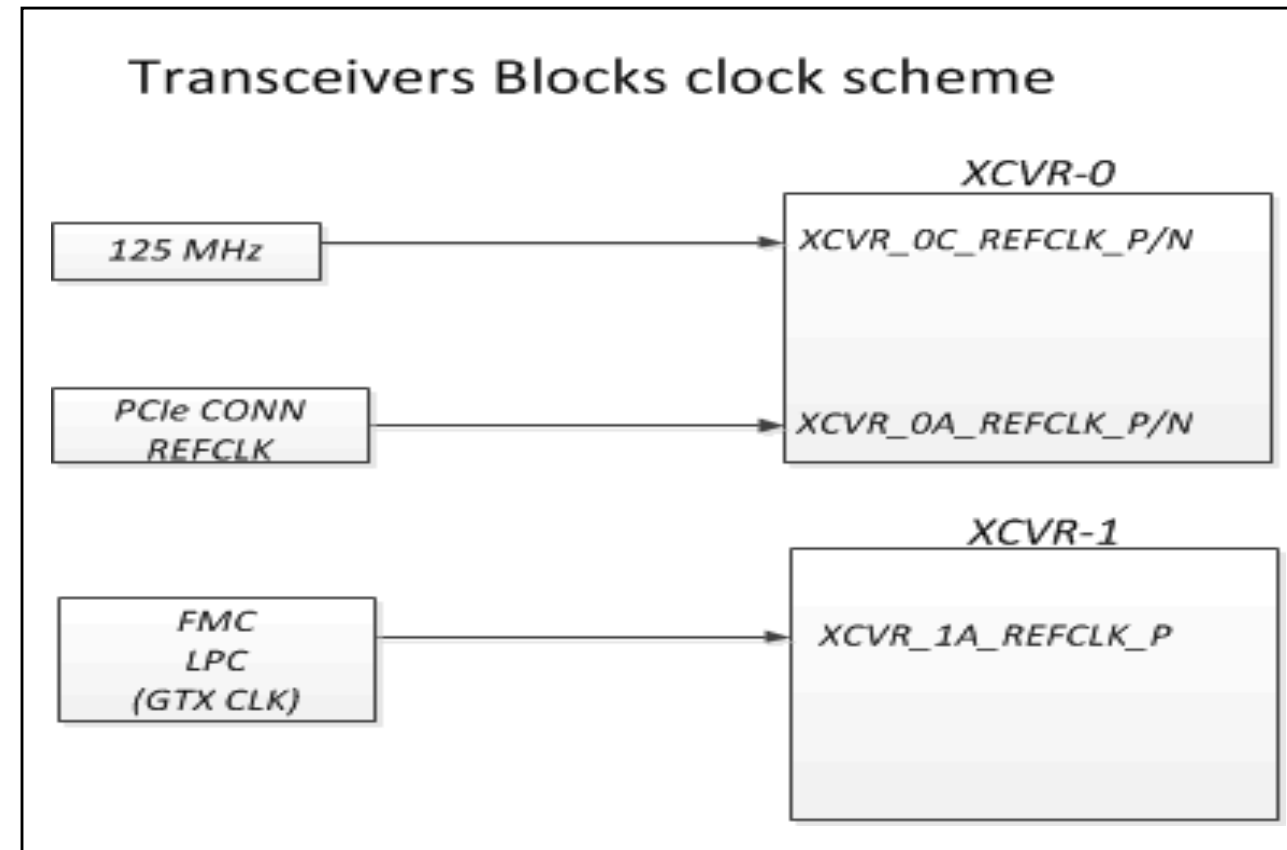
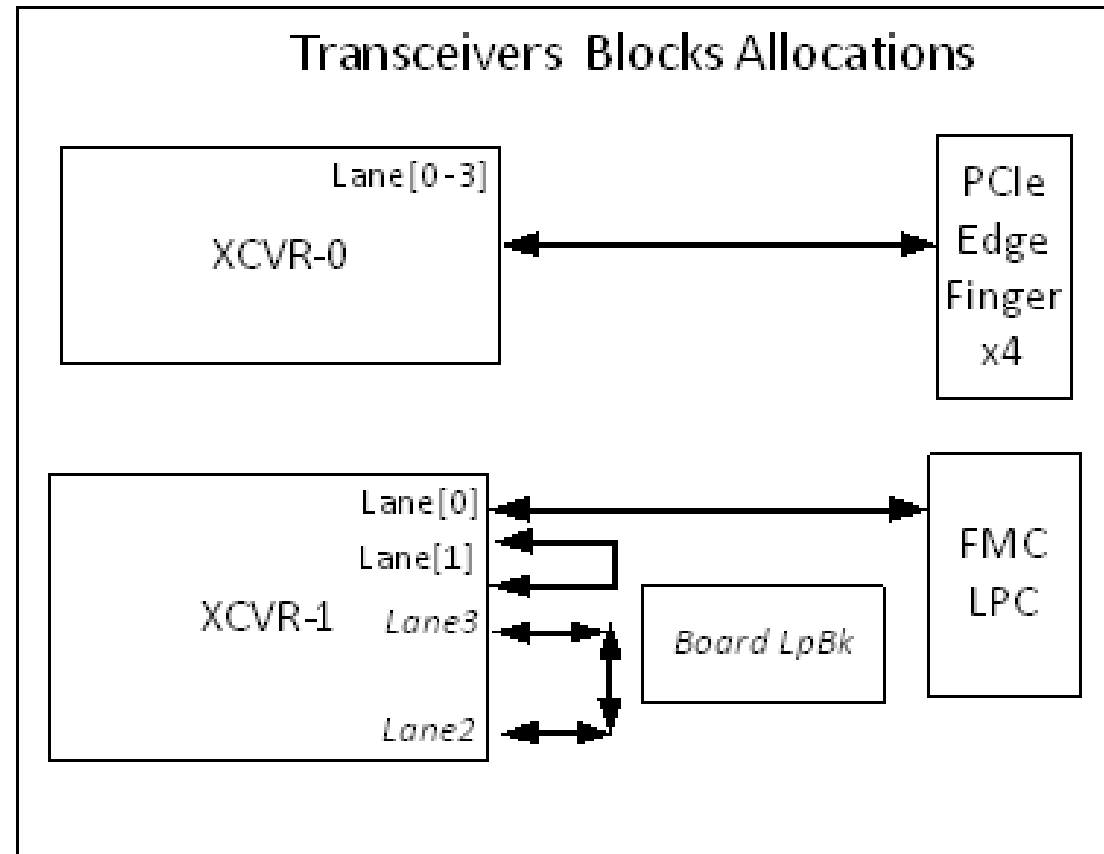
NET NAME	FPGA PIN NO	FPGA PIN NAME	BANK
LED1	P7	GPIO186PB4	BANK-4
LED2	P8	GPIO186NB4	BANK-4
LED3	N7	GPIO187PB4/DQS	BANK-4
LED4	N8	GPIO187NB4/DQS	BANK-4
LED5	N6	GPIO188PB4	BANK-4
LED6	N5	GPIO188NB4	BANK-4
LED7	M8	GPIO189PB4	BANK-4
LED8	M9	GPIO189NB4	BANK-4

USER DEFINED LEDs



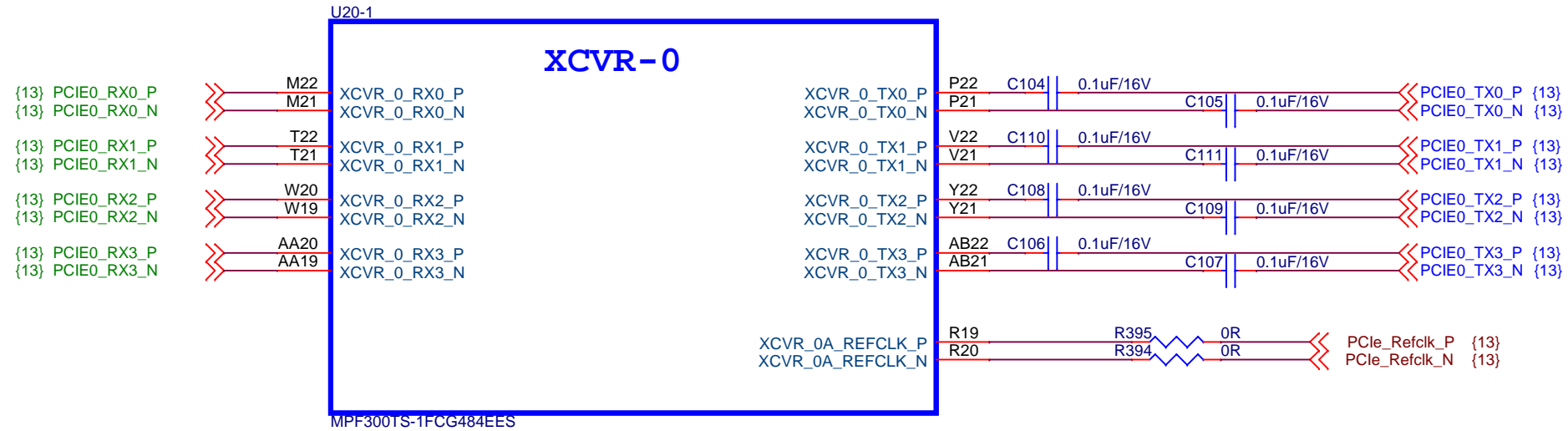
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TRANSCEIVER BLOCK DIAGRAM

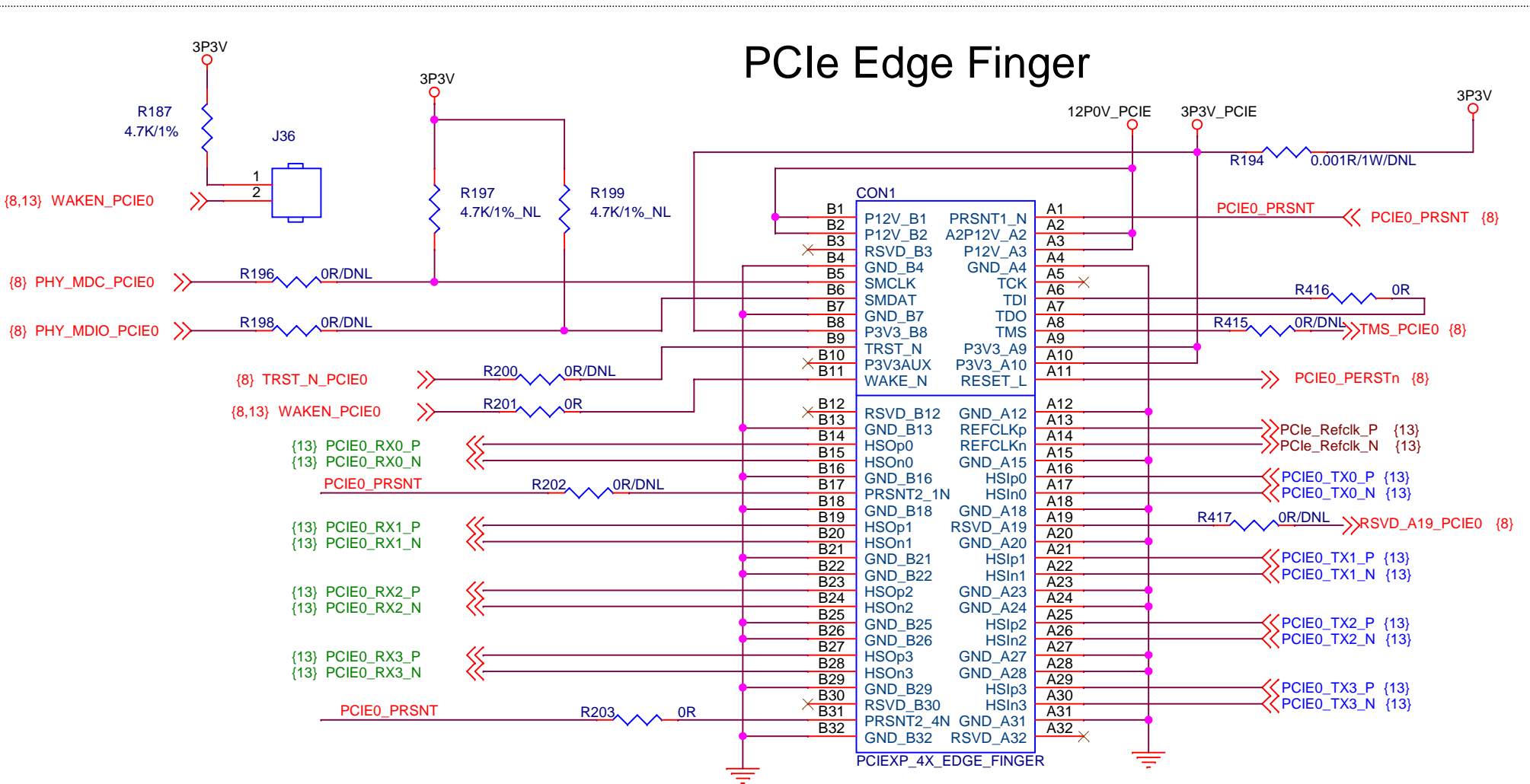


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TRANSCEIVER 0

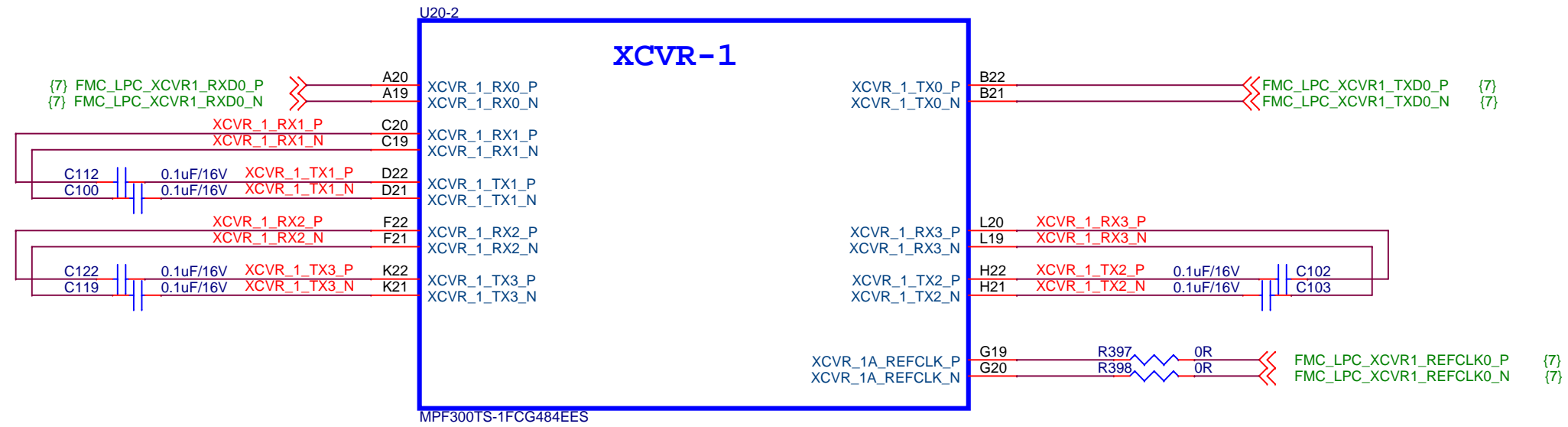


PCIe Edge Finger

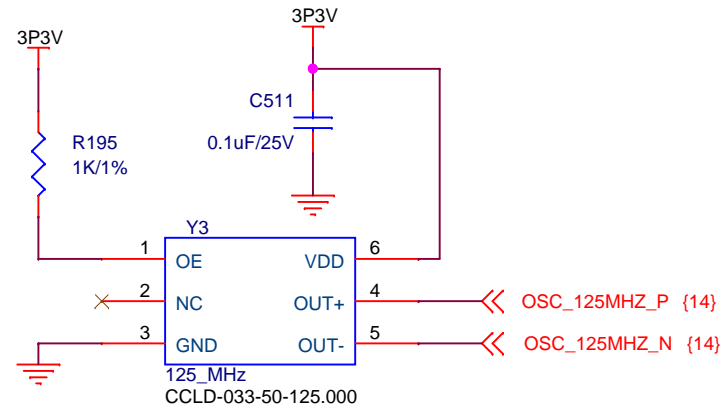


TITLE POLARFIRE SPLASH KIT			
Microsemi			
SIZE B	DOCUMENT NO. DVP-100-000496-001	REV 2	
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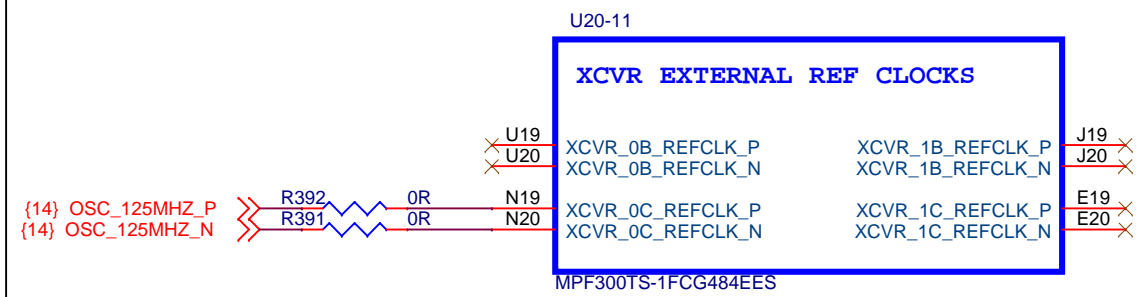
TRANSCEIVER 1



125MHz OSCILLATOR

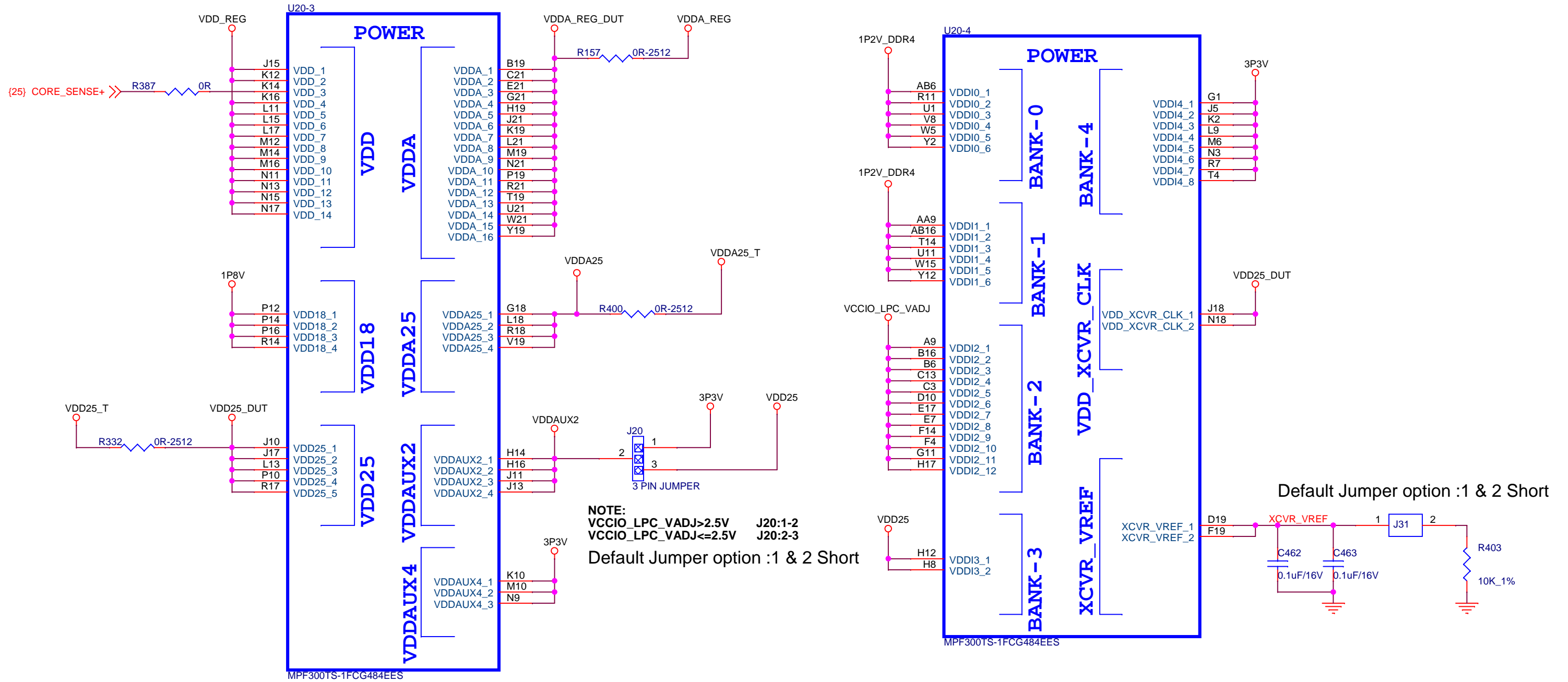


TRANSCEIVER EXTERNAL REF CLOCKS



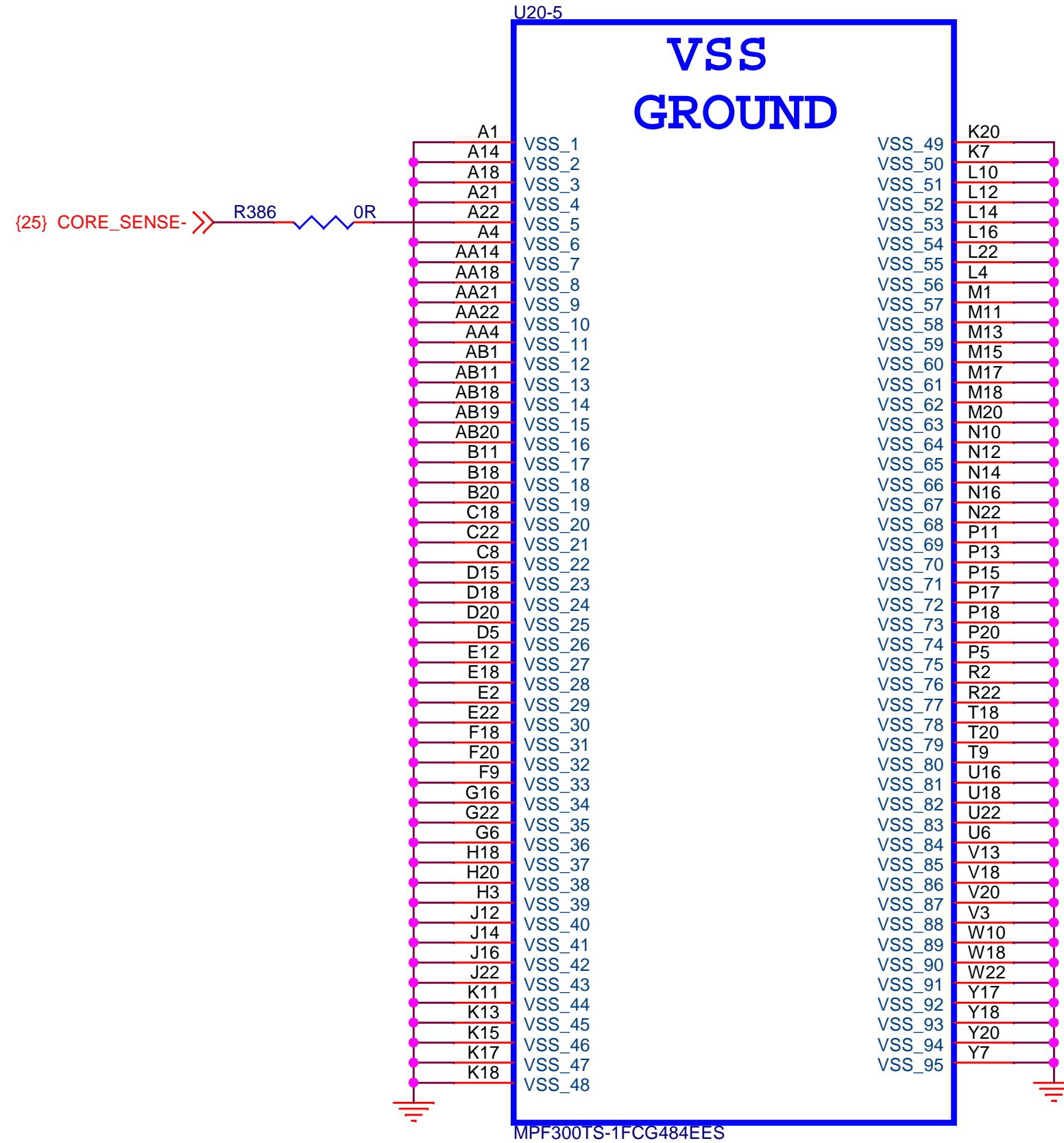
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POWER CONNECTIONS



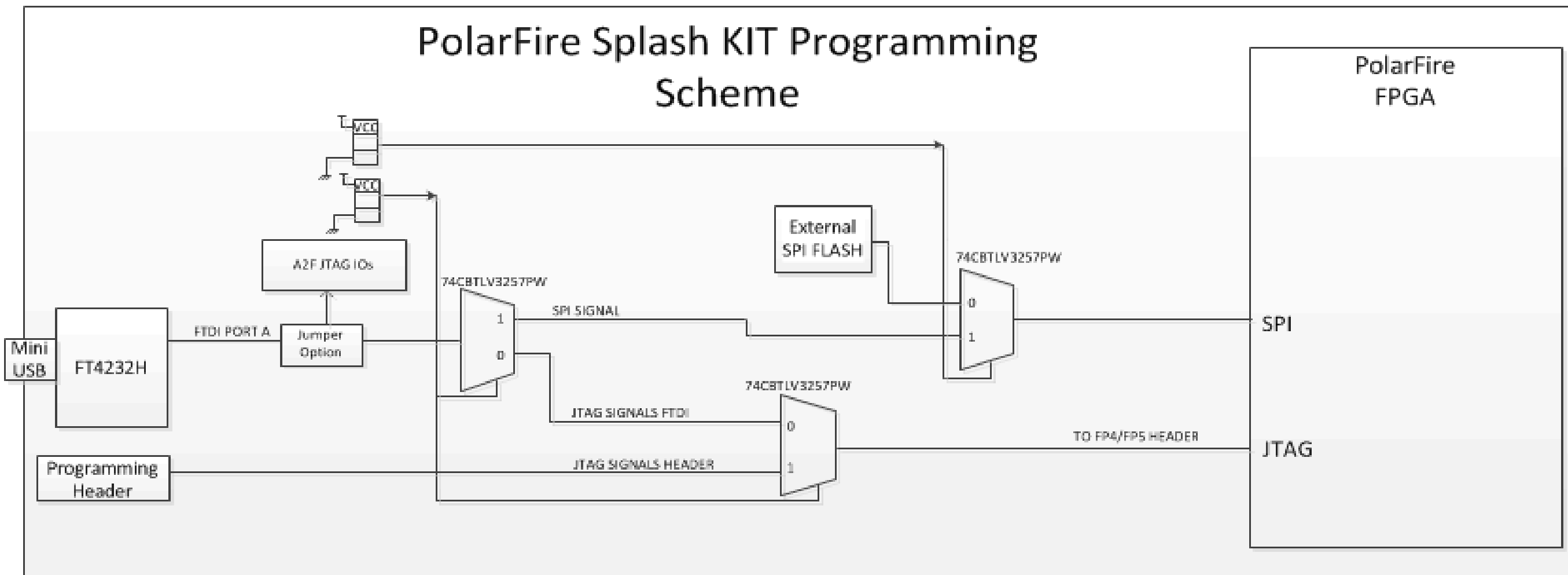
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GROUND CONNECTION



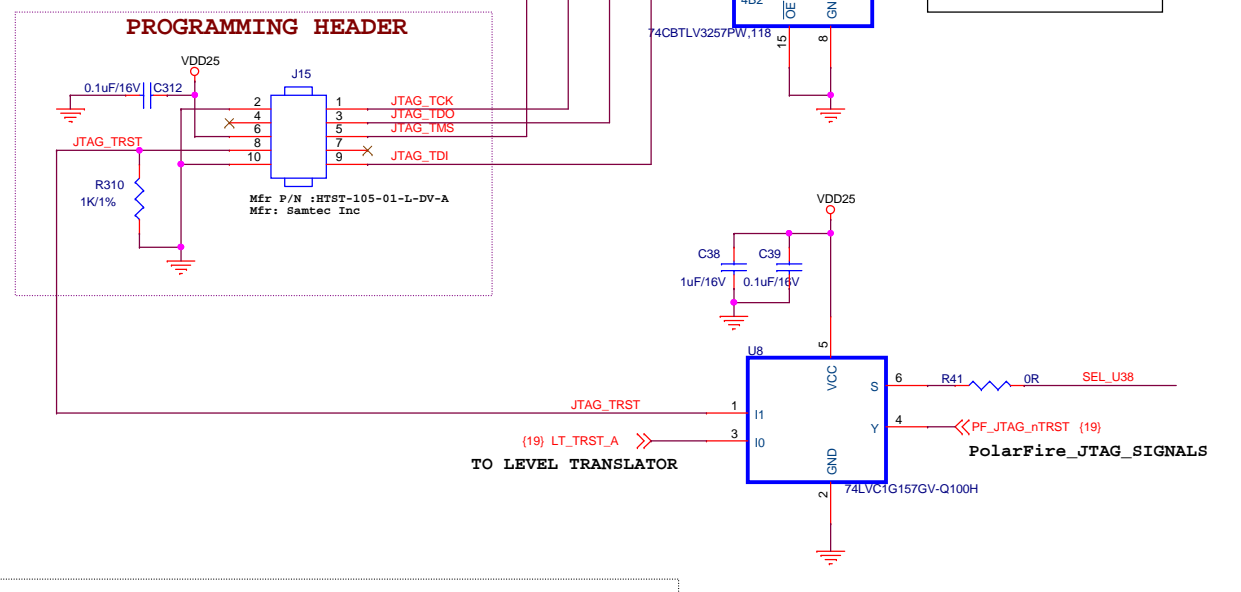
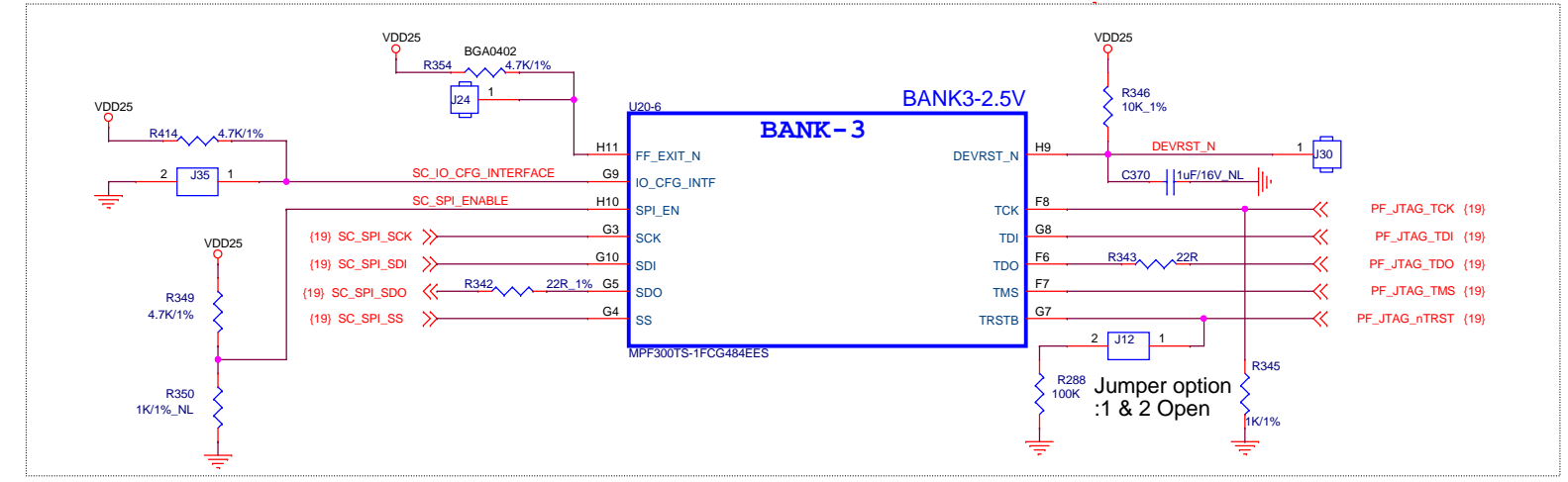
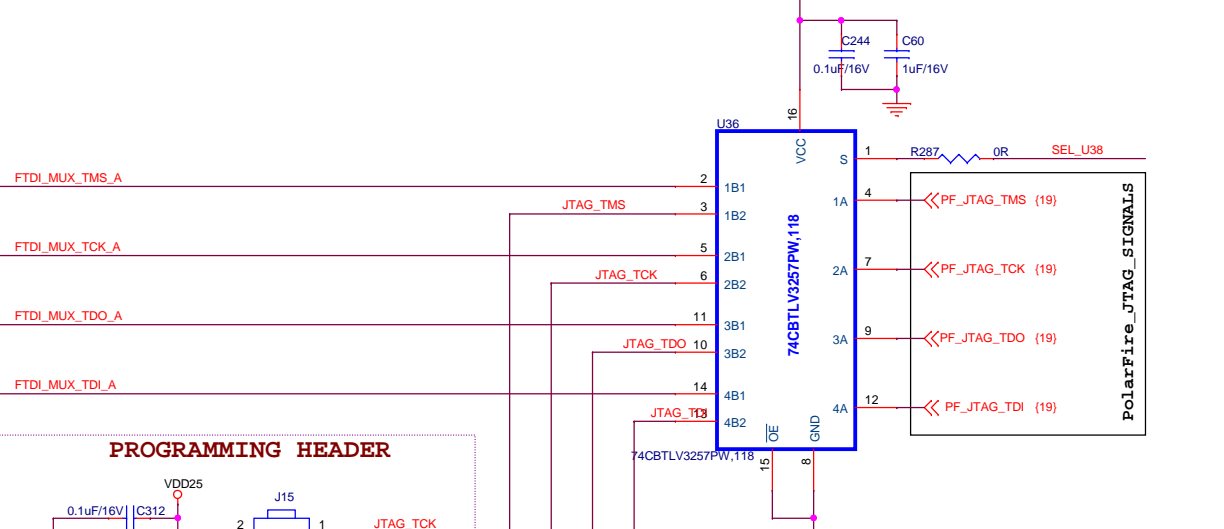
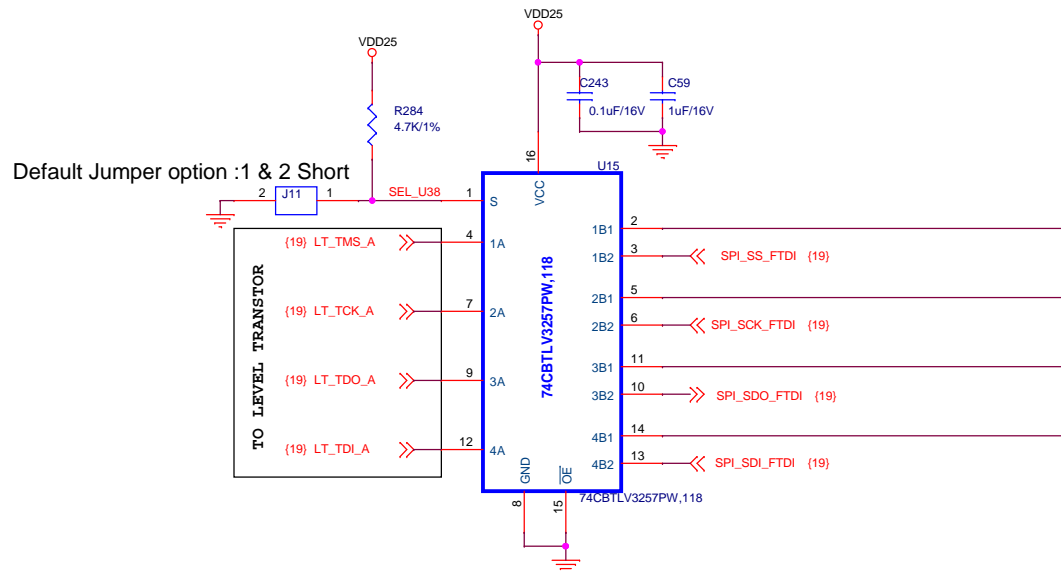
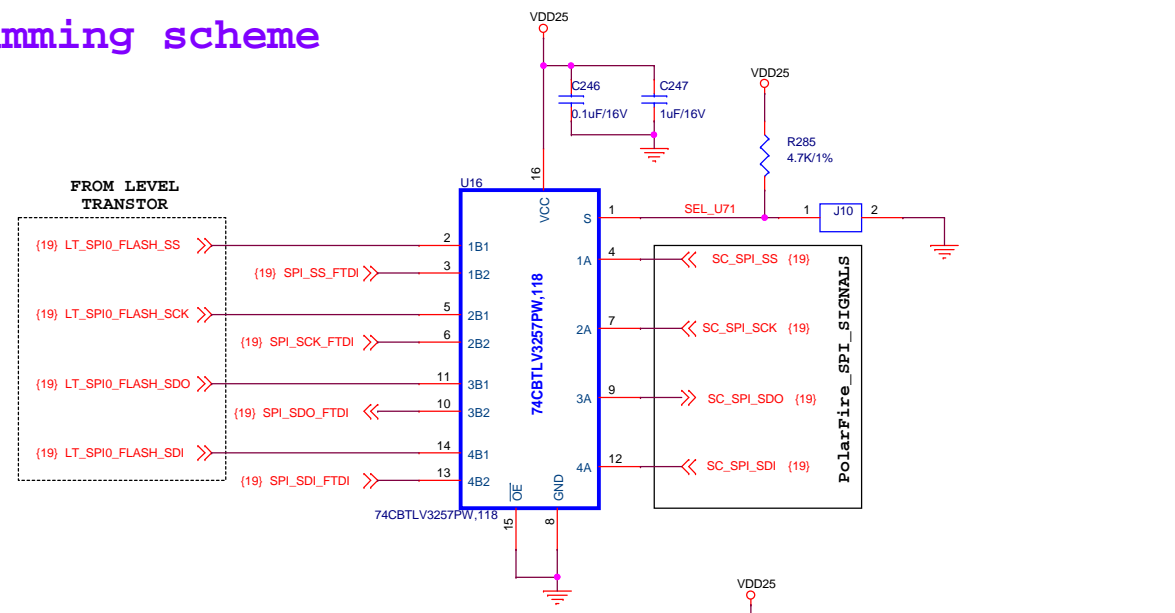
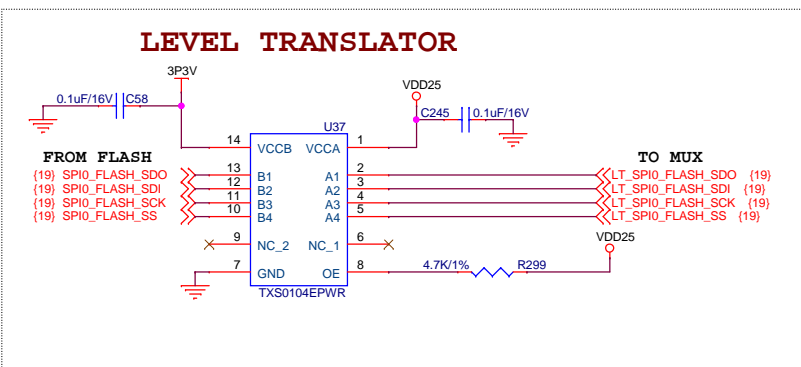
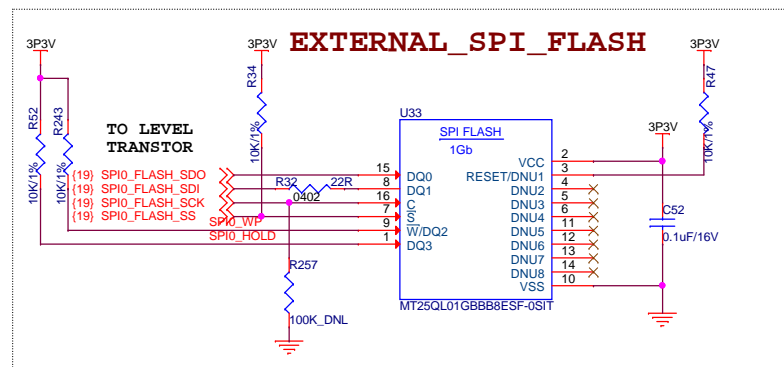
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Polarfire Splash kit programming scheme Block Diagram

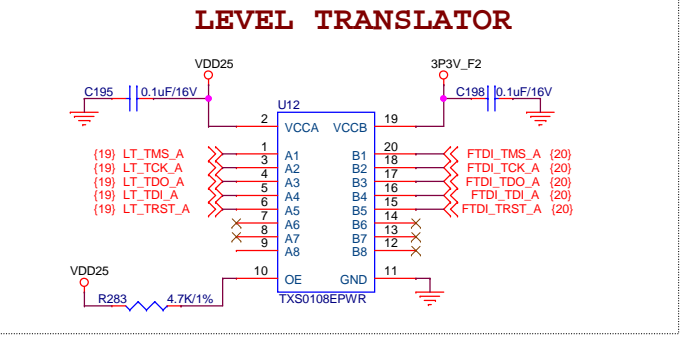
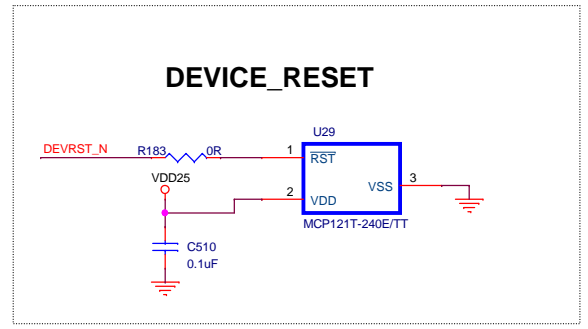


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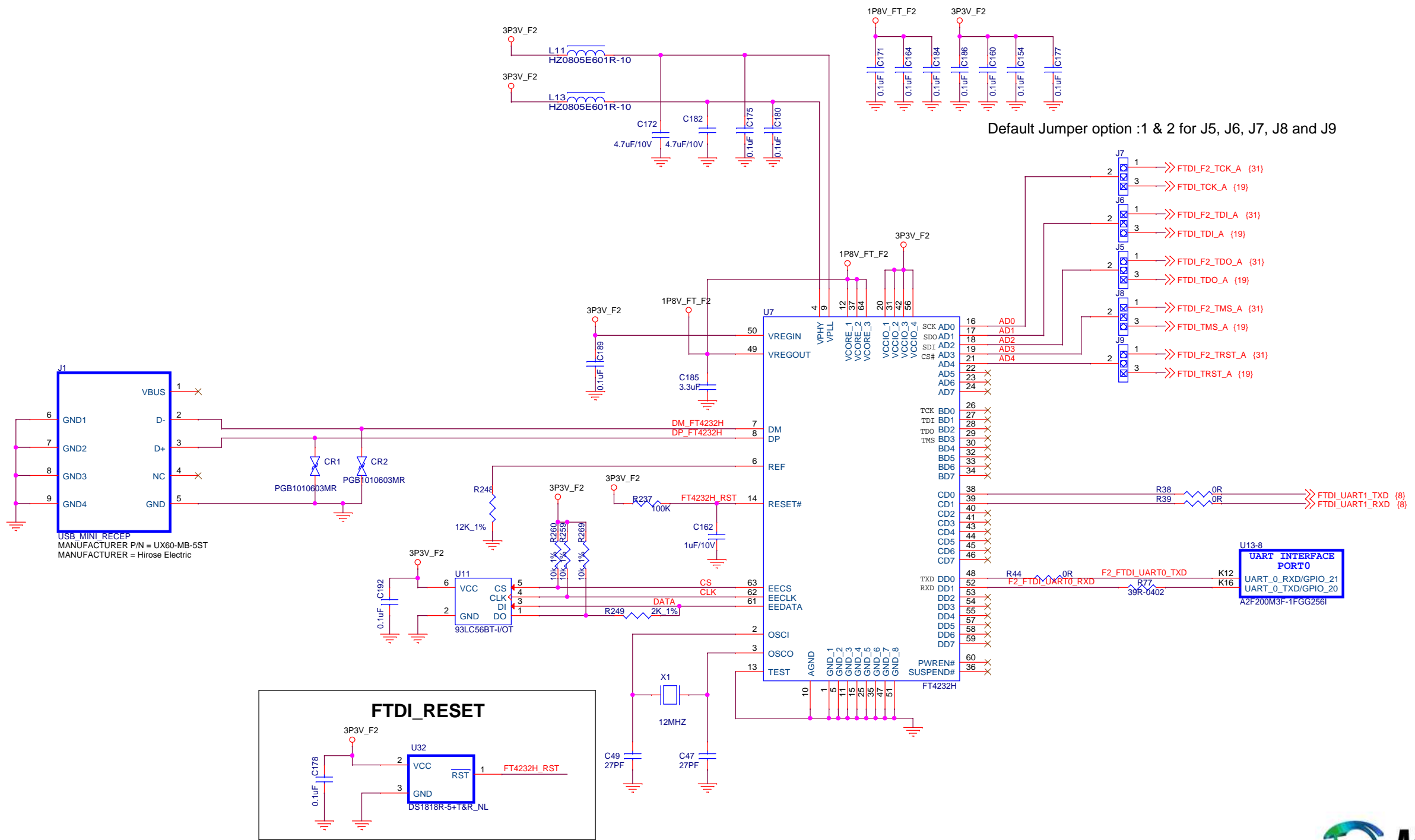
Polarfire Splash kit programming scheme



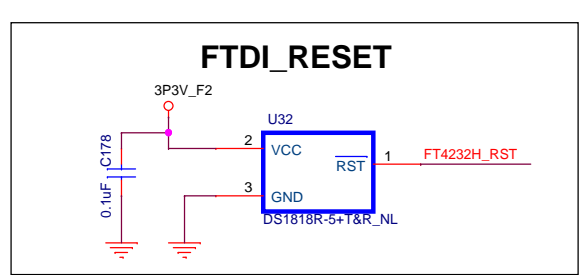
SR No	PROGRAMMING MODE	Jumper	
		J11	J10
1	JTAG Programming using Programming Header	OPEN	X
2	JTAG Programming using embedded Flash Pro5	SHORT 1-2	X
3	SPI Slave programming using embedded Flash Pro5	OPEN	OPEN
4	IAP programming	X	SHORT 1-2
5	Programming External SPI Flash using Programming Header	OPEN	SHORT 1-2
6	Programming External SPI Flash using Embedded JTAG	SHORT 1-2	SHORT 1-2



USB PROGRAMMING FT4232H INTERFACE

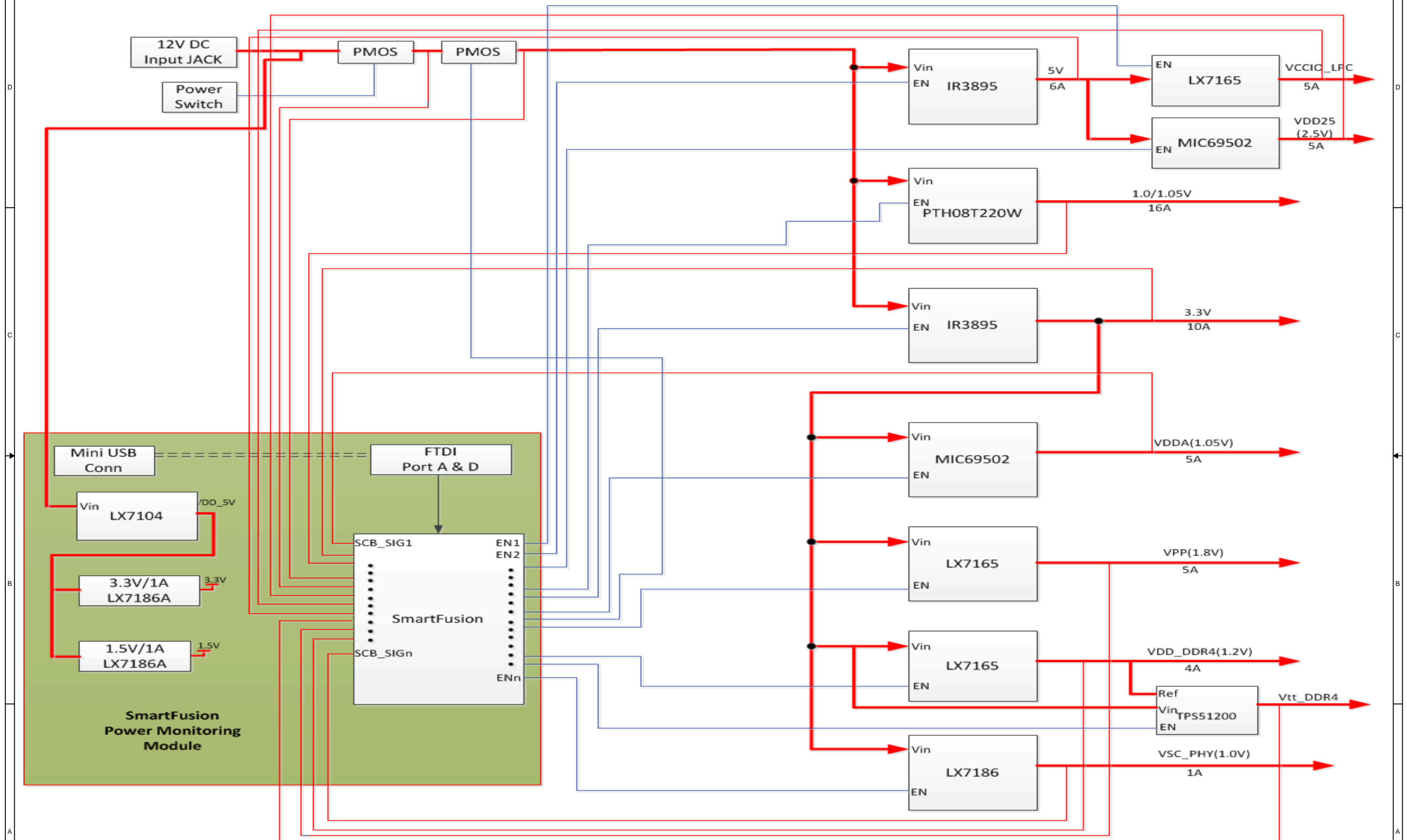


Default Jumper option : 1 & 2 for J5, J6, J7, J8 and J9



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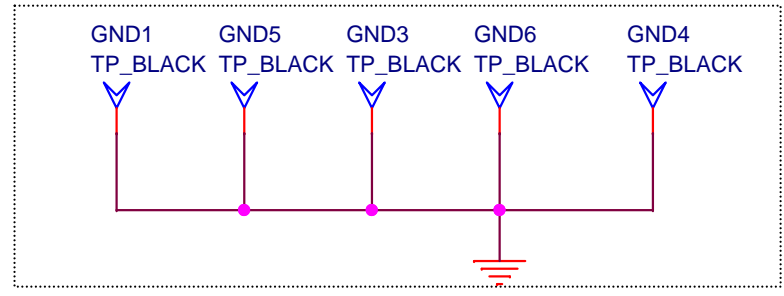
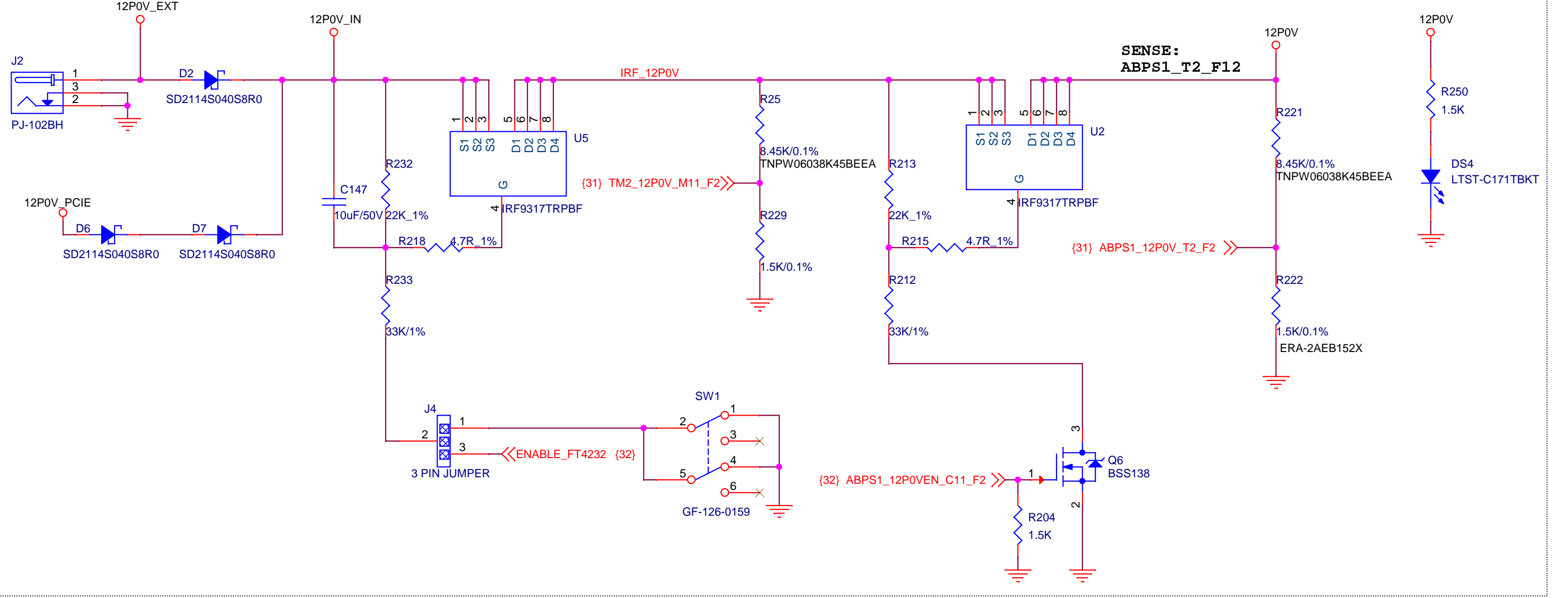
POWER AND MONITORING TOPOLOGY



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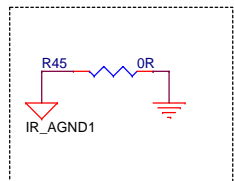
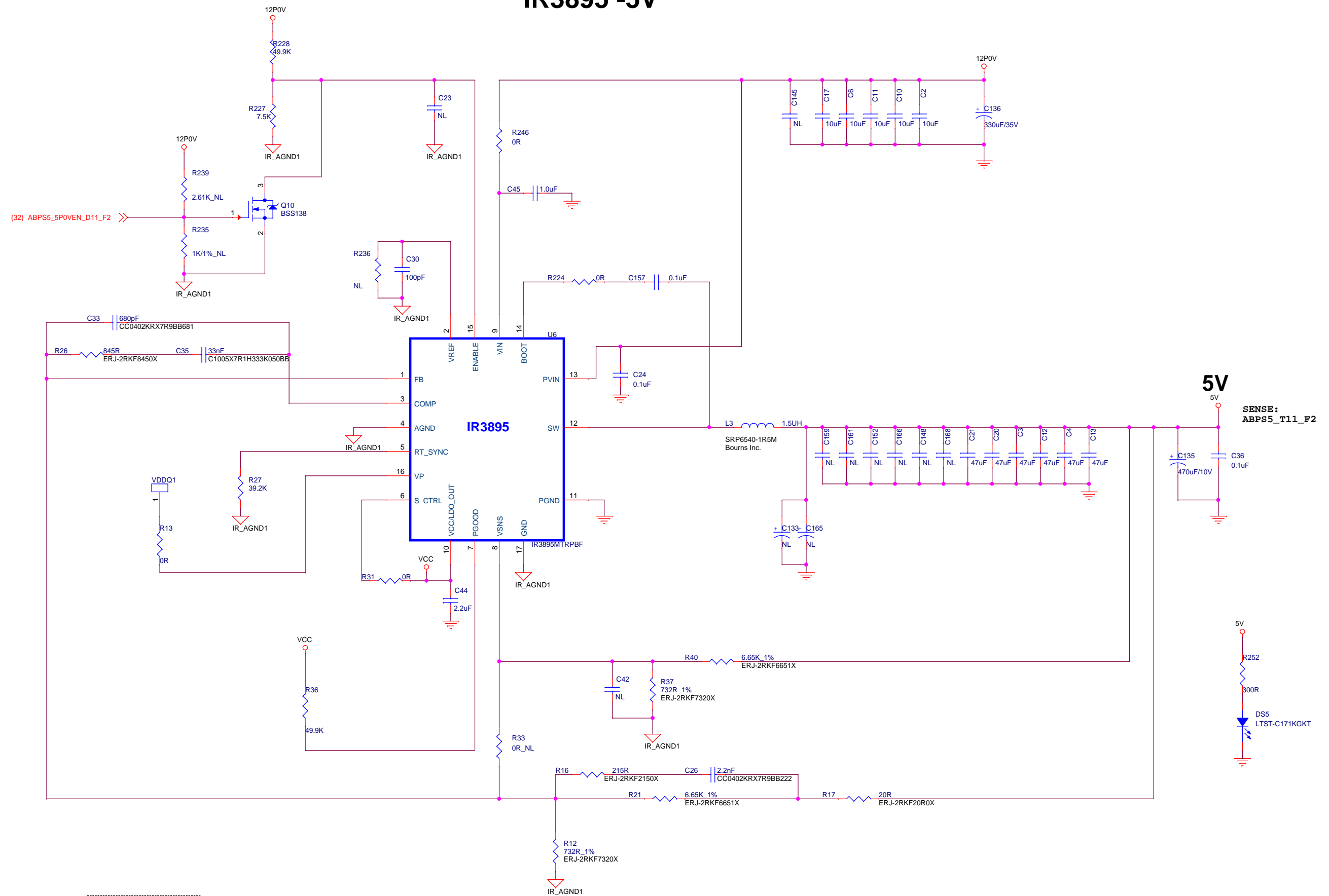


12V EXTERNAL SUPPLY



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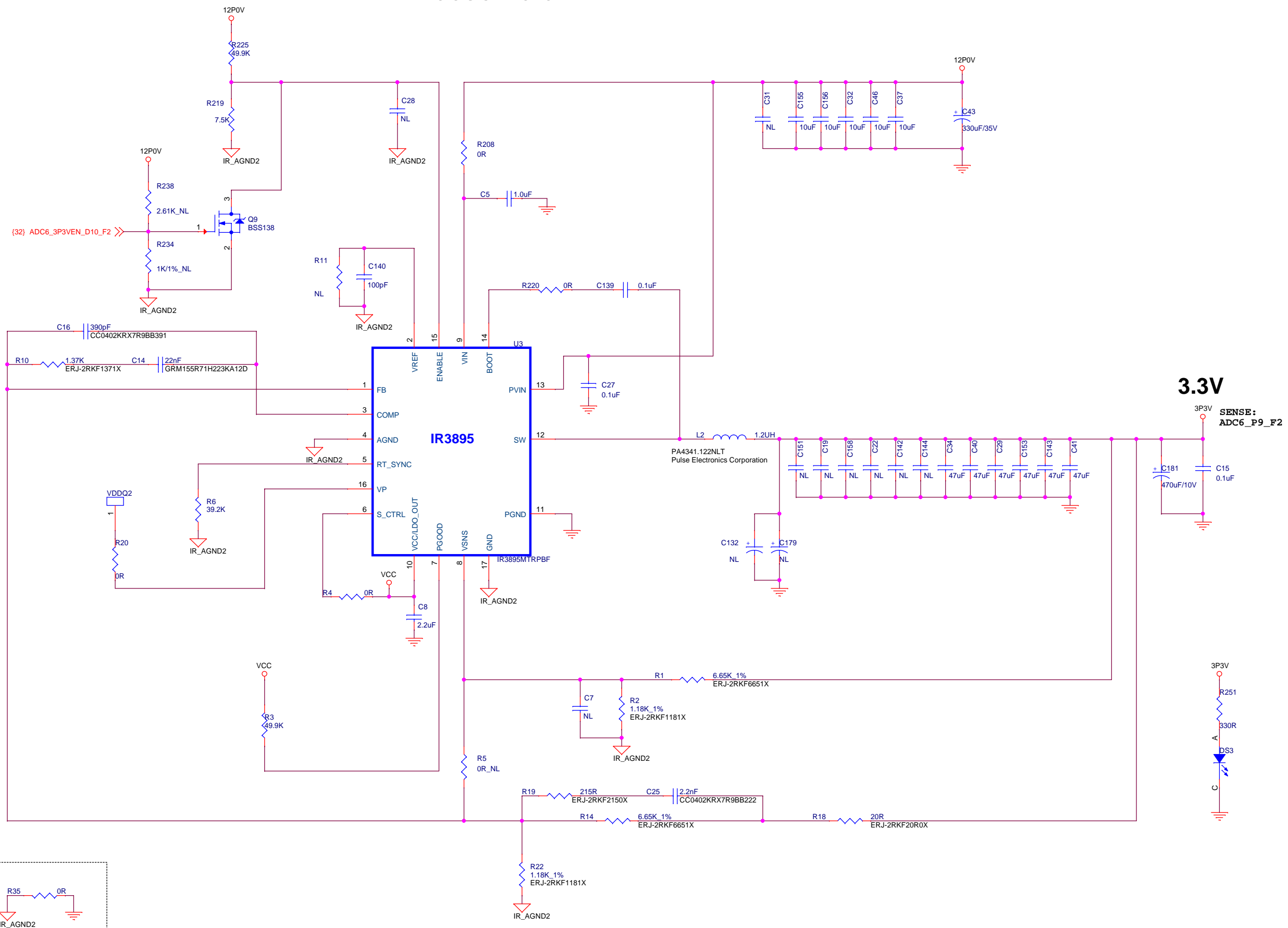
IR3895 -5V



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IR3895 - 3.3V

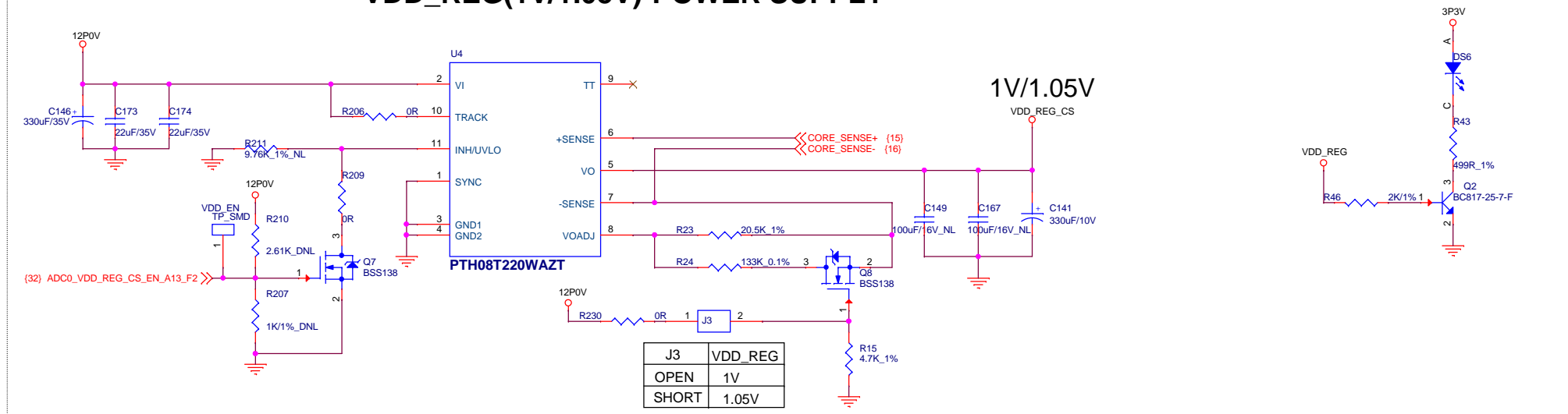


3.3V
SENSE: ADC6_P9_F2

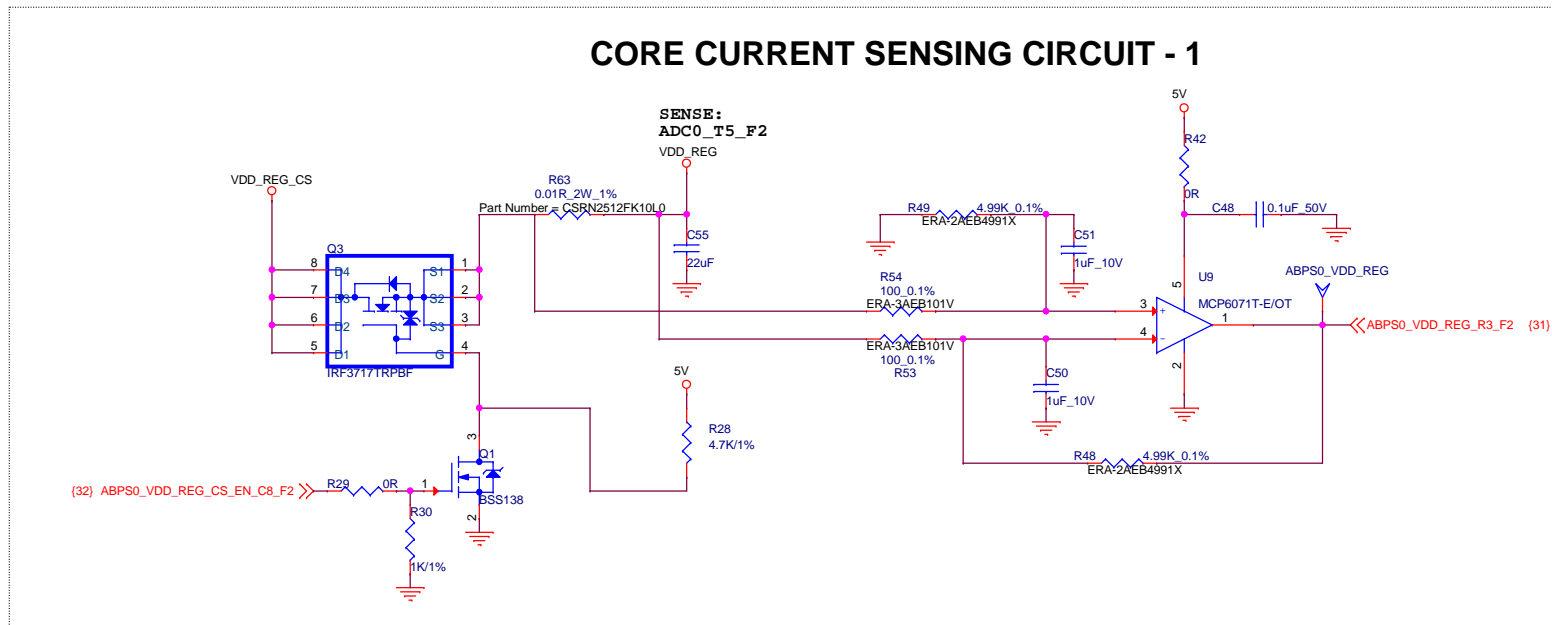
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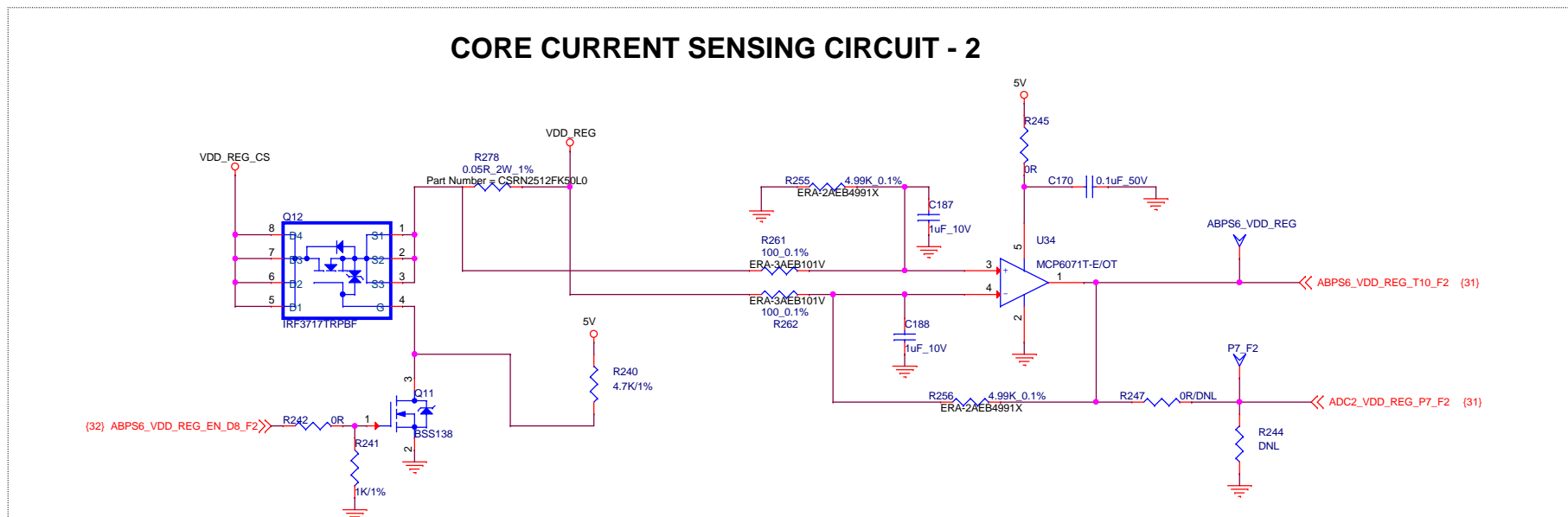
VDD_REG(1V/1.05V)-POWER SUPPLY



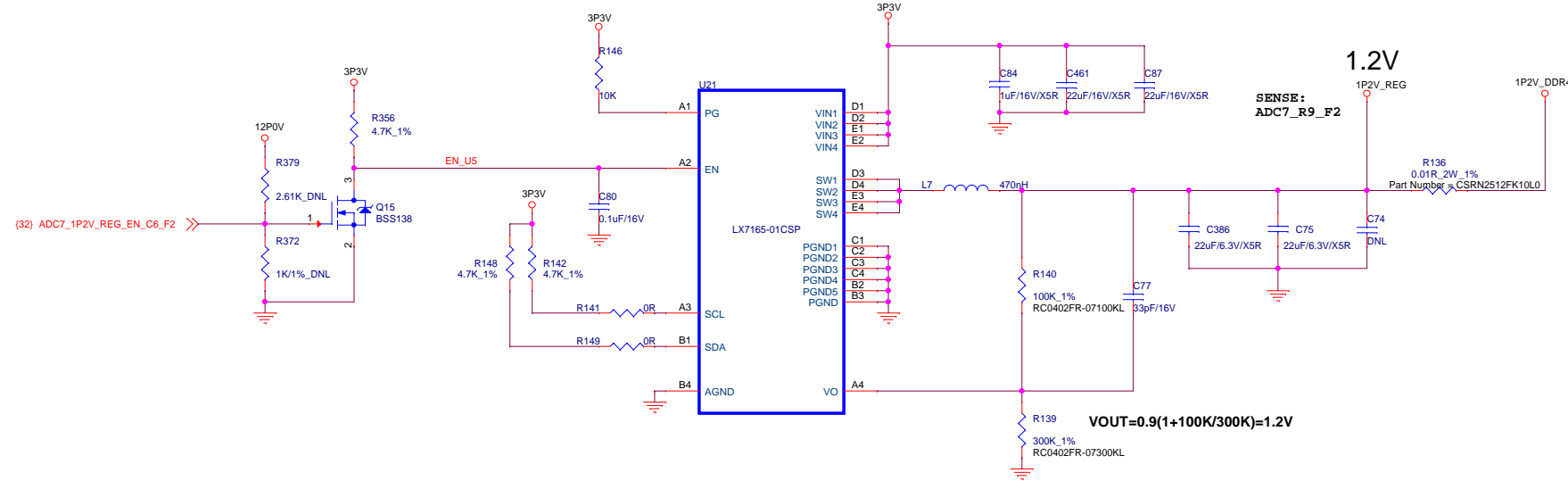
CORE CURRENT SENSING CIRCUIT - 1



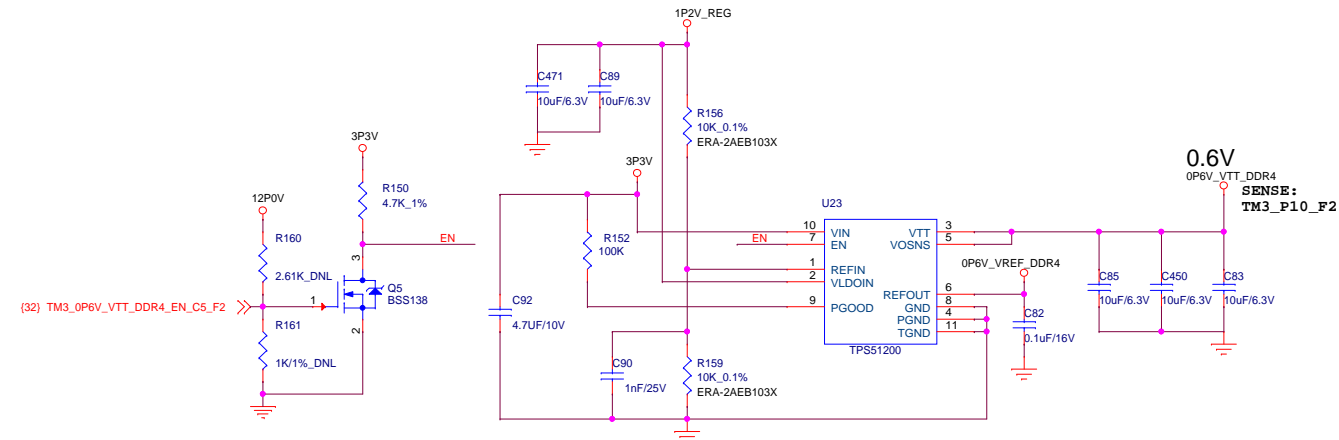
CORE CURRENT SENSING CIRCUIT - 2



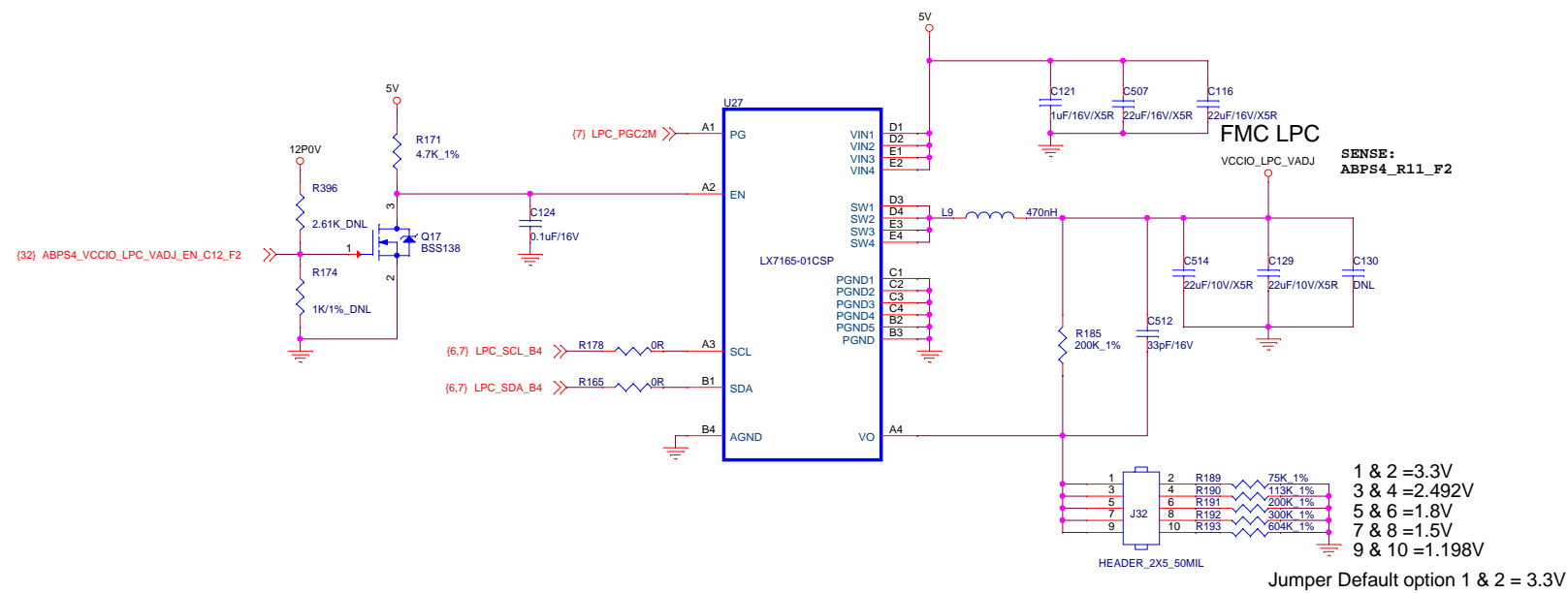
LX7165-01CSP- 1.2V



0.6V FOR DDR4 -VTT & VREF SUPPLY



LX7165-01CSP-FOR FMC LPC

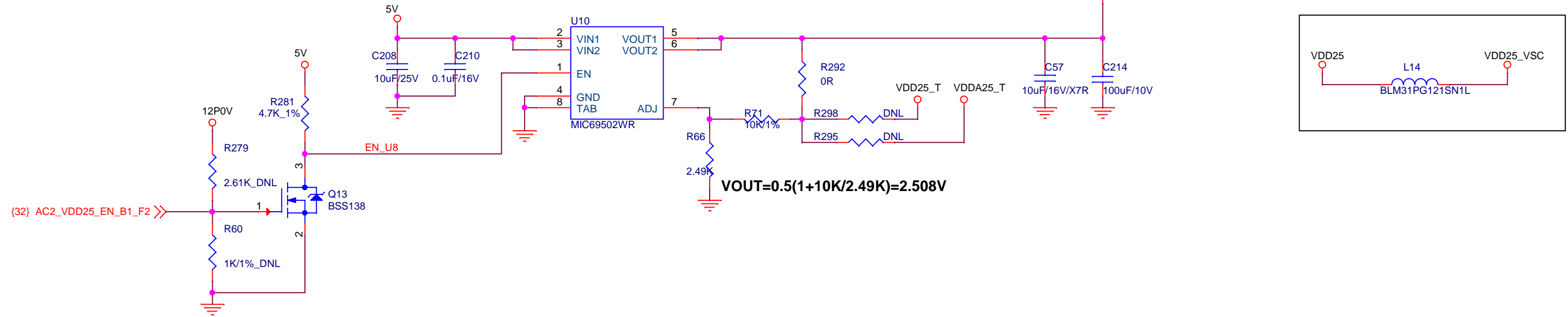


TITLE POLARFIRE SPLASH KIT			
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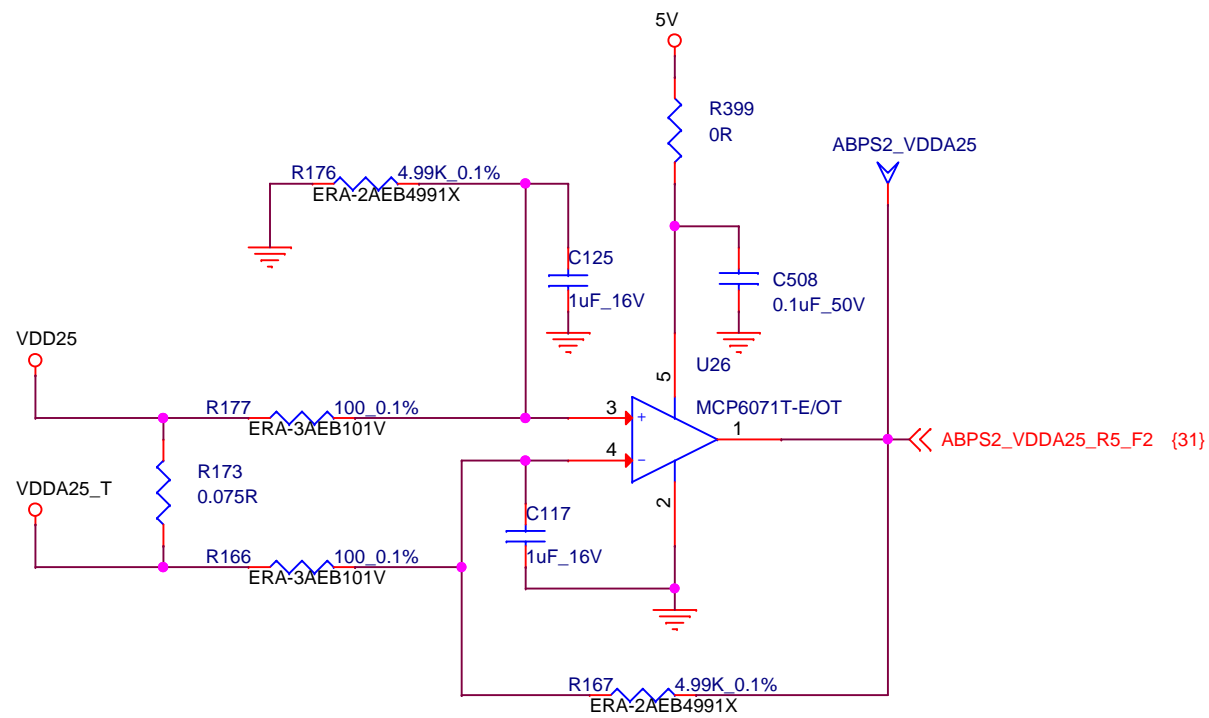
MIC69502WR-2.5V

2.5V

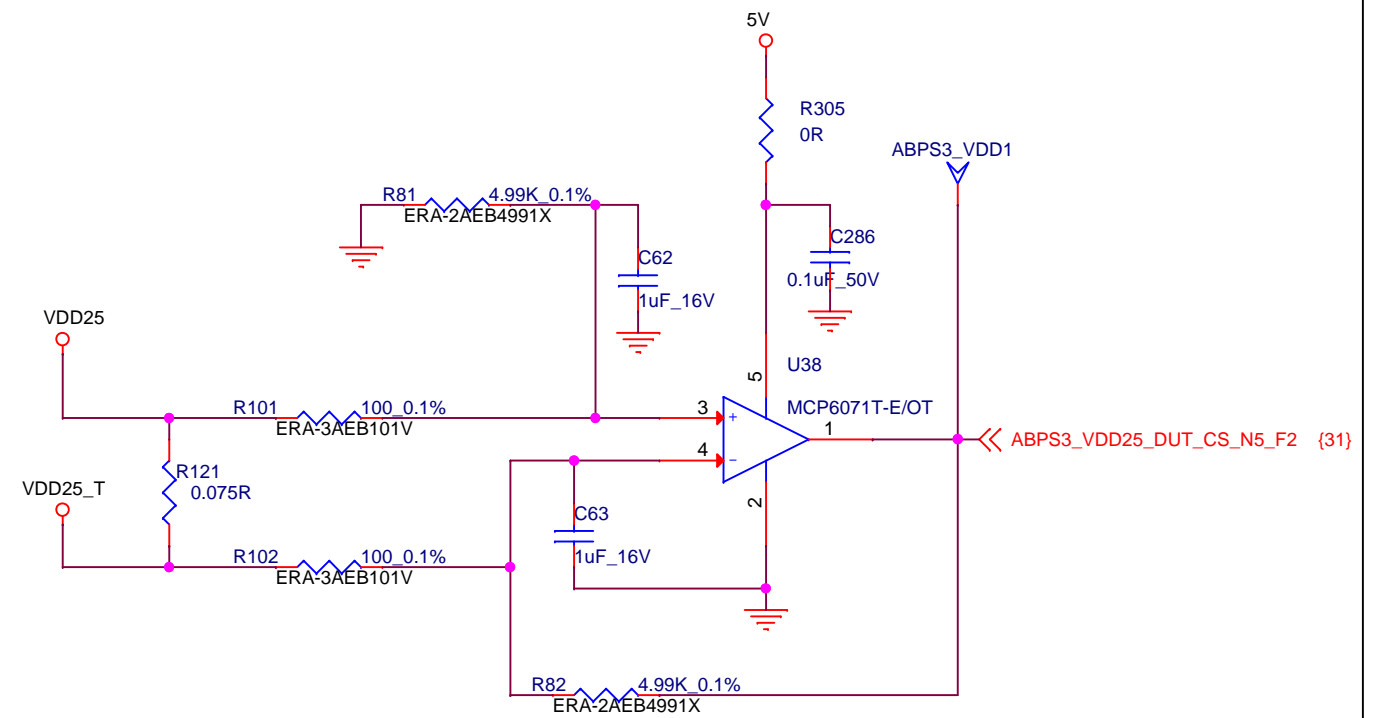
SENSE:
CM2_M12_F2



VDDA25 CURRENT SENSE CIRCUIT

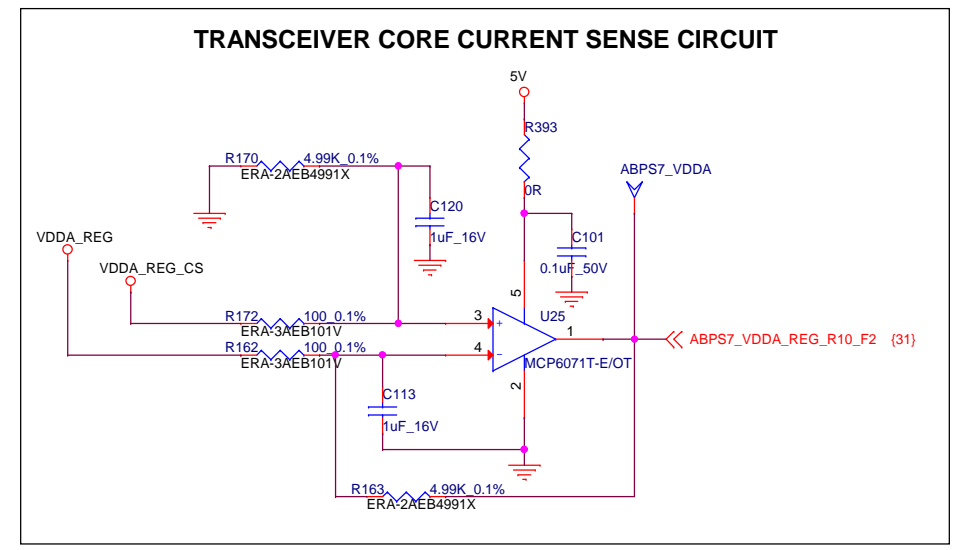
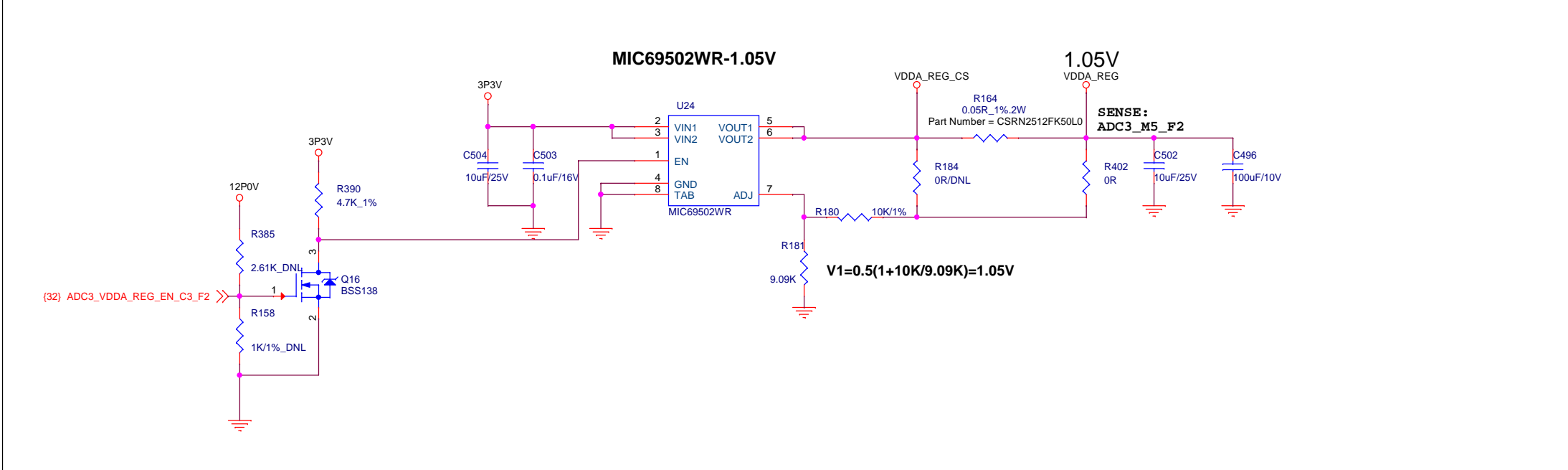
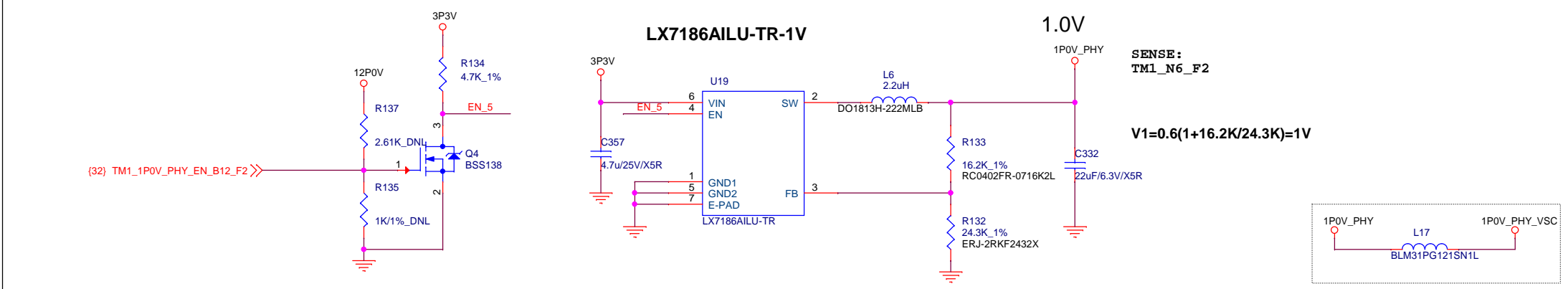
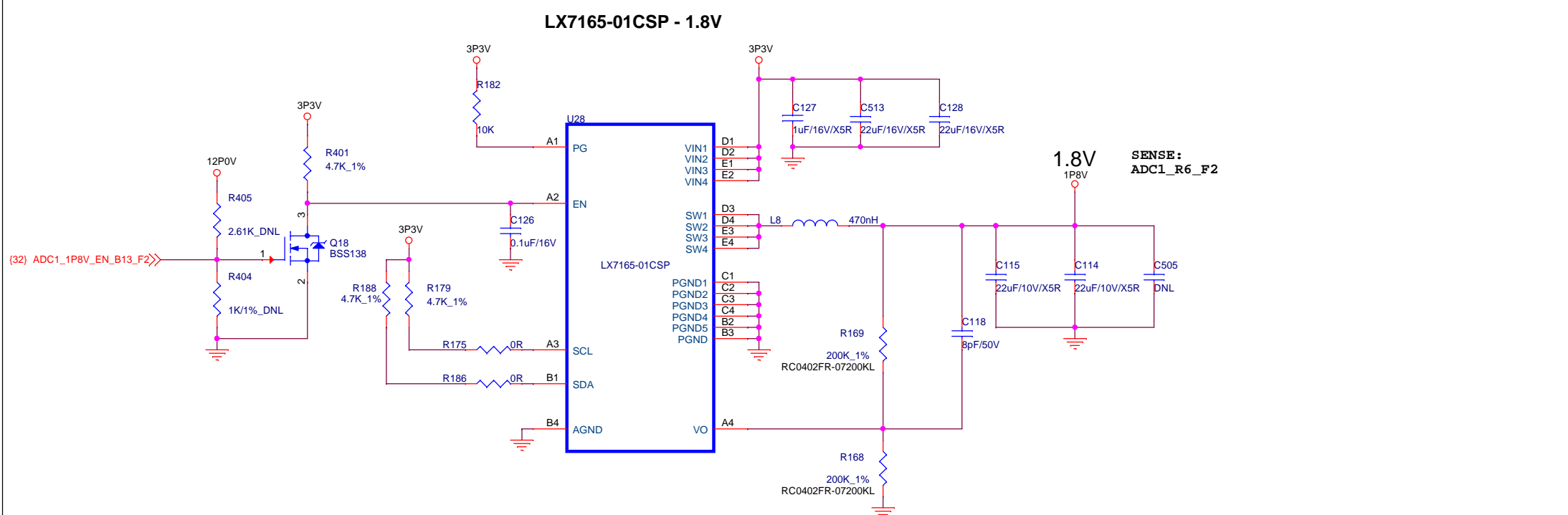


VDD25 CURRENT SENSE CIRCUIT



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"POWER SUPPLIES" - "1.05V", "1V" & "1.8V"



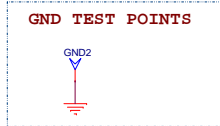
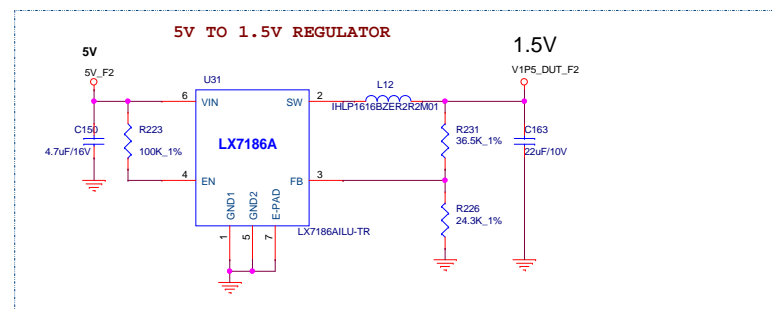
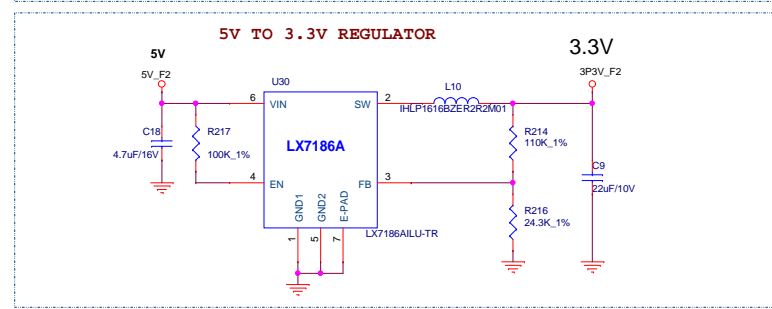
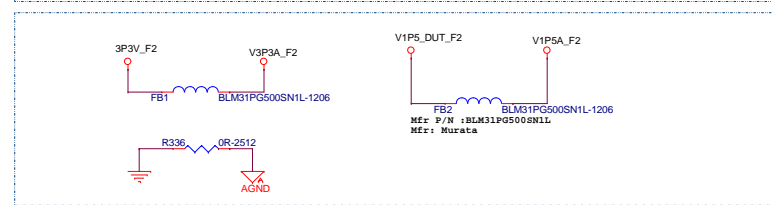
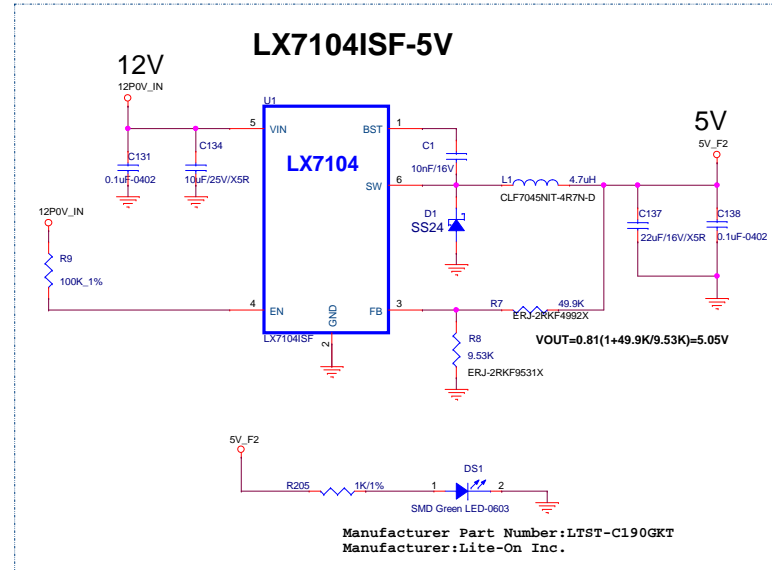
TITLE POLARFIRE SPLASH KIT		
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POWER MONITORING SOLUTION USING SmartFusion

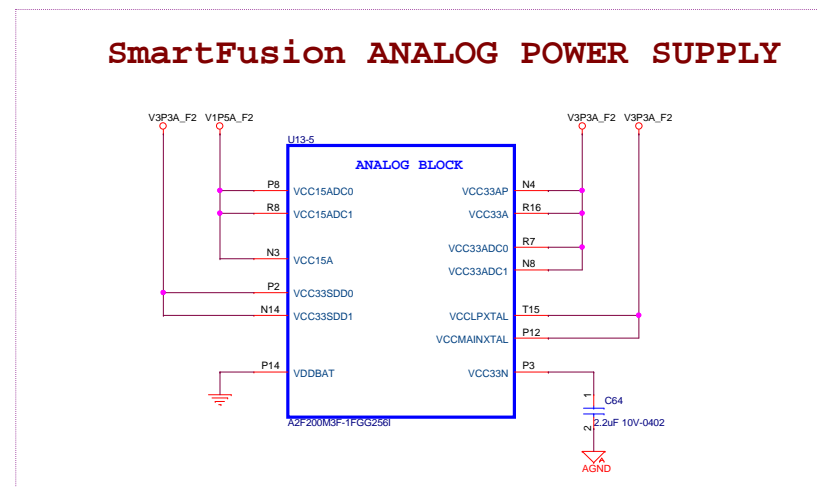
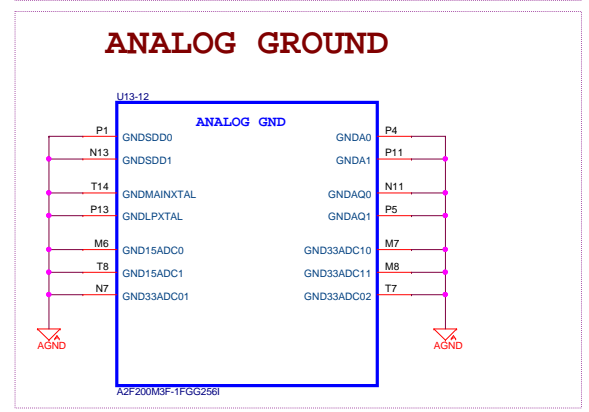
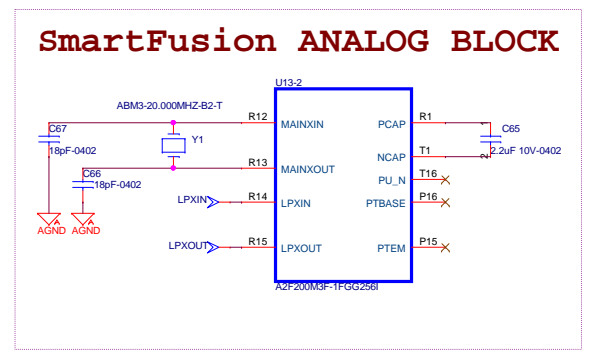


TITLE		
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Microsemi		
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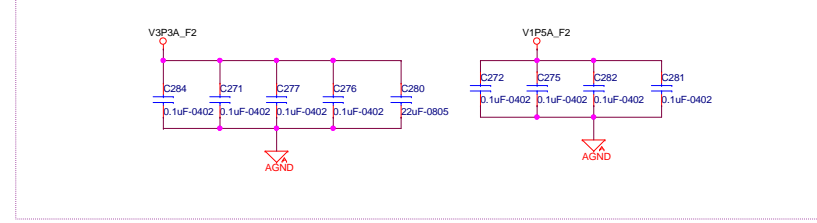
SmartFusion POWER SUPPLY



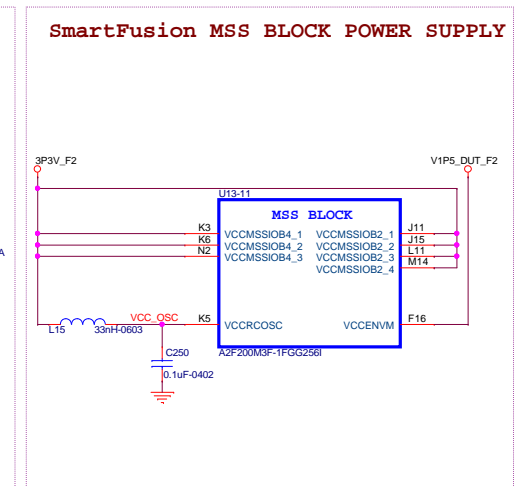
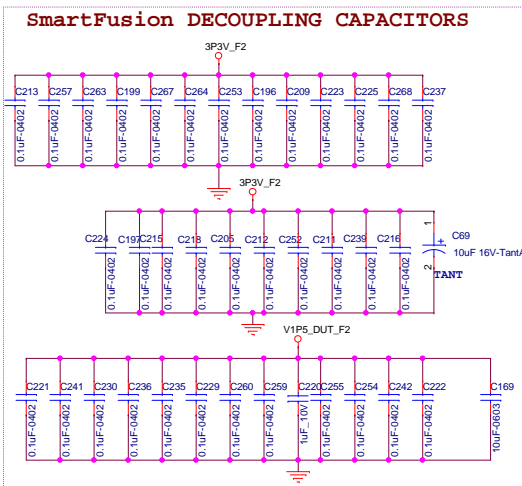
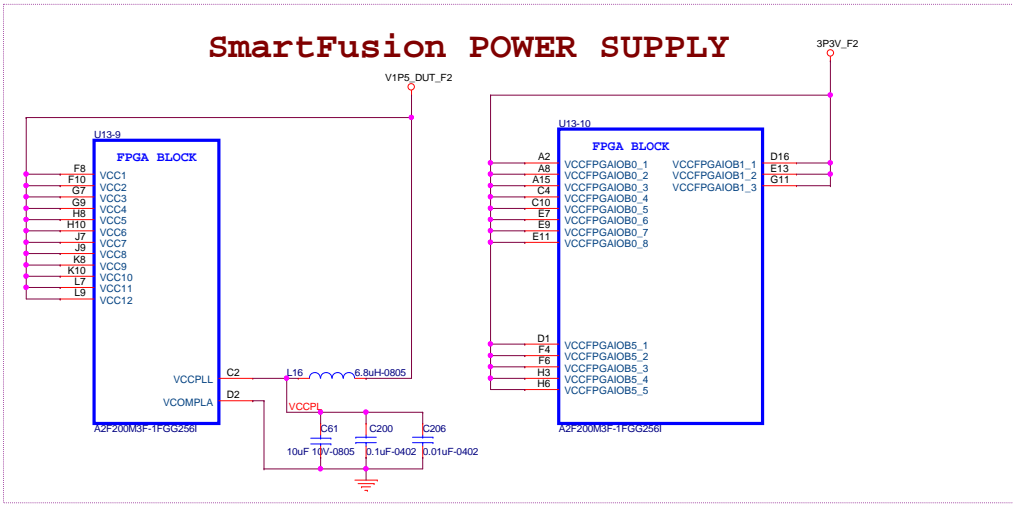
ANALOG PWR & GND



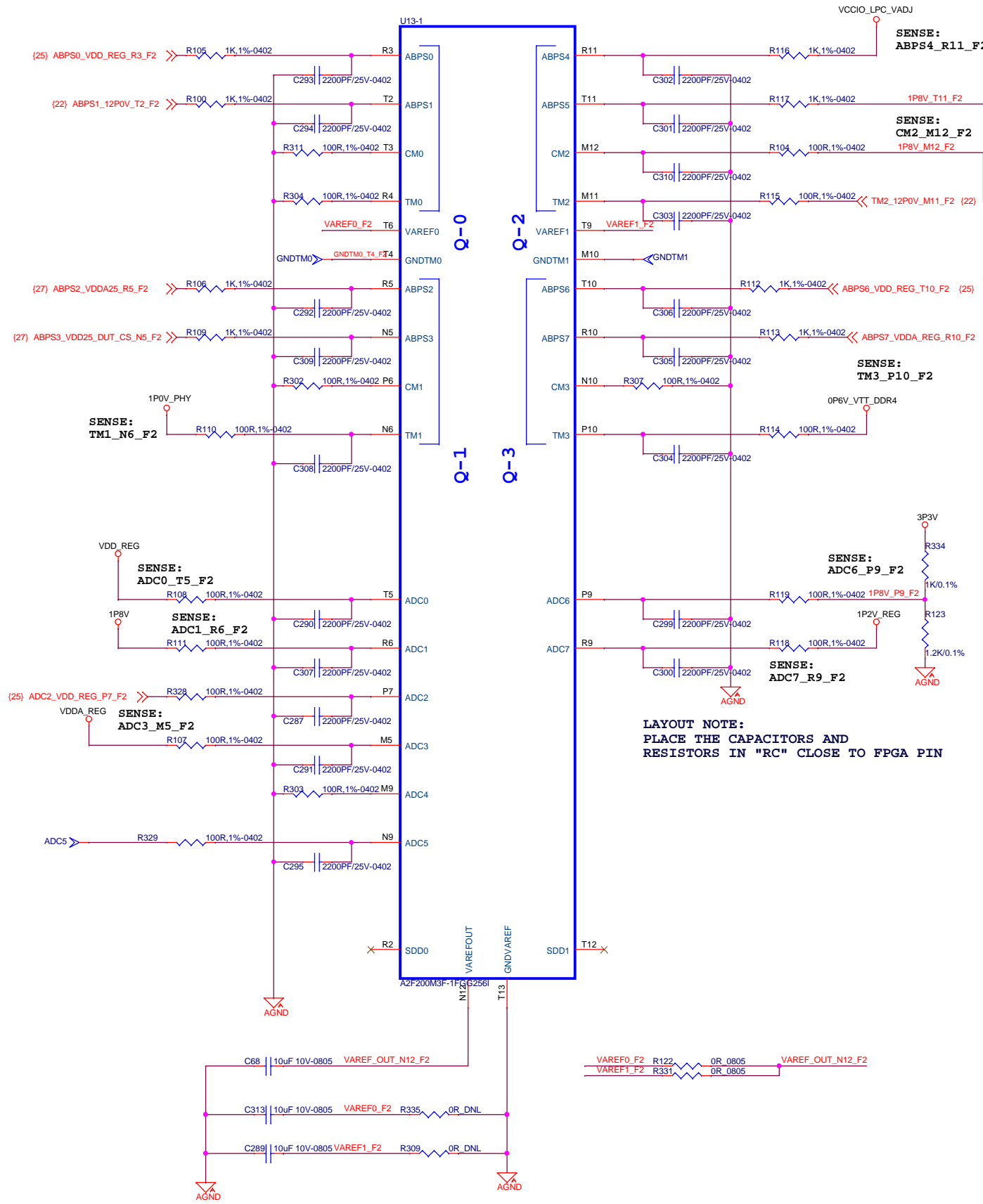
NOTE: PLACE ALL CAPS NEAR DUT BALLS



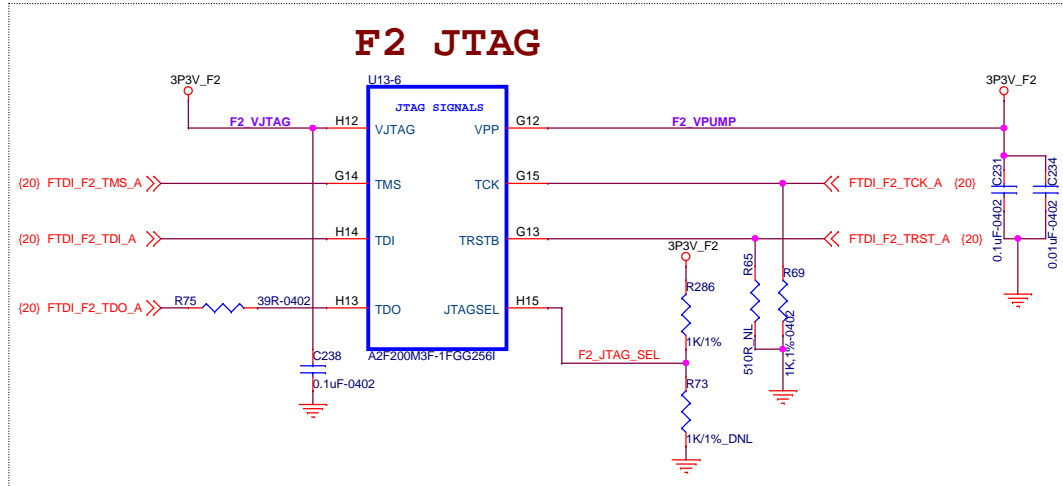
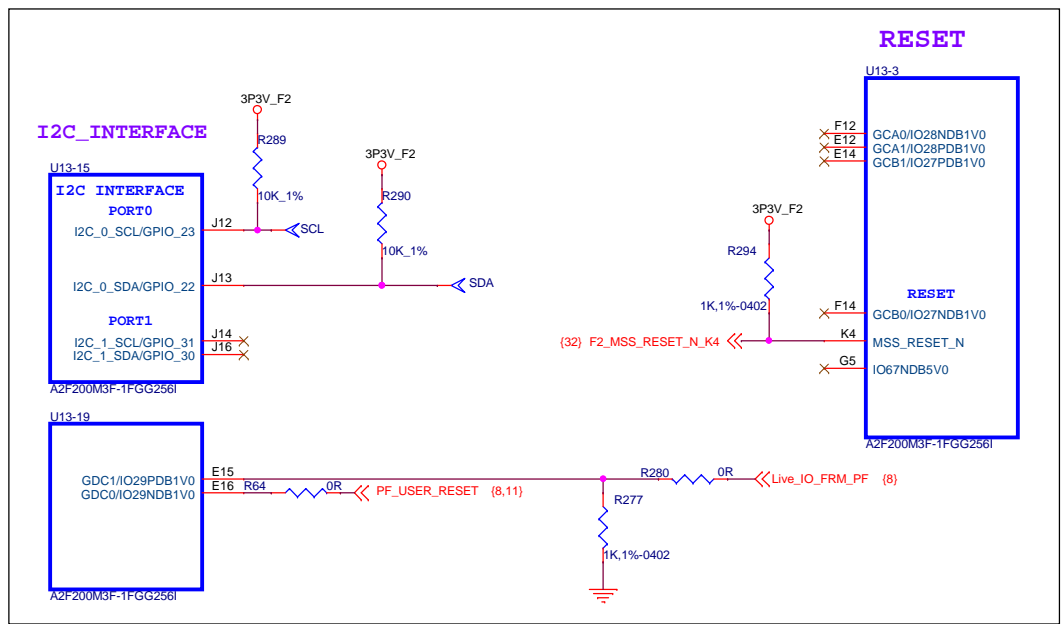
DIGITAL PWR & GND



ANALOG SIGNAL INTERFACE



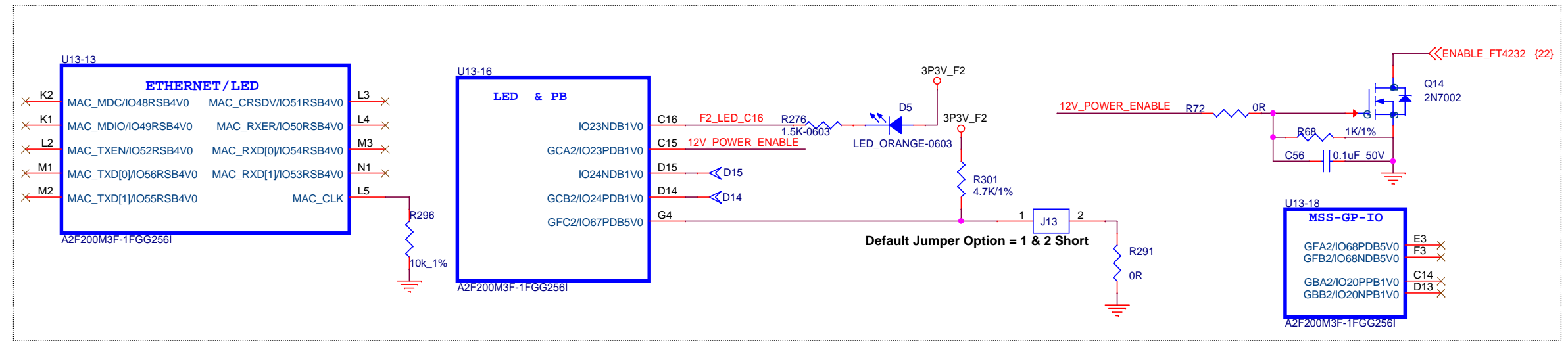
LAYOUT NOTE:
PLACE THE CAPACITORS AND RESISTORS IN "RC" CLOSE TO FPGA PIN



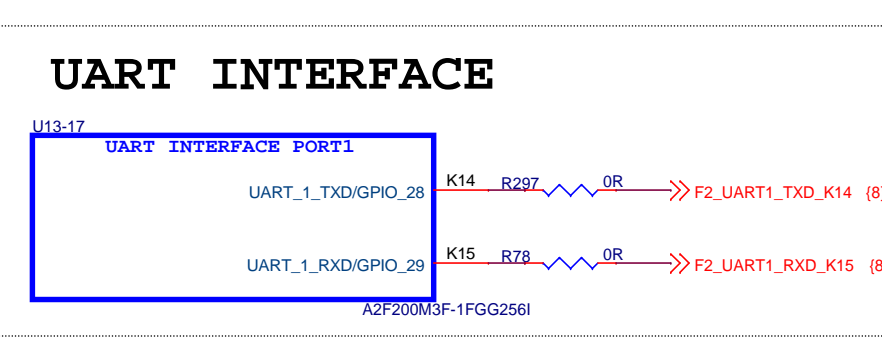
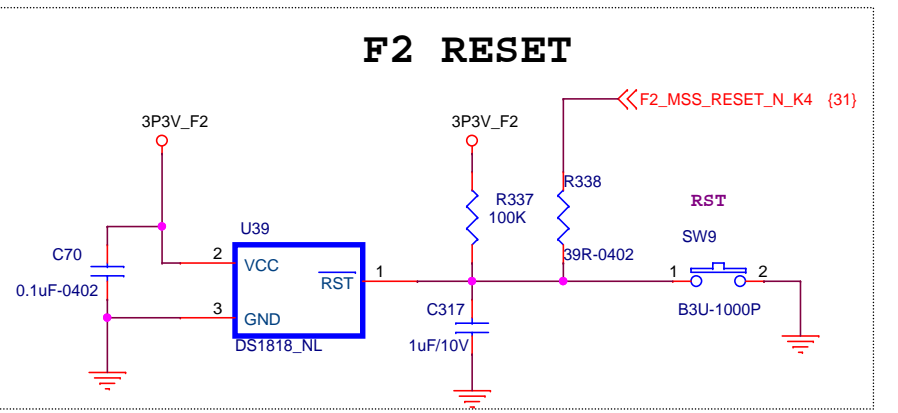
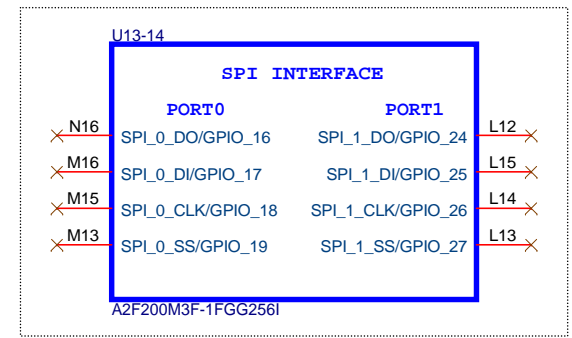
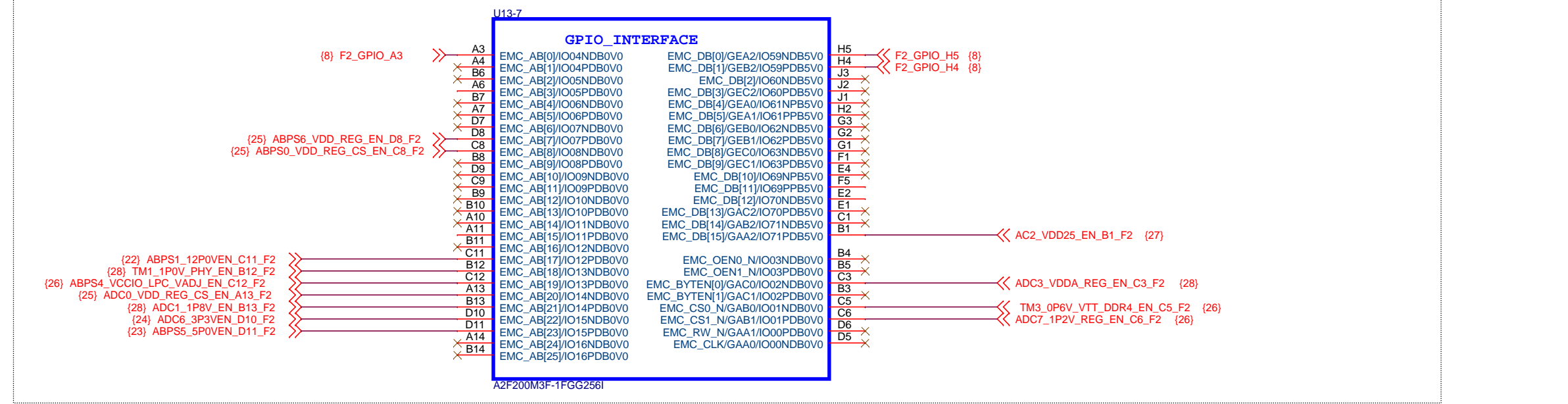
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USER DEBUG LOGIC



GPIO INTERFACE



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