ER0207

Errata

PolarFire FPGAs: Engineering Samples (ES) Devices

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 3.0

Revision 3.0 was published in January 2018. The following is a summary of changes made in revision 3.0 of this document.

- Re-applied errata item for VDDI3 and VDD_XCVR_CLK power supply limits as included in revision 1.0.
- Edited title of errata item for hot-swapping/cold sparing on erased devices to include unexpected driven pins. For more information, see ER0207 Errata Descriptions and Workarounds (see page 4).
- The errata is edited to remove DDR3 GPIO support for ES/XT devices. For more information, see Supported Memory Interfaces (see page 10).

1.2 Revision 2.1

Revision 2.1 of this document was published in January 2018. There were no changes to the technical content.

1.3 Revision 2.0

Revision 2.0 was published in November 2017. The following is a summary of changes made in revision 2.0 of this document.

- New errata items were added.
- Updated table to provide the availability of the errata item. For more information, see Summary of PolarFire FPGA Errata (see page 4).
- Added a note with a reference to the package pin assignment table. For more information, see Unsupported GPIO Pins on Erased Devices (see page 6).
- Updated re-programming failure using FlashPro errata item. For more information, see Re-programming Failure using FlashPro (JTAG Programming). (see page 8)
- The Transceiver Protocol and Memory Interface tables were added. For more information, see Supported Transceiver Protocols (see page 11) and Supported Memory Interfaces (see page 10).
- The following items from the Revision 1.0 errata were removed, as they were found to no longer be an issue in -ES devices or with PolarFire v2.0 software improvements.
  - PCIe AXI slave interface has lower than expected throughput
  - Transaction layer clock behavior of PCIe clock
  - CCC-PLL lock output can glitch after reset has occurred using DEVRSTN pin
  - LSRAM read before write (RBW) mode

1.4 Revision 1.0

Revision 1.0 was published in June 2017. It was the first publication of this document.

2 Errata for PolarFire Engineering Samples

The PolarFire® FPGA family engineering samples (ES) are subject to the limitations described in this errata. This document contains updated information about any known engineering sample-specific issues and provides the available limitations and workarounds. Engineering sample issues identified in this errata will be corrected in subsequent revisions of the devices listed in the following table. This errata highlights dependencies between silicon device revisions and specific support by Libero PolarFire SoC software versions. Contact Microsemi Technical Support for more information.

2.1 Sample Revisions

The following table lists the sample revisions released. Errata items impact all ES revisions listed unless specified otherwise.

Table 1 • Sample Revisions Released per Device

Devices	Packages	Revisions
MPF300T	FCG1152, FCG784, FCG484, FCVG484, and FCSG536	0, 1, 2, 3

The following table lists the operating conditions for the PolarFire engineering samples. The operating conditions for production devices will follow datasheet specifications.

Table 2 • PolarFire Engineering Sample Operating Conditions

Operation Temperature Range	Program/Erase	Retention Lifetime	sNVM Endurance	FPGA Endurance
0 °C to 50 °C[1]	20 °C to 50 °C	1 year	1000 cycles	200 cycles

1. T_J = Junction temperature.
2. These operating conditions are for engineering samples only. Refer to DS0141: PolarFire FPGA Datasheet for production specifications.

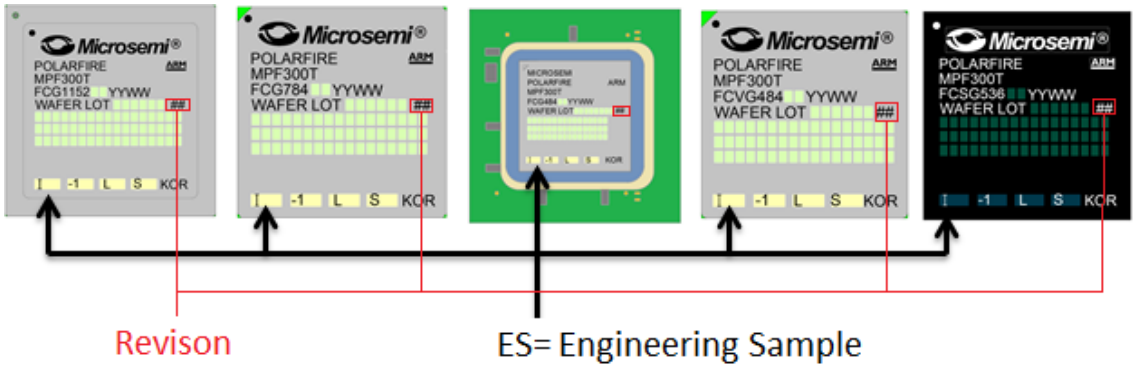
2.2 PCB Designs

For information about how to determine proper signal pinout, see UG0726: PolarFire FPGA Board Design User Guide. The proper signal pinout is required for all clocking, transceiver, and FPGA pin recommendations.

2.3 Engineering Sample Device Identification

PolarFire FPGA engineering samples can be identified by the temperature grade field in the lower left hand corner. As the following illustration shows, an ES annotation will appear in the temperature grade field indicating device is engineering sample and revision marking is shown along right side of code mark.

Figure 1 • ES Identification Markings



3 Errata Descriptions and Workarounds

The following sections provide a description of device errata and workarounds (when applicable).

The following table lists the specific device errata and the affected PolarFire ES devices. For die revision part marking specification, see ES Identification Markings (see page 3).

Table 3 • Summary of PolarFire FPGA Errata

Description	Silicon Revisions				Errata Removal Details
	MPF300T				
	0	01	2	3	
Power supply sequencing	*	*	*	*	
Bank3 VDDI, VDD_XCVR_CLK and XCVR_VREF[1:2] reduced from specification	*	*	*	*	
Hot-swapping/cold sparing support on any I/Os powered by VDDI3 or XCVR_CLK_VDD banks	*	*	*	*	
Hot-swapping/cold sparing on erased devices/unexpected driven pins	*	*	*	*	
Calibration of FPGA I/O buffers	*	*	*	*	
SmartDebug active probe speed	*	*	*	*	
Missing global clock connection in XCVR Quad1	*	*	*	*	
Inefficient usage of asynchronous dual-port LSRAM blocks	*	*	*	*	
GPIO IOCDR SGMII	*	*	*	*	
SmartDebug active probe write	*	*	*	*	
PCIe core initialization	*	X	X	X	Libero SoC PolarFire v1.1 SP1 is required
HSIO and GPIO drive strength	*	*	*	*	
PCIe transmit compliance with a 50 Ω load	*	*	*	*	
Voltage reference sensitivity issue	*	*	*	*	
LVDS VOS output common mode specification	*	*	*	*	
V_{DD} power estimation	*	*	*	*	
Re-programming failure using FlashPro (JTAG programming)	*	X	X	X	Libero SoC PolarFire v1.1 SP1 is required
GPIO on-die termination	*	*	*	*	Libero SoC PolarFire v2.0 provides updated termination settings for ES devices
Transceiver polarity inversion	*	*	*	*	
Lanes 2 and 3 are swapped between PCS to FPGA fabric	*	*	X	X	Libero SoC PolarFire v2.0 required to correct issue
JTAG programming times	*	*	*	*	
PCIe after asserting the PCIE_PERST_N port	*	*	*	*	
SSTL18I I/O standard is not supported for PF_XCVR_REF_CLK	*	*	*	*	
PCIe ECC detection	*	*	*	*	
JTAG TCK duty cycle	*	*	*	*	
Transceiver PCS mode 64b/6xb limitations	*	*	*	*	

Description	Silicon Revisions				Errata Removal Details
Transceiver lock to reference clock limitation	*	*	*	*	
Limitations for ACJTAG IEEE 1149.6 for transceiver transmit pins	*	*	*	*	
Incorrect transceiver LANEx_RX_READY pin behavior	*	*	*	*	
Unsupported Features					
System controller suspend mode	*	*	*	*	
Flash*Freeze mode	*	*	*	*	
Temperature voltage sensor (TVS)	*	*	*	*	
Device zeroization	*	*	*	*	
Digest check	*	*	*	*	
Generic I/O gearing modes	*	*	*	*	
PCIe Gen2 electrical compliance for x2 and x4 links	*	*	*	*	
Automated DFE support (contact factory)	*	*	*	*	
XCVR limitations for entire data rate range (contact factory)	*	*	*	*	
Feature Clarifications					
Memory interfaces	List of currently supported memory interfaces with ES devices and Libero PolarFire SoC V2.0 software				
Supported transceiver protocols	List of currently supported transceiver protocols with ES devices and Libero PolarFire SoC V2.0 software				

Note: * indicates that the errata exists for that particular device and revision number.

Note: X indicates that the errata is removed and no longer exists for that particular device and revision number (based on additional details).

3.1 Power Supply Sequencing

The engineering sample must follow this power-on sequence:

1. V_{DD} to V_{DD} operational minimum
2. V_{DD25} to V_{DD25} operational minimum
3. V_{DDI} and V_{DDAUX} must be powered up any time before V_{DD18} or simultaneously with V_{DD18} if supplied from same power source. If V_{DDI} and V_{DDAUX} are not tied to same voltage rail, then V_{DDI} should be powered up before V_{DDAUX}.
4. V_{DD18} (V_{PP}) must be the last major supply in the power-up sequence. Other supplies that are not mentioned, such as power supplies related to transceivers, do not have mandatory sequence requirements.

The V_{DD25} power-supply can draw large currents at power-up or power cycling if the correct sequence is not followed.

For more information about the operational minimum voltages, see the DS0141: PolarFire FPGA Datasheet. Observe the power supply ramp rates specified in the datasheet.

Sequencing will not be required for production MPF300T devices.

3.2 Bank3 VDDI, VDD_XCVR_CLK and XCVR_VREF[1:2] reduced from specification

Bank 3 VDDI, VDD_XCVR_CLK and XCVR_VREF[1:2] cannot exceed 2.5 V nominal.

3.3 Hot-Swapping/Cold Sparing Support on any I/Os Powered by VDDI3 or XCVR_CLK_VDD Banks

This feature is not supported on any I/Os powered by V_{DDI3} or the transceiver reference clock input pins, including:

- SDO
- SDI
- FF_EXIT_N
- IO_CFG_INTFK
- SPI_EN
- SCK
- DEVRST_N
- SS
- TCK
- TMS
- TDI
- TDO
- TRSTB
- XCVR_#A_REFCLK_P/N
- XCVR_#B_REFCLK_P/N
- XCVR_#C_REFCLK_P/N

There is no workaround for this issue.

3.4 Hot-Swapping/Cold Sparing on Erased Devices/Unexpected Driven Pins

The following table lists the 35 GPIO pins that do not support hot-swapping/cold sparing on erased devices.

Table 4 • Unsupported GPIO Pins on Erased Devices

Bank	GPIO Pins
0	HSIO169PB0, HSIO170PB0, HSIO171PB0, HSIO173NB0
1	HSIO72NB1, HSIO73PB1, HSIO74PB1, HSIO75PB1, HSIO79PB1, HSIO80PB1, HSIO81PB1
2	GPIO244NB2, GPIO246PB2, GPIO247PB2, GPIO248PB2, GPIO26PB2, GPIO27PB2, GPIO28PB2, GPIO32PB2, GPIO33PB2, GPIO34PB2, GPIO35NB2
4	GPIO174PB4, GPIO180PB4, GPIO181PB4
5	GPIO238PB5, GPIO239PB5, GPIO241PB5
6	HSIO62PB6, HSIO63PB6, HSIO64PB6, HSIO68PB6, HSIO69PB6, HSIO70PB6, HSIO71NB

Note: This errata is only applicable to erased parts. Programmed parts do not have the errata. If these pins are used as input or bi-directional buffers, an erased device will actively drive these outputs rather than being properly disabled. For more information about the pin numbers, see the MPF300T /MPF300TS package pin assignment table at https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga.

If the part is not programmed, do not use these pins if required for hot-swapping/cold sparing applications.

3.5 Calibration of FPGA I/O Buffers

The FPGA I/O buffers have calibration circuitry to optimize and match the I/O impedance and termination within a system. The calibration occurs every time the device is powered up. After the device power-up, re-calibration is not available on command.

The device requires a power-cycle to correctly re-calibrate.

3.6 SmartDebug Active Probe Speed

The live probe output cannot toggle faster than 100 MHz.

There is no workaround for this issue.

3.7 Missing Global Clock Connection in XCVR Quad1

Designs cannot utilize two global clocks for XCVR Quad1. Designs have access to only one global clock on Quad1.

In the Libero® SoC PolarFire transceiver lane configurator, the user can select the clock resources used for transmit, receive and global or regional clocks. For lanes assigned to Quad1, only a single global connection is available. This implies that only one lane in that quad and one direction of that lane can select global in this interface. Therefore, the clocks assigned to LANE#_RX_CLK_[G] & LANE#_TX_CLK_[G] are limited to one across all lanes in a quad.

3.8 Inefficient Usage of Asynchronous Dual-Port LSRAM Blocks

For LSRAM blocks configured as asynchronous dual-ports when port A is greater than x20, twice the number of required LSRAM blocks are used.

Two 1K × 20 LSRAM blocks are automatically instantiated by Libero SoC PolarFire to implement the single 512 × 40 LSRAM.

3.9 GPIO IOCDR SGMII

IOD CDR interfaces cannot be used with a >0 ppm offset. For SGMII, the PHY device and PolarFire IOD CDR must use the same reference clock. SGMII interfaces using transceivers are not affected by this limitation.

SGMII can be implemented with IOCDR using 0 ppm or a common clock using the same clock configuration for both Tx and Rx clocks.

3.10 SmartDebug Active Probe Write

SmartDebug Active Probe write operation is not available. Active Probe read operation functions as documented.

There is no workaround for this issue.

3.11 PCIe Core Initialization

PCIe is not correctly initialized after programming the device.

Impacts only silicon revision 0 and software prior to Libero PolarFire V1.1 SP1.

3.12 HSIO and GPIO Drive Strength

HSIO and GPIO drive strength deviates by up to ±20% from the datasheet specifications.

There is no workaround for this issue.

3.13 PCIe Transmit Compliance with a 50 Ω Load

PCIe fails to automatically enter into transmit compliance when used with a 50 Ω load.

There is no workaround for this issue.

3.14 Voltage Reference Sensitivity Issue

There is a voltage reference sensitivity issue with HSIOs when V_{DD18} and V_{DD25} supply voltage rail separation is too large. This effects the HSIO buffer banks only.

This issue is managed by reducing the separation between V_{DD25} and V_{DD18}. For example, when V_{DD25} is maximum, then V_{DD18} needs to be maximum or when V_{DD25} is typical, then V_{DD18} needs to be typical. If V_{DD18} and V_{DD25} are minimum and the other maximum (respectively), it will influence the effectiveness of the voltage references of the HSIO banks, preventing I/O buffers from correctly functioning.

3.15 LVDS VOS Output Common Mode Specification

The LVDS VOS output common mode specification can vary as much as 175 mV below the datasheet specification.

3.16 VDD Power Estimation

The PolarFire power estimator (v3e) is currently optimistic with regard to the estimated V_{DD} static power. It is expected that designs utilizing ES silicon can have a 40% higher current on the V_{DD} power supply compared to the provided estimation.

3.17 Re-programming Failure using FlashPro (JTAG Programming)

Designs that have stored device initialization in µPROM or external SPI will fail reprogramming with FlashPro and receive the following error message: "Error: programmer 'S201Z7FK2R': Executing action PROGRAM FAILED, EXIT -38."

The error condition can be cleared by re-attempting programming. This issue is only identified in MPF300-ES Rev0 devices.

3.18 GPIO On-Die Termination

The on-die pull-up of the Thévenin's termination can be as high as 2x. This causes a weak ODT termination.

The user can select a stronger termination value for the design. This issue is automatically adjusted with Libero PolarFire V2.0 software.

3.19 Transceiver Polarity Inversion

There is no programmable receiver polarity inversion possible on the transceivers for 8b10b, 64b6xb, and PMA modes.

There is no workaround for this issue.

3.20 Lanes 2 and 3 are Swapped Between PCS to FPGA Fabric

This effects 8b10b, 64b6xb, PIPE, and PMA PCS modes and is identified with PolarFire V1.1 SP1 software or earlier.

For example, lanes 2 and 3 are swapped while using PIPE mode, and a TS1 packet is "00 01 03 02" instead of "00 01 02 03" for a x4 link.

Libero PolarFire SoC v2.0 corrects this issue.

3.21 JTAG Programming Times

FPGA programming using the FlashPro4 or 5 programming cable exceeds the current datasheet programming specification. This also impacts programming times of external SPI flash devices with PolarFire using the FlashPro cable.

Refer to the Libero SoC PolarFire 2.0 release notes for specific details.

For more information regarding actual programming specifications, see DS0141: PolarFire FPGA Datasheet.

This is not a device limitation, but rather the inherent speed of the cable, and will be addressed in a subsequent release of new FlashPro hardware.

3.22 PCIe After Asserting the PCIE_PERST_N Port

After a PCIe link is established at Gen2 speed, toggling the PCIE_PERST_N port of the PCIe block can cause the PCIe to fail to re-enumerate or re-link up. For example, a Gen2 (5 Gbps) link will not re-link up if the PCIE_PERST_N port is toggled.

When PERST# is asserted in L2/P2 state, the device will fail to exit L2 as expected.

An FPGA fabric workaround is available to mitigate this issue. Contact the factory for more information.

3.23 SSTL18I I/O Standard Not Supported for PF_XCVR_CLK

The SSTL18 I/O type is not supported in the PF_XCVR_REF_CLK input pins, as shown in the UG0677: PolarFire FPGA Transceiver User Guide.

LVDS25, HCSL25, and LVCMOS25 I/O types can be used as alternative inputs.

3.24 PCIe ECC Detection

The embedded ECC functions of the PCIe core that provide indicators for single-error correction (SEC) and double-error detection (DED) data detection is improperly functioning. These flags are tied to the incorrect operation of PCIE_#_M_RDERR/WRERR and PCIE_#_S_RDERR/WRERR pins of the PCIe embedded core.

The error-correcting logic is functional. The SECDED status indicators are incorrect.

For certain situations, an FPGA fabric workaround is available to mitigate this issue. Contact the factory for more information.

3.25 JTAG TCK Duty Cycle

The minimum and maximum specifications for JTAG TCK duty cycle deviate from the datasheet values: 25 MHz TCK with 45/55% duty cycle.

3.26 Transceiver PCS Mode 64b/6xb Limitations

The 64-bit data bus of the fabric interface for mode 64b6xb is permitted for the following lanes: Q0 LANE {0, 1, 2, 3} and Q{1-5} LANE{0,2}. The 32-bit data bus of the fabric interface can be used on all lanes of all transceiver quads.

3.27 Transceiver Lock to Reference Clock Limitation

The RX_CLK will stop for a specific period of time in BMR mode when the user changes the mode to lock-to-reference-clock-mode using control pins from the FPGA fabric. The minimum period of time is 1,024 REFCLK cycles and the maximum is 10,240 REFCLK cycles over the REFCLK frequency range of 100 MHz–312 MHz.

3.28 Limitations for ACJTAG IEEE 1149.6 for Transceiver Transmit Pins

For transceiver transmit pins, the following ACJTAG IEEE 1149.6 limitations exist:

- The instruction EXTEST_PULSE actually implements EXTEST_TRAIN instruction.
- The transceiver transmitter will transmit signals at very low amplitude during any AC or DC JTAG instructions.

3.29 Incorrect Transceiver LANEx_RX_READY Pin Behavior

The transceiver LANEx_RX_READY pin toggles when the Rx signal is open (or disconnected) or while an out-of-range condition occurs (due to incorrect Rx serial data rates, for instance: serial input data >1.7% away, which is considered out of range).

3.30 Unsupported Features

The following is a list of unsupported features. The features listed are not supported by engineering samples, but production devices have been updated to support these features.

- System Controller Suspend Mode
- Flash*Freeze Mode
- Temperature Voltage Sensor (TVS)
- Device Zeroization
- Digest Check
- Generic I/O Gearing Modes
  - Simulation-only support available in Libero PolarFire SoC 2.0
- PCIe Gen2 Electrical Compliance for x2 and x4 Links
- Automated DFE Support
  Contact the factory for DFE support
- XCVR Limitations for Entire Data Rate Range.
  Current support is limited to 10.3 Gbps and below. Contact the factory for solutions outside support listed in the Transceiver User Guide.

3.31 Supported Memory Interfaces

Double-data-rate (DDR) memory interface capabilities deviate from the specifications published in the DS0141: PolarFire FPGA Datasheet and UG0676: PolarFire FPGA DDR Memory Controller User Guide.

The following table highlights the current DDR3 and DDR4 capabilities per device and package combinations with all MPF300-ES silicon revisions and Libero SoC PolarFire v2.0. Additional capabilities will be added upon completion of silicon validation and software inclusion.

Table 5 • DDR Memory Interfaces

Die	Package	IO Type	Edge_Anchor	Memory Type	Interface Width	–1 SPD (Mbps)	STD (Mbps)
MPF300-ES	FCG484	HSIO	NORTH_NW	DDR3	up to x16	1333	1066
MPF300-ES	FCG484	HSIO	NORTH_NW	DDR3	x32, x40	1066	800
MPF300-ES	FCG484	HSIO	NORTH_NE	DDR3	up to x16	1333	1066
MPF300-ES	FCG484	HSIO	NORTH_NE	DDR3	x16, x32, x40	1066	800
MPF300-ES	FCG484	HSIO	NORTH_NW	DDR4	up to x16	1600	1333
MPF300-ES	FCG484	HSIO	NORTH_NW	DDR4	x32, x40	1333	1066
MPF300-ES	FCG484	HSIO	NORTH_NE	DDR4	up to x16	1600	1333
MPF300-ES	FCG484	HSIO	NORTH_NE	DDR4	x32, x40	1333	1066

Die	Package	IO Type	Edge_Anchor	Memory Type	Interface Width	–1 SPD (Mbps)	STD (Mbps)
MPF300-ES	FCG784	HSIO	NORTH_NE	DDR3	up to x16	1333	1066
MPF300-ES	FCG784	HSIO	NORTH_NE	DDR3	x16, x32, x40, x72	1072	800
MPF300-ES	FCG784	HSIO	NORTH_NW	DDR3	up to x40	1333	1066
MPF300-ES	FCG784	HSIO	NORTH_NW	DDR3	x64, x72	1066	800
MPF300-ES	FCG784	HSIO	NORTH_NW	DDR4	up to x40	1600	1333
MPF300-ES	FCG784	HSIO	NORTH_NW	DDR4	x64, x72	1333	1066
MPF300-ES	FCG784	HSIO	NORTH_NE	DDR4	up to x16	1600	1333
MPF300-ES	FCG784	HSIO	NORTH_NE	DDR4	x32, x40, x64, x72	1333	1066
MPF300-ES	FCG1152	HSIO	NORTH_NW	DDR3	up to x72	1333	1072
MPF300-ES	FCG1152	HSIO	NORTH_NE	DDR3	up to x16	1333	1072
MPF300-ES	FCG1152	HSIO	NORTH_NE	DDR3	x16, x32, x40, x72	1072	800
MPF300-ES	FCG1152	HSIO	SOUTH_SE	DDR3	up to x16	1333	1066
MPF300-ES	FCG1152	HSIO	NORTH_NW	DDR4	up to x72	1600	1333
MPF300-ES	FCG1152	HSIO	NORTH_NE	DDR4	up to x16	1600	1333
MPF300-ES	FCG1152	HSIO	NORTH_NE	DDR4	x32, x40, x72	1333	1066
MPF300-ES	FCG1152	HSIO	SOUTH_SE	DDR4	up to x16	1600	1333

3.32 Supported Transceiver Protocols

Transceiver protocol capabilities deviate from the specifications published in the DS0141: PolarFire FPGA Datasheet and UG0677: PolarFire FPGA Transceiver User Guide .

The following table summarizes the transceiver protocols supported by all MPF300-ES silicon revisions with Libero SoC PolarFire v2.0. Additional capabilities will be added upon completion of silicon validation and software inclusion.

Table 6 • Supported Transceiver Protocols

Transceiver Protocol	Details
SGMII/1000BaseX	Transceiver: 1.25 Gbps with CoreTSE IP Core TxPLL SyncE not supported
CPRI	Support for CPRI data rates 1–6

Transceiver Protocol	Details
10GBASE-R	Transceiver: 10.3 Gbps with Core10GMAC IP Core TxPLL SyncE not supported IEEE 1588 time stamping not supported
SATA 1-2-3	PHY layer supported. Contact factory.
Interlaken	Contact factory for support
JESD204B	Up to 10G with CoreJESD20BTX/RX IP Core
PCIE Endpoint Gen1/Gen2	See errata (see page 4)
PCIE Rootport Gen1/Gen2	See errata (see page 4)
LiteFast	Up to 5 Gbps

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA
Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Fax: +1 (949) 215-4996
Email: sales.support@microsemi.com
www.microsemi.com

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