Libero SoC PolarFire v2.0

Release Notes

2/2018

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51300186-1/2.18

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Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

Revision 1.6

Added section 5.13 Interaction with CoreFIFO, PolarFire v2.0, and Gold License.

Revision 1.5

Updated section 5.8 PCIe.

Revision 1.4

Updated section 1.1.1 Libero – Added bullet and text under SynplifyPro L201609MSP1-4 (RAM inference for ROM).

Revision 1.3

Updated section 1.1.7 SmartDebug.

Revision 1.2

Revision 1.2 includes the following changes:

- Update to section 3.1, General Notes on Design Migration
- Added limitation in Known Issue 5.4, DDR3 and DDR4 Memories
- Added Known Issue 5.5, Constraints Coverage Report Missing Some DDR Constraints
- Added Known Issue 5.13 PolarFire SgCore and SystemBuilder Core Generation
- Added Known Issue 5.17 Installer Note
- Added Known Issue 5.18 Installation on Windows 7
- Minor text edits and formatting changes for clarity

Revision 1.1

Added location of megavault, minor edits for clarity.

Revision 1.0

Revision 1.0 is the first publication of this document.

Reference Documents

PO0137: Product Overview PolarFire FPGA

DS0141: PolarFire FPGA Datasheet

UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide

Pin package Assignment Tables:

- MPF300T/MPF300TS-FCG484 Package Pin Assignment Table
- MPF300T/MPF300TS-FCVG484 Package Pin Assignment Table
- MPF300T/MPF300TS-FCSG536 Package Pin Assignment Table
- MPF300T/MPF300TS-FCG784 Package Pin Assignment Table
- MPF300T/MPF300TS-FCG1152 Package Pin Assignment Table

UG0752: PolarFire FPGA Power Estimator User Guide

UG0680: PolarFire FPGA Fabric User Guide

UG0684: PolarFire FPGA Clocking Resources User Guide

UG0686: PolarFire FPGA User I/O User Guide

UG0677: PolarFire FPGA Transceiver User Guide

UG0685: PolarFire FPGA PCI Express User Guide

UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide

UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide

UG0676: PolarFire FPGA DDR Memory Controller User Guide

UG0748: PolarFire FPGA Low Power User Guide

Athena TeraFire Cryptographic Algorithm Library (CAL) Users Guide

UG0743: PolarFire FPGA Debugging User Guide

UG0714: PolarFire FPGA Programming User Guide

UG0725: PolarFire FPGA Device Power-Up and Resets User Guide

UG0726: PolarFire FPGA Board Design User Guide

UG0753: PolarFire FPGA Security User Guide

UG0786: PolarFire FPGA Splash Kit User Guide

DG0755: PolarFire FPGA JESD204B Interface Demo Guide

DG0756: PolarFire FPGA PCIe Endpoint Demo Guide

DG0757: PolarFire FPGA 10GBASE-R Ethernet Loopback Demo Guide

DG0759: PolarFire FPGA Multi-Rate Transceiver Demo Guide

DG0762: PolarFire FPGA DSP FIR Filter Demo Guide

Verilog Simulation Guide

VHDL Simulator Guide

PolarFire FPGA Design Flow User Guide

PolarFire FPGA Macro Library Guide

PolarFire FPGA Design Constraints User Guide

PolarFire FPGA PDC Commands User Guide

PolarFire FPGA Timing Constraints User Guide

PolarFire FPGA Tcl Commands User Guide

PolarFire FPGA I/O Editor User Guide

Chip Planner User Guide

Netlist Viewer Interface User Guide

PolarFire FPGA Netlist Viewer User Guide

SmartPower User Guide

Timing Constraints Editor User Guide

SmartTime Static Timing Analyzer User Guide

PolarFire FPGA SmartDebug User Guide

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1 Libero SoC PolarFire™ v2.0 Software Release Notes

The Libero® system on chip (SoC) PolarFire™ v2.0 release is software for designing with Microsemi PolarFire FPGAs. PolarFire FPGAs are the fifth generation nonvolatile FPGA devices from Microsemi, built on 28-nm flash technology. The PolarFire cost-optimized FPGAs deliver lowest power at mid-range densities.

For more information about Libero SoC PolarFire devices, see the Microsemi website.

1.1 What's New in Libero SoC PolarFire v2.0

The PolarFire v2.0 release includes the following new features and enhancements.

1.1.1 Libero

- Design Entry
  - New SmartDesign Canvas
    - SmartDesign enables you to stitch together design blocks of different types (HDL, IPs, re-usable design blocks, lower-level SmartDesign blocks, basic macros) and generate a top-level design.
    - The new canvas places all components in columns, with the nets vertically routed in the space between columns. Top-level input ports are placed in the leftmost column. Top-level output ports and inout ports are placed the in rightmost column.
    - The new canvas has much more efficient placement and routing algorithms.
    - New highlight feature works on nets, instances, pins, ports and identifies modified modules.
    - In-place hierarchical expansion of sub-SmartDesign components

      For details, see the SmartDesign User Guide.
  - On-Demand Design Hierarchy Flow
    - Improves overall responsiveness of Libero during the design creation process. Design Hierarchy is not rebuilt on every design change; it is just marked as out-of-date.
    - You can rebuild the design hierarchy any time by clicking on the "Build Hierarchy" button located above the hierarchy frame.
    - Design Hierarchy is automatically rebuilt when invoking tools such as Synthesis, Simulation.
  - Component-Based Instantiation
    - Improves overall responsiveness of Libero during the design creation process by minimizing SmartDesign regeneration time when instantiated Components undergo incremental changes
    - Enforces that all cores are configured before they can be used
  - Addition of a 'User HDL Source Files' node in the Design Hierarchy window where all user HDL files are shown
  - Addition of a 'Components' node in the Design Hierarchy window where all components (SmartDesign(s), configured cores) are shown
- Place and Route Enhancements
  - Driver replication option which enables an algorithm to replicate critical net drivers to reduce timing violations. The algorithm prints the list of registers along with the duplicate names. Each set of names should be used in place of the original register in any specified timing constraint.

- Automatic input I/O register combining driven by set_input_delay constraint in the P&R SDC file.
- Automatic demotion of timing critical pins from CLKINT global nets.
- Expanded Global Net report.

- Block Flow Support
  - Enables the use of design blocks (optionally, with fixed placement and routing) as building blocks for a top-level design. Using these blocks can cut down design time as well as improve timing and power performance. Note that some PDC commands and hard macros are not supported in this release.
  - Number of row-global resources. The Place and Route tool configuration of a project creating a design block includes an option to restrict the number of row-global resources available in every quarter-row of a PolarFire device. During Place and Route of the block, the tool will not exceed this capacity on any quarter-row. If you enter a value lower than the maximum capacity (the default), the layout of the block will be able to integrate with the rest of the design if they consume the remaining row-global capacity.

- SynplifyPro L201609MSP1-4
  - Automatic Compile Points to improve runtime of design iterations.
    - This capability is in addition to manual Compile points that could be selected by the user.
    - Compile points disable cross-boundary optimizations, so it could impact total area.
  - RAM inference for ROM
    - Case statements in RTL or MEMORYFILE contents will be implemented in the sNVM memory of the device.
    - Clients will automatically appear inside the Design and Memory Initialization tool.
    - At power up, make sure that the circuit connected to the inferred ROM starts after one of the following system controller signals is asserted:

      ```
      INIT:SRAM_INIT_DONE
      INIT:PCIE_INIT_DONE
      INIT:GPIO_ACTIVE
      INIT:HSIO_ACTIVE
      INIT:FABRIC_POR_N
      ```

      To turn off ROM inference, insert the following parameter in the "Additional options" section and rerun synthesis:

      ```
      set_option -rom_map_logic 1
      ```
  - LSRAM inference for Write Byte-enables
    - Optimization of RAM inference when there are separate controls to enable writing per byte.
    - Note yet supported: Write Byte-enables in true Dual-port RAM.
  - Math inference for Coefficient ROM
    - Supported for signed and unsigned operations in Multiply, Multiply-accumulate, Multiply-add, Multiply-subtract and Preadder-multiply structures.
    - Not yet supported: Coefficient ROM inference in DOTP mode and Wide-multiplier where ROM data is registered.

1.1.2 Timing

- I/O timing
  - LVCMOS
  - PCI
  - LVDS outputs; LVDS inputs (MID VCM only)
  - SSTL 135/15/18 – all impedances and ODT (mid VCM only)
  - SSTL 135D/15D/18D – all impedances and ODT (mid VCM only)
- Updated MATH, URAM, LSRAM, UPROM models for improved accuracy
- Updated CFG, SLE, routing buffer models for improved accuracy
- Added Multi-corner Static Timing Analysis support
- Added Industrial temperature range support
- The timing data in this release is in the “Advance” state. In this state, data is extracted using electrical simulation but is not yet considered final. Adjustments in future releases are still possible based on silicon measurements.

1.1.3 Power

- SmartPower data updates
  - MATH Block – Default output toggling rate has been updated to reflect more realistic the math block usage in designs.
  - Transceiver – automatic use of the data rate set in the configurator
- SmartPower runtime Improvements
  - Invocation time improved by up to 4x
  - Significantly Improved time taken to switch between SmartPower tabs
- The power data in this release is in the “Advance” state. In this state, data is extracted using electrical simulation but is not yet considered final. Adjustments in future releases are still possible based on silicon measurements.

1.1.4 I/O Editor

- Added New Transceiver Signal Integrity View; see section 1.2.1 Signal Integrity Enhancements for details.

1.1.5 Design and Memory Initialization

- Design Flow
  - Separated Design and Memory Initialization Data Configuration and Generation steps
  - Simplified the Design Initialization Configuration dialog
  - Added Tcl Support
- RAM Initialization
  - Added support for Initializing RAMs to ‘0’
  - Added support for Synthesis ROM Inference – clients are automatically created with content defined in RTL
  - Added support to recognize Synthesis-inferred RAMs; users can choose to have the RAM bocks initialized at power up

1.1.6 Programming

Programming includes the following features and enhancements:

- SPI Flash Programming -- Allows programming of the SPI Flash device connected to the PolarFire device through the JTAG programming interface.
- DirectC
    - Added support for DAT file export
    - Supports SPI and JTAG programming
- Added FlashPro Express standalone support

For details about these features and enhancements, see the following:

- Libero SoC PolarFire Online Help
- FlashPro Express Online Help
- FlashPro Express User Guide

1.1.7 SmartDebug

For Libero SoC PolarFire v2.0, SmartDebug includes the following new features and enhancements:

- Signal Integrity enhancements, see section 1.2.1 Signal Integrity Enhancements for details.
- Eye Monitor for receivers on the XCVR lane.
- SmartBERT IP support which generates PRBS patterns from fabric.
- Supports demo mode – SmartDebug can be invoked without hardware connected.
- Added support to view sNVM clients as organized in the sNVM configurator.
- Eye Monitor – Allows creation of an eye diagram to measure signal quality on the receiver lane. Eye Monitoring estimates the horizontal eye-opening at the receiver serial data sampling point and helps the user select an optimum data sampling point at the receiver. The Eye Monitor feature is non-invasive, and supports both CDR and DFE modes. Eye Monitor is not supported when a transceiver lane is configured with data rates below 3.125 Gbps.
- Signal Integrity Widget – Allows users to modify Signal Integrity parameters after programming the device. It is used in conjunction with the Eye Monitor to improve the Eye Plot and ensure the best possible eye area. Once optimal Signal Integrity parameters have been reached, they can be exported into a PDC file that can be used as input to the Libero Constraints Manager tool for generating the final Design Initialization client data.
- Custom DFE Solution – This feature should be used to optimize DFE coefficients on lanes when data rates are greater than 5Gbps. It is used in conjunction with the Eye Monitor to improve Eye Plot and ensure the best possible eye area. DFE coefficients can also be exported into a custom configuration file that can be used as input to the Design and Memory Initialization tool for generating the final Design Initialization client data.
- SmartBERT – The CoreSmartBERT core provides a broad-based evaluation and demonstration platform for PolarFire transceivers. Parameterizable to use different transceivers and clocking topologies in native PMA mode, the SmartBERT core can also be customized to use different line rates and reference clock rates. Data pattern generators and checkers are included for each Transceiver lane, giving several different Pseudo-random binary sequences.

For details, see the PolarFire SmartDebug User Guide.

1.1.8 Identify

Identify for PolarFire is now available with Libero SoC PolarFire v2.0.

1.2 Silicon Features

The Libero SoC PolarFire v2.0 release includes the following PolarFire FPGA silicon feature enhancements and/or changes.

1.2.1 Signal Integrity Enhancements

Libero SoC PolarFire v2.0 has added a comprehensive set of tools to enable users to fine tune Transceiver interfaces at the board level.

The new Signal Integrity (SI) View in the I/O Editor allows users to customize the following XCVR Signal Integrity parameters:

- TX Emphasis Amplitude
- TX Impedance
- TX Transmit Common Mode Adjustment
- RX Insertion Loss
- RX CTLE
- RX Termination
- RX P/N Board Connection
- RX Loss of Signal Detector
- RX and TX Polarity

Alternatively, the above parameters can also be set in a PDC file.

For details, see the PolarFire I/O Editor User Guide.

With Libero SoC PolarFire v2.0, the default XCVR RX SI parameters, as a function of data rate and RX insertion loss, have been silicon-characterized.

The Transceiver Reference Clock Configurator now has On-Die Termination set to ON by default for better board-level signal integrity.

In Libero SoC PolarFire v2.0, SmartDebug has been significantly enhanced to help debug XCVR designs on the board.

- Eye Monitor -- Allows creation of an eye diagram to measure signal quality on the receiver lane. Eye Monitoring estimates the horizontal eye-opening at the receiver serial data sampling point and helps the user select an optimum data sampling point at the receiver. The Eye Monitor feature is non-invasive, and supports both CDR and DFE modes. Eye Monitor is not supported for transceiver lanes configured with data rates below 3.125 Gbps.
- Signal Integrity Widget – Allows users to modify Signal Integrity parameters after programming the device. It is used in conjunction with the Eye Monitor to improve the Eye Plot and ensure the best possible eye area. Once optimal Signal Integrity parameters have been reached, they can be exported into a PDC file that can be used as input to the Libero Constraints Manager tool for generating the final Design Initialization client data.
- Custom DFE Solution – This feature should be used to optimize DFE coefficients on lanes when data rates are greater than 5Gbps. It is used in conjunction with the Eye Monitor to improve Eye Plot and ensure the best possible eye area. DFE coefficients can also be exported into a custom configuration file that can be used as input to the Design and Memory Initialization tool for generating the final Design Initialization client data.
- SmartBERT - The CoreSmartBERT core provides a broad-based evaluation and demonstration platform for PolarFire transceivers. Parameterizable to use different transceivers and clocking topologies in native PMA mode, the SmartBERT core can also be customized to use different line rates and reference clock rates. Data pattern generators and checkers are included for each Transceiver lane, giving several different Pseudo-random binary sequences.

2 Device Support

Libero SoC PolarFire Device Support (Devices and packages in **bold** are new in v2.0)

Device	Package	Speed Grade	Core Voltage	Required License
MPF500T_ES	**FCG784_Eval**	-1, STD	1.0/1.05V	Eval/Platinum
	FCG1152_Eval	-1, STD	1.0/1.05V	Eval/Platinum
MPF500TS_ES	**FCG784_Eval**	-1, STD	1.0 /1.05V	Eval/Platinum
	FCG1152_Eval	-1, STD	1.0 /1.05V	Eval/Platinum
MPF300T_ES	FCG484	-1, STD	1.0 /1.05V	Eval/Platinum
	FCG1152	-1, STD	1.0 /1.05V	Eval/Platinum
	FCSG536	-1, STD	1.0 /1.05V	Eval/Platinum
	FCVG484	-1, STD	1.0 /1.05V	Eval/Platinum
	FCG784	-1, STD	1.0/1.05V	Eval/Platinum
MPF300TS_ES	FCG484	STD	1.0 /1.05V	Eval/Gold/Platinum
		-1	1.0 /1.05V	Eval/Gold/Platinum
	FCG1152	STD	1.0 /1.05V	Eval/Platinum
		-1	1.0 /1.05V	Eval/Gold/Platinum
	FCSG536	-1, STD	1.0 /1.05V	Eval/Platinum
	FCVG484	-1, STD	1.0 /1.05V	Eval/Platinum
	FCG784	-1, STD	1.0 /1.05V	Eval/Platinum
MPF200T_ES	**FCSG325_Eval**	-1, STD	1.0 /1.05V	Eval/Gold/Platinum
	FCSG536_Eval	-1, STD	1.0 /1.05V	Eval/Gold/Platinum
	FCVG484_Eval	-1, STD	1.0 /1.05V	Eval/Gold/Platinum
	FCG484_Eval	-1, STD	1.0 /1.05V	Eval/Gold/Platinum
	FCG784_Eval	-1, STD	1.0 /1.05V	Eval/Gold/Platinum
MPF200TS_ES	**Fully Bonded Package**	-1, STD	1.0 /1.05V	Eval/Gold/Platinum
	FCSG325_Eval	-1, STD	1.0/1.05V	Eval/Platinum
	FCSG536_Eval	-1, STD	1.0/1.05V	Eval/Platinum
	FCVG484_Eval	-1, STD	1.0/1.05V	Eval/Platinum
	FCG484_Eval	-1, STD	1.0/1.05V	Eval/Platinum
	FCG784_Eval	-1, STD	1.0/1.05V	Eval/Platinum
MPF100T_ES	**FCSG325_Eval**	-1, STD	1.0/1.05V	Eval/Silver/Gold/Platinum
	FCVG484_Eval	-1, STD	1.0/1.05V	Eval/Silver/Gold/Platinum
	FCG484_Eval	-1, STD	1.0/1.05V	Eval/Silver/Gold/Platinum
MPF100TS_ES	**Fully Bonded Package**	-1, STD	1.0 /1.05V	Eval/Silver/Gold/Platinum
	FCSG325_Eval	-1, STD	1.0/1.05V	Eval/Platinum
	FCVG484_Eval	-1, STD	1.0/1.05V	Eval/Platinum
	FCG484_Eval	-1, STD	1.0/1.05V	Eval/Platinum

See the Licensing web page for licensing details.

3 Design Migration

3.1 General Notes on Design Migration

The Libero SoC PolarFire v2.0 is a major release milestone in the Microsemi® PolarFire FPGA program. The number and scope of software enhancements and fixes require that older Libero PolarFire projects be invalidated in this release.

1. Upon opening a Libero SoC PolarFire v1.1 or v1.1 SP1 project, the design state will be reset to pre-Synthesis (pre-Compile, if Synthesis is turned off).
2. You must upgrade all cores to the latest version and re-generate existing designs through full implementation and timing verification flow.
    a. You must also rerun the Derive Constraints step before running Synthesis or Place-and-Route to get the most up to date configured core related timing constraints.

3.2 Cores Supported in Libero SoC PolarFire v2.0

Display Name	Libero SoC PolarFire v2.0	Change Status	Changes from Libero SoC PolarFire v1.1 SP1
Clock Conditioning Circuitry (CCC)	1.0.112	Must Upgrade	Functional bug fixes
Clock divider	1.0.101	Must Upgrade	
Glitchless clock mux	1.0.101	Must Upgrade	
PolarFire RC Oscillators	1.0.102	Must Upgrade	
DDR3	2.1.100	Must Upgrade	Detailed Change Notes in Section 3.2.1
DDR4	2.1.100	Must Upgrade	Detailed Change Notes in Section 3.2.1
PF Dual-Port Large SRAM	1.1.110	Must Upgrade	Added Tcl support for Memory Initialization When migrating designs with RAM blocks from releases prior to v2.0, you must re-generate the designs.
PolarFire SRAM (AHBLite and AXI)	1.1.121	Must Upgrade	Functional bug fixes Added Tcl support for Memory Initialization When migrating designs with RAM blocks from releases prior to v2.0, you must re-generate the designs.
PF Two-Port Large SRAM	1.1.108	Must Upgrade	Added Tcl support for Memory Initialization When migrating designs with RAM blocks from releases prior to v2.0, you must re-generate the designs.
PF uPROM	1.0.108	Must Upgrade	
PF Micro SRAM	1.1.107	Must Upgrade	Added Tcl support for Memory Initialization

			When migrating designs with RAM blocks from releases prior to v2.0, you must re-generate the designs.
PCI Express	1.0.230	Must Upgrade	Functional bug fixes
Transceiver Transmit PLL	1.0.109	Must Upgrade	DIV_CLK has been renamed to CLK_125, and is only exposed when TxPLL BIT_CLK is 2.5 Gbps; nets connecting to the DIV_CLK port of an instance of TxPLL will need to be reconnected to the renamed port CLK_125 after upgrade to this latest version Configuration dialog simplification
Transceiver Interface	1.0.223	Must Upgrade	Detailed Change Notes in Section 3.2.2
Transceiver Reference Clock	1.0.103	Must Upgrade	On-Die Termination is now ON by default
CoreSmartBERT	2.0.106	New for this release	Used in conjunction with SmartDebug to test XCVR data signal quality
PolarFire Dynamic Reconfiguration Interface	1.0.101	Must Upgrade	
PolarFire IOD CDR	1.0.210	Must Upgrade	
PolarFire IOD Generic Interfaces	N/A	Obsolete	Split RX and TX interfaces for ease of design. Replace with one of the following, depending on your configuration: PolarFire IOD Generic Receive Interface PolarFire IOD Generic Transmit Interface
PolarFire IOD Generic Receive Interface	1.0.115	New for this release	
PolarFire IOD Generic Transmit Interface	1.0.110	New for this release	
PolarFire 7:1 LVDS Receive Interface	1.0.104	New for this release	
PolarFire 7:1 LVDS Transmit Interface	1.0.104	New for this release	
PolarFire RGMII TO GMII	1.0.115	New for this release	
Crypto	1.0.101	Must Upgrade	
PolarFire Initialization Monitor	2.0.101	Must Upgrade	Removed GPIO/HSIO_ACTIVE ports; added bank controller options to monitor completion of IO calibration and bank power supply readiness
Tamper	1.0.102	Must Upgrade	

3.2.1 DDR3 and DDR4 Memory Configuration

All DDR3 and DDR4 configurations offered by the DDR3 and DDR4 cores can be used to create designs, verify design through simulation as well as running place and route and verifying the overall timing of the design.

The following enhancements and/or changes have been made in Libero SoC PolarFire v2.0:

- The DDR and FPGA fabric clocks are now a multiple of each other (a pulldown menu is available to select the ratio) to avoid rounding errors during configuration of the DDR core.
- The timing parameters have been re-organized in functional groups
- The Settling Time option has been removed; it is now fixed to 600us
- The AXI ID width is now configurable
- The Activate-Precharge lookup option has been added
- The ODT activation settings have been re-organized; the default settings have been changed for better signal integrity
- The PHY-only option has been added for users needing to integrate their own DDR controllers

For details on DDR use models, see UG0676: PolarFire FPGA DDR Memory Controller User Guide.

Note: DDR3/4 Design Timing Closure: You may need to add additional constraints to close timing for DDR3 and DDR4 interfaces. For details, refer to the DDR3/DDR4 reference designs.

3.2.2 Generic I/O Gearing Configuration

The following new configurators are available:

- PolarFire IOD Generic Receive Interface
- PolarFire IOD Generic Transmit Interface
- PolarFire 7:1 LVDS Receive Interface
- PolarFire 7:1 LVDS Transmit Interface
- PolarFire RGMII TO GMII

3.2.3 Transceiver Interface Configuration

The following are the changes in the Transceiver Interface for this release:

- New options available for “PCS Reset” setting (under “Interface Resets”):
    - RX Only → Default, for both newly created and migrated designs
    - TX Only
    - TX and RX
- Fixed functional bugs when the PCS-Fabric width is configured to be 64 or 80 and the RX and/or TX clocks are configured as Global or Global (Shared). You will observe some changes in the derived timing constraints for the above configurations.
- Fixed functional bugs and clock configurations for Soft PIPE SATA mode

For details, see UG0677: PolarFire FPGA Transceiver User Guide for details.

3.2.4 Power Up Monitoring Configuration

The PF_INIT_MONITOR configurator has been changed as follows:

- The GPIO/HSIO_ACTIVE ports have been removed and replaced with individual bank control options to monitor completion of IO calibration and power supply readiness on a per bank basis.

For details, see UG0725: PolarFire FPGA Device Power-Up and Resets User Guide.

4 Resolved Issues

The following table lists the customer-reported SARs resolved in Libero SoC PolarFire v2.0. Resolution of previously reported “Known Issues and Limitations” is also noted in this table.

4.1 List of Resolved Issues

Customer Case #	Description
493642-2258013558	PolarFire: Synplify mapper crash
493642-2266013245	Importing VHDL crashes Libero
493642-2279438509	DIV_CLK unknown in simulation
493642-2291898576	PF_PCIE: Address Translation and data transfer Simulation Support
493642-2304680808	Importing VHDL Files crashes Libero
493642-2306521385	Untested windows version 6.2 detected message appears at generation of bit stream
493642-2324625695	The BAR size included in the PCIe Configurator is not reflected on Linux
493642-2344316732	Libero SoC fails to create core from VHDL
493642-2347883772	DDR3:DQ_72:Error:PRPF_026: No feasible dedicated connection exists between pin Y of instance *.(HS_IO_CLK)' and *.(LANECTRL)' because of routing resource sharing. You must place these instances according to the PolarFire connectivity architecture rules
493642-2347929747	Libero IP core generation crashes when project path character length is 177
493642-2347929747	VHDL library not recognized by hierarchy properly
493642-2347929747	Root of design cannot exist in lib other than work
493642-2351704505	Synplify Pro L2016.09M-G5: .vm file does not contain definitions for all the instances
493642-2360116562	Generate FPGA Array Data Fails after successful Layout
493642-2361434769	PF_INIT_MONITOR RFU port size mismatch in simulation
	Crash: Max Path length issue
	PCIESS lanes timing needs to be updated with new portlist
	Incorrect pad mapping of uSPI related pins
	Remove PCIE slave ports when AXI slave is disabled in GUI
	Windows 10: SmartDesign instance port names overlap
	Import Files Tcl command needs to be updated in Tcl user guide
	set_clock_groups does not work with multiple clocks in 1 group
	PolarFire PCIe BFM simulation: Need 64-bit readstore support for PCIe AXI BFM
	PolarFire PCIe BFM simulation: need BFM support for built-in DMA transfer
	QuestaSim 3-Step Simulation Support

	SmartPower and on-board power are not matching
	DDR Memory Model - allow reduction in simulation time
	PF_DDR3: Require AXI IF ID width support up to 8-bit
	FAB_RAM_TAB: Ram initialization tool is not supporting imported Memory file paths having Spaces in the path.
	PF_SRAM_AHBL_AXI: Status of HEX file import and imported file name is not shown in the Configurator
	Unconstrained path report that shows multiple paths on the same line
	PolarFire PCIe BFM simulation: AXI bursts are limited to 16 cycles
	Auto generation of XCVR/PCIe initialization clients
	Popup message directs user to unavailable option for selecting programmers
	Unknown module warnings during Synthesis
	Runtime error crash when trying to bring up XCVR GUI in Libero SoC PolarFire v1.1 SP1
	PolarFire: DAT file only generated with STAPL
	VHDL: Module is not recognized when library clause is present above architecture block and used in entity instantiation
	Libero SoC PolarFire Transmit PLL GUI clock name mismatch
	Transceiver Provide Broadcast write support for all lanes
	PolarFire Transceiver UI: Too many clicks to add all lanes for debugging
	PolarFire router failed due to open nets
	Generate Initialization Clients failed in Linux
	DAT file support in export bitstream
	PF_IOD_CDR: P & R is failing with derived default constraints for the attached design
	Message Window usability issue
	Issue with Libero Export script file
	Near end EQ loopback failure
	Update needed for Phy reset in XCVR SmartDebug
	Remove FHB selection from project setting
	New core popup tells user a core version exists in repository even though it cannot be used with current software version
	Transceiver Loopback modes tool tip for ease of use
	PF_XCVR: REG_FILE location should be relative to simulation folder
	PF_XCVR: Bit-Slip option is not reset after update XCVR core even though new core has no bit slip GUI option
	SmartDebug standalone flow -- Export DDC file in Libero does not support bitstream option

5 Known Issues and Limitations

5.1 SPI Flash Programming

This release includes the following limitations:

- Only the Micron SPI Flash is currently supported with the Evaluation Kit.
- The verify time is currently not optimized. It is recommended to authenticate the SPI bitstreams with system services for quicker verification.
- This tool erases the SPI flash prior to programming, and currently does not support Data Storage clients for user data. It is recommended to program the SPI flash with Libero prior to programming other data on the SPI flash.
- Programming time is currently not optimized. It is recommended to not have huge gaps between clients in the SPI flash, since gaps are currently programmed with 1's.

  The following table lists the ERASE, PROGRAM, and VERIFY/READ times for different client sizes. All times are in hh:mm:ss.

  Note: Depending on the SPI-Flash memory silicon version, you may observe a shorter erase time.

	SPI Size	ERASE	PROGRAM	VERIFY/READ	TCK	Programmer
Data client size	1MB	0:3:55	0:2:08	0:14:00	4MHz	FlashPro5
	9 MB	0:3:55	0:17:22	2:46:29	4MHz	FlashPro5
Full SPI Memory Device	128 MB	0:3:55	4:15:50	38:58:42	4MHz	FlashPro 5

- Using the embedded FlashPro5 programmer on the PolarFire Eval Kit may more than double SPI flash programming times. This issue will be resolved in the PolarFire v2.1 release.

  Workaround: Use an external FlashPro5 programmer instead of the embedded programmer.
- The external FlashPro5 programmer TCK is fixed at 4MHz for SPI flash programming. The embedded FlashPro5 programmer is fixed at 1MHz for SPI flash programming.
- The TCK frequency in the Programmer Setting is not applicable for SPI-Flash Programming. This issue will be resolved in the PolarFire v2.1 release.
- SPI Bitstream content option "Filled with 1s" does not work for the SPI Flash. "Generate SPI Flash Image" and "Export SPI Flash Image" will fail if this option is selected.

  Workaround: Specify content to be "SPI Bitstream file for IAP", "SPI Bitstream file for Recovery/Golden", or "SPI Bitstream file for Auto Update".

5.2 SPI-Slave Programming

SPI-Slave programming is not supported for PolarFire.

5.3 SmartDebug

This release includes the following limitations:

- Standalone SmartDebug: Non Microsemi Devices in chain: Microsemi devices present in chain along with non-Microsemi devices cannot be debugged using standalone SmartDebug.

  Workaround: Users should use SmartDebug through Libero flow to debug Microsemi Devices

- Standalone SmartDebug: ID Code of Microsemi device cannot be read when non-Microsemi device is connected in chain when using standalone SmartDebug
- Logical View: The logical view cannot be reconstructed for:
    - LSRAM/uSRAM for port widths of x1 inferred through RTL.
    - LSRAM/uSRAM configurations when a single net of output bus is used i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM and others are unused. The memories can be read/write using physical view.
    - LSRAM/uSRAM configurations inferred using IP Cores CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).
    - HDL modules inferring RAM blocks are instantiated in SmartDesign.
- Plot eye introduces errors in data traffic on XCVR lanes that are configured to use CDR receiver path, when DFE and EM blocks are turned off in normal operation to save power.
- SmartBERT IP does not work when lanes are configured at 250Mbps data rate.
- The Custom DFE solution does not work when the transceiver is configured in 8B10B PCS mode

  Workaround: Perform the following steps to obtain the expected eye output with PLOT_EYE.

  1. Assert PCS RX RESET.
  2. Optimize DFE.
  3. Plot Eye
  4. De-Assert PCS RX RESET

5.4 DDR3 and DDR4 Memories

- Multi-rank SDRAM is currently not supported.
- DBI (DDR4) is currently not supported.
- The debug interface for DDR3/DDR4 should not be used.

5.5 Constraints Coverage Report Missing Some DDR Constraints

The constraint coverage report indicates numerous unconstrained paths in the DDR solution and from/to DDR I/O. The unconstrained paths can be ignored.

5.6 DLL Secondary Phase Restrictions Missing

- Although the user can specify values for Primary and Secondary phase with no restrictions, the Secondary Phase value cannot be lower than the Primary Phase value.

  Workaround: Do not set the Secondary Phase value lower than the Primary Phase value.

5.7 PLL

- Only the post-VCO feedback mode is available in this release.
- Bypass option on output clocks is not available in this release.
- In DLL Phase Generation Mode, the secondary output clocks are not producing the correct phase in simulations.

5.8 PCIe

- The AXI interface minimum clock frequency is 125 MHz. If the user would like the AXI4 to run slower, the CoreAXI4Interconnect uses a clock per interface to allow the PCIe to run at 125MHz while the rest of the design can run slower.
- For BFM simulation of AXI master or slave, the simulator may print out a warning message about AHB signals, such as “HRESP”. The warning message can be ignored.
- Due to an issue in the PCIe configurator, MSI interrupts are not set correctly. When a user selects any of the MSI interrupts (i.e. MSI1, MSI2, MSI4, MSI8, MSI16, MSI32), the PCIe block is generated with interrupts configured as ‘MSI1’. This issue will be fixed in an upcoming release. To work around this issue, users can use “Custom configuration file” in the Configure Design Initialization Data and Memories tool settings to update the register contents.

  See UG0685: PolarFire FPGA PCI Express User Guide, section 5.4 for interrupts and MSI register settings.

5.9 Transceiver

- When XCVR is configured in 8b10b mode and the PCS-Fabric width is 16, the following Interface Clock options are not supported for both TX and RX Clocks:
  - Use as PLL reference clock option.
  - Global and Global (Shared) options.
- When the PCS-Fabric width is configured to be 64 or 80, the Interface clock option “Use as PLL reference clock” is not supported.

5.10 Synthesis

During Synthesis, you may see a message such as “Blackbox CRYPTO is missing a user supplied timing model” in the log file. This can be ignored.

Synplify Pro is intended to be used only with PolarFire devices in this release.

5.11 Standalone Synthesis Flow

PolarFire users may synthesize their design outside the Libero SoC tool by using Synopsys SynplifyPro directly. When using this flow, the following additional steps are necessary to successfully synthesize and implement a design:

- Ensure that the <install location>/Designer/data/aPA5M/polarfire_syn_comps.v is passed to SynplifyPro. This file contains module declarations – known as blackbox, with timing information in most cases, for PolarFire primitives not known to Synopsys.
- Many configured cores generate timing constraints. You must ensure that these constraint files are passed to synthesis for optimal results. These constraint files must also be imported into Libero SoC along with the synthesis gate level netlist to get optimal place and route results and have correct timing analysis done by Libero. Note that the core generate constraint files are needed to be modified so constraints are expressed using the proper hierarchical name of the configured cores in the top-level design.

5.12 I/O and I/O Bank Known Issues

- For FCG484/FCVG484/FCSG536 – I/O Bank 4 and Bank 5 must have the same VDDI, but I/O Editor and ChipPlanner do not enforce that requirement. Specifying different VDDI will fail during Place and Route. User must specify the same VDDI for both I/O banks.
- Multiple voltages in an I/O bank are not supported in this release.

5.13 Interaction with CoreFIFO, PolarFire v2.0, and Gold License

In the Libero SoC PolarFire v2.0 release, for the MPF100TS_ES, MPF200TS_ES, and MPF300TS_ES devices, if you are using a Gold License and attempt to generate CoreFIFO, you will see errors. As a workaround, create a new project with the device set to “MPF100T” or “MPF200T”, configure CoreFIFO, and generate. Then close your project, open your actual project and import the required files.

Import the following .v or .vhdl files from the folder /<Prj_MPF100T/MPF200T>/component/Actel/DirectCore/COREFIFO/2.6.108/rtl/vlog/test/user.

- clock_driver
- fifo_driver
- fifo_monitor
- g4_dp_ext_mem
- MEM_WeqR
- MEM_WgtR
- MEM_WltR

For the below steps,”sdfifo” refers to the name given to the CoreFIFO component during instantiation.

Import the .v or .vhdl files from the folder /<Prj_MPF100T/MPF200T>/component/work/sdfifo/sdfifo_0/rtl/vlog/core.

- COREFIFO
- corefifo_async
- corefifo_doubleSync
- corefifo_fwft
- corefifo_grayToBinConv
- corefifo_sync
- corefifo_sync_scntr
- sdfifo_sdfifo_0_LSRAM_top
- sdfifo_sdfifo_0_ram_wrapper

Also Import the sdfifo (.v or .vhdl) file in the folder <Prj_MPF100T/MPF200T>/component/work/sdfifo.

5.14 PolarFire SgCore and SystemBuilder Core Generation

With Libero SoC PolarFire v2.0, PolarFire SgCore and SystemBuilder cores generate only Verilog files, regardless of the preferred HDL language selected. VHDL users must use mixed-language simulation (available with ModelSim ME Pro).

5.15 Other Limitations

This release has the following additional limitations:

- Post-synthesis and post-layout simulations are not supported
- IBIS generation is not supported

5.16 Installation on Local Drive Only

This release is intended for installation only on a local drive. The Installer might report permission rights problems if the release is installed across a networked drive.

5.17 Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click Yes and the software is installed successfully.

5.18 Installer Note

The Libero SoC PolarFire installer for Windows has been updated to address a cross-version compatibility issue. If you had the previous installer, and encountered an error when trying to install Libero SoC v11.8 after installing PolarFire v2.0, perform the following steps:

1. Uninstall PolarFire v2.0.
2. Download the installer.
3. Reinstall PolarFire v2.0.

5.19 Installation on Windows 7

During PolarFire v2.0 installation on Windows 7 machines, you may see pop-up warning messages about shortcuts toward the end of installation process.

These messages can be safely ignored. Click OK to close the pop-up windows and the installation will proceed and complete as expected. All Windows shortcuts will appear correctly.

5.20 Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. Microsemi is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC, ModelSim ME and/or Synplify Pro ME may or may not be affected.

All public releases of Libero are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, Microsemi's software development and testing environment is also protected by antivirus tools and other security measures.

6 System Requirements

The Libero SoC PolarFire v2.0 release has the following system requirements:

- 64-bit OS
  - Windows 7, Windows 8.1, or Windows 10 OS
  - RHEL 5, RHEL 6, RHEL 7, CentOS 5, CentOS 6, or CentOS 7
    - Programming is not supported on RHEL 5, CentOS 5
- A minimum of 32 GB RAM

Note: Setup instructions for using Libero SoC on Red Hat Enterprise Linux OS are available on the Libero SoC Documents web page. As noted in that document, installation step 2 now includes running a shell script (bin/check_linux_req.sh) to confirm the presence of all required runtime packages.

Note: Support for the following operating systems will cease after December 2017. For more information, refer to PCN17031.

- RedHat Enterprise Linux 5.x through 6.5
- CentOS 5.x through 6.5

7 Download Libero SoC PolarFire v2.0 Software

The following are available for download:

- Libero SoC PolarFire v2.0 for Linux
- Libero SoC PolarFire v2.0 for Windows
- Libero SoC PolarFire v2.0 MegaVault

Note: Installation requires administrative privileges.

After successful installation, clicking **Help-> About Libero** will show Version: 12.200.0.20.