DG0796
Demo Guide
PolarFire FPGA Splash Kit JESD204B Standalone Interface

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the current publication.

1.1 Revision 3.0

This document is updated with respect to Libero® SoC PolarFire v2.2 release.

1.2 Revision 2.0

This document is updated with respect to Libero SoC PolarFire v2.1 release.

1.3 Revision 1.0

The first publication of this document.

2 PolarFire FPGA Splash Kit JESD204B Standalone Interface

This document describes how to run the JESD204B standalone demo design on the PolarFire® Splash Board using the JESD204B Standalone Demo GUI application. The GUI application is packaged along with the design files. The demo design is a reference design built using the PolarFire high-speed transceiver blocks and the CoreJESD204BTX and CoreJESD204BRX IP cores. It operates in loopback mode by sending the CoreJESD204BTX data to the CoreJESD204BRX IP core through the transceiver lanes, which are manually looped back on the board. This loopback setup facilitates a standalone JESD interface demo that does not require analog-to-digital converter (ADC) or digital-to-analog converters (DAC).

Microsemi PolarFire devices have embedded, high-speed transceiver blocks that can handle data rates ranging from 250 Mbps to 12.5 Gbps. The transceiver (PF_XCVR) module integrates several functional blocks to support multiple high-speed serial protocols within the FPGA. JESD204B is a high-speed serial interface standard for data converters developed by the JEDEC committee. The JESD204B standard reduces the number of data inputs and outputs between the high-speed data converters and receivers.

Microsemi provides CoreJESD204BTX and CoreJESD204BRX IP cores that implement the transmitter and receiver interfaces of the JESD204B standard. These IP cores are easy to integrate with JESD204B-based data converters to develop high-bandwidth applications such as wireless infrastructure transceivers, software-defined radios, medical imaging systems, and radar and secure communications. These IP cores support link widths from x1 to x8, and link rates from 250 Mbps to 12.5 Gbps per lane using subclass 0, 1, and 2.

For more information about the JESD204B interface design implementation, and all the necessary blocks and IP cores instantiated in Libero® SoC PolarFire, see Demo Design, page 3.

The JESD204B standalone Interface design can be programmed using any of the following options:

- Using the stp file: To program the device using the stp file provided along with the design files, see Programming the Device Using FlashPro, page 18.
- Using Libero SoC PolarFire: To program the device using Libero SoC PolarFire, see Libero Design Flow, page 14. Use this option when the demo design is modified.

2.1 Design Requirements

The following table lists the resources required to run the demo.

Table 1 • **Design Requirements**

Requirement	Version
Operating System	Windows 7, 8.1, or 10
Hardware	
PolarFire Splash Kit • PolarFire Splash Board with MPF300TS-1FCG484EES device • 12 V, 5 A AC power adapter and cord • USB 2.0 A to Mini-B cable for UART and programming	Rev 2 or later
Software	
FlashPro	v2.2
GUI executable (provided with the design files)	
Libero SoC PolarFire	v2.2

Table 1 • **Design Requirements *(continued)***

ModelSim	10.5c Pro
Synplify Pro	L201609MSP1-5
IP	
JESD204BTX	3.0.114
JESD204BRX	3.0.126
PF_XCVR	1.0.231
PF_TX_PLL	1.0.112
PF_XCVR_REF_CLK	1.0.103
PF_URAM	1.1.107
PF_INIT_MONITOR	2.0.103
COREUART	5.6.102
CORERESET_PF	2.1.100

2.2 Prerequisites

Before you start:

1. Download the demo design files from the following location: *http://soc.microsemi.com/download/rsc/?f=mpf_dg0796_liberosocpolarfirev2p2_df*
2. Download and install Libero SoC PolarFire v2.2 on the host PC from the following location: *https://www.microsemi.com/products/fpga-soc/design-resources/design-software/libero-soc-polarfire#downloads*

   The latest versions of ModelSim and Synplify Pro are included in the Libero SoC PolarFire installation package.

Note: A Libero Gold license is required to evaluate your designs using the PolarFire Splash Kit.

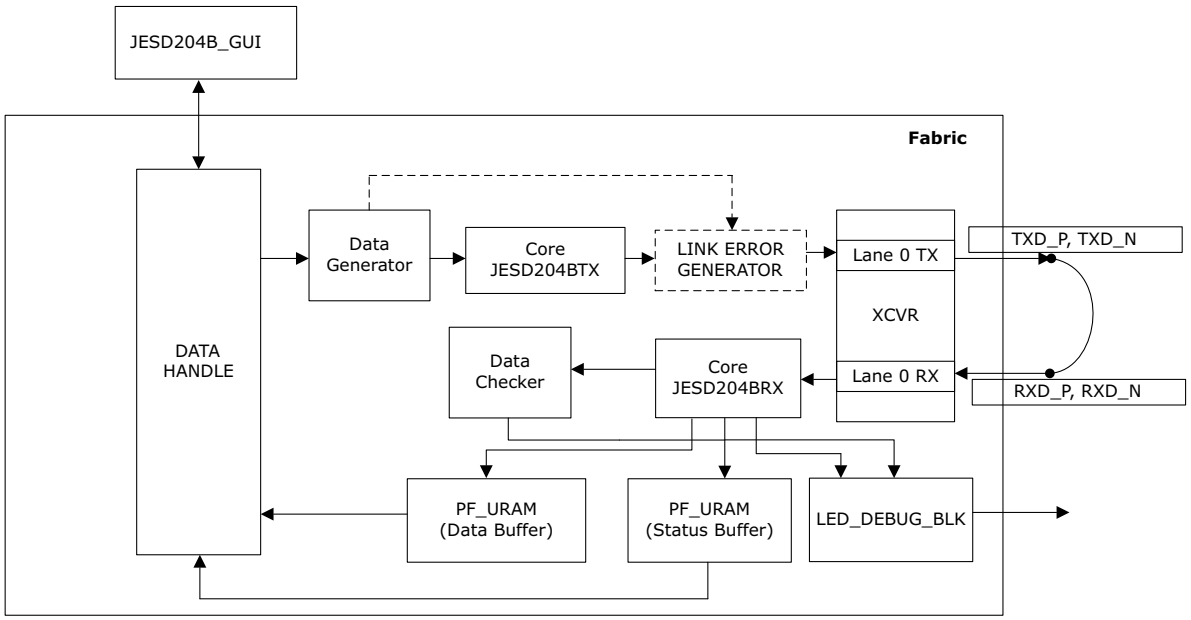
2.3 Demo Design

The PolarFire JESD204B demo design is developed for interfacing JESD204B- compliant data converters with PolarFire devices. In this design:

1. The DATA_HANDLE_0 block interfaces with the GUI. The GUI enables the selection of PRBS or waveform input.
2. The DATA_HANDLE_0 block passes the input selection to the DATA_GENERATOR_0 block, which generates and sends the corresponding input data to the CoreJESD204BTX IP core.
3. The CoreJESD204BTX IP core performs JESD204B transmitter functions based on the configuration, and sends the data to the PF_XCVR (transceiver) IP core.
4. The encoded data is received by the CoreJESD204BRX IP core because the TX and RX lanes of the PF_XCVR block are looped back.
5. The CoreJESD204BRX IP core performs JESD204B receiver functions based on the configuration, and sends the data to the GUI for viewing the selected input.

Note: When a data error or link error is selected on the GUI, the error generator block generates that error and displays it on the GUI.

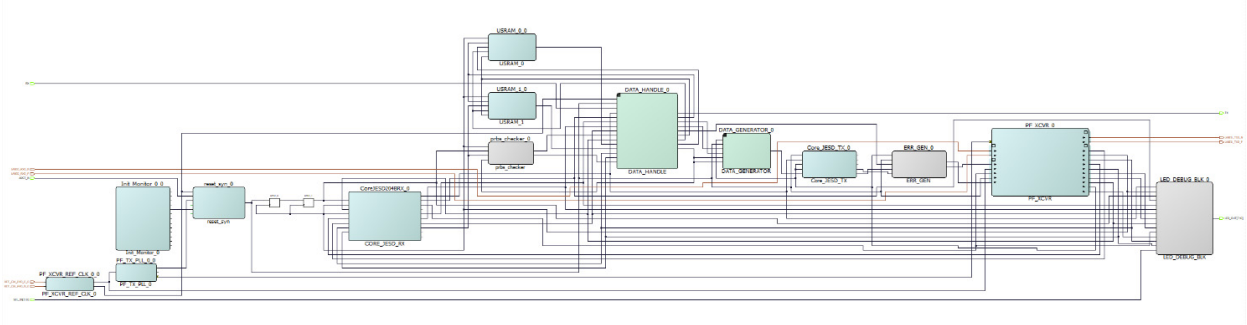
Figure 1 • **Hardware Implementation Block Diagram**



2.3.1 Design Implementation

The following figure shows the Libero design implementation of the JESD204B interface demo.

Figure 2 • **JESD204B Interface Design**



The following table lists the important I/O signals of the design.

Table 2 • **I/O Signals**

Signal	Description
Input Signals	
LANE0_RXD_P and LANE0_RXD_N	Transceiver receiver differential inputs
ARST_N	Reset signal obtained from the SW2 push-button switch on the board
RX	Receiver of UART interface
REF_CLK_PAD_P_0 and REF_CLK_PAD_N_0	Differential reference clock obtained from the on-board 125-MHz oscillator

Table 2 • **I/O Signals**

Signal	Description
Input Signals	
SEL_IN[3:0]	Signal mapped to DIPs 1, 2, 3, 4 of SW8 dip slide switch used to debug the status and errors
Output Signals	
LANE0_TXD_P and LANE0_TXD_N	Transceiver transmitter differential outputs
LED_OUT[7:0]	Signal that indicates whether link is up or down
TX	Transmitter of UART interface

2.3.2 IP Configuration

The hardware design for the JESD204B interface includes the following blocks:

2.3.2.1 Data Handle

The data handle (DATA_HANDLE_0) block receives the input data selection and link or data error generation information from the GUI. This block also sends the data output received from the CoreJESD204BRX core and the data or link status error to the GUI for viewing.

2.3.2.2 Data Generator

The data generator has a PRBS generator and a waveform generator. The PRBS generator generates PRBS7, PRBS15, PRBS23, and PRBS31 patterns. An error insertion mode implemented in the PRBS generator, inserts an error into the PRBS sequence. The waveform generator generates sine, sawtooth, triangle, and square waveforms. The data generator feeds the 64-bit test pattern to the JESD204BTX core, which then transmits data to the transceiver.

2.3.2.3 PF_URAM

There are two instances of PF_URAM blocks, the PF_URAM_0 block stores the JESD204B link status before sending it to the GUI. The PF_URAM_1 block stores the data received from the CoreJESD204BRX before sending the data to the GUI.

2.3.2.4 Error Generator

The error generator block (ERR_GEN_0) generates link errors by sending random data between CoreJESD204BTX and PF_XCVR when the link error generation is selected on the GUI.

2.3.2.5 PRBS_checker

The data checker receives 64-bit data from the CoreJESD204BRX IP core and checks whether the received data is correct. It generates an error count and a status signal, which are sent to the GUI for status indication. The data checker only checks the PRBS sequences of the data generator.

2.3.2.6 LED Debug

The LED debug block (LED_DEBUG_BLK_0) debugs the JESD204B link status and other errors. When the link is up, LEDs 1, 2, 3, 4, 5, and 6 glow, and LEDs 7 and 8 do not glow (with DIP 1, 2, 3, and 4 set low on the SW8 dip slide switch).

2.3.2.7 Init_monitor

When the DEVICE_INIT_DONE signal from Init_monitor block goes high, the transceiver is completely configured. This signal is anded with ARST_N signal to get proper reset signal for the design.

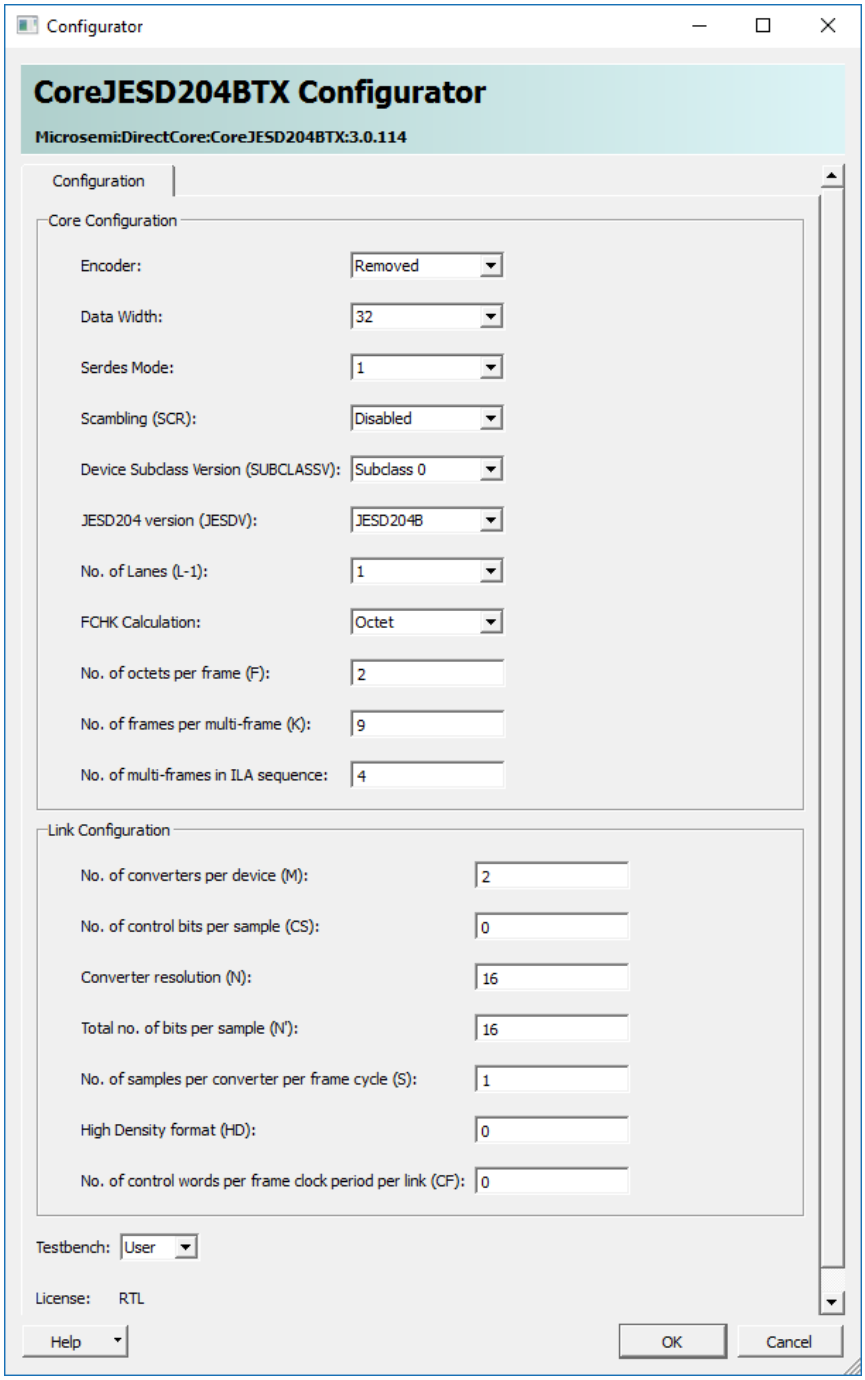
2.3.2.8 CORERESET_PF

CoreReset_PF synchronizes resets to the respective user-specified clock domain. This ensures that when the assertion is asynchronous, the negation is synchronous to the clock.

2.3.2.9 CoreJESD204BTX

CoreJESD204BTX is the transmitter interface of the JEDEC JESD204B standard. For this demo design, this IP core is configured in Libero SoC PolarFire v2.2, as shown in Figure 3, page 6. For more information about CoreJESD204BTX, see *CoreJESD204BTX Handbook*.

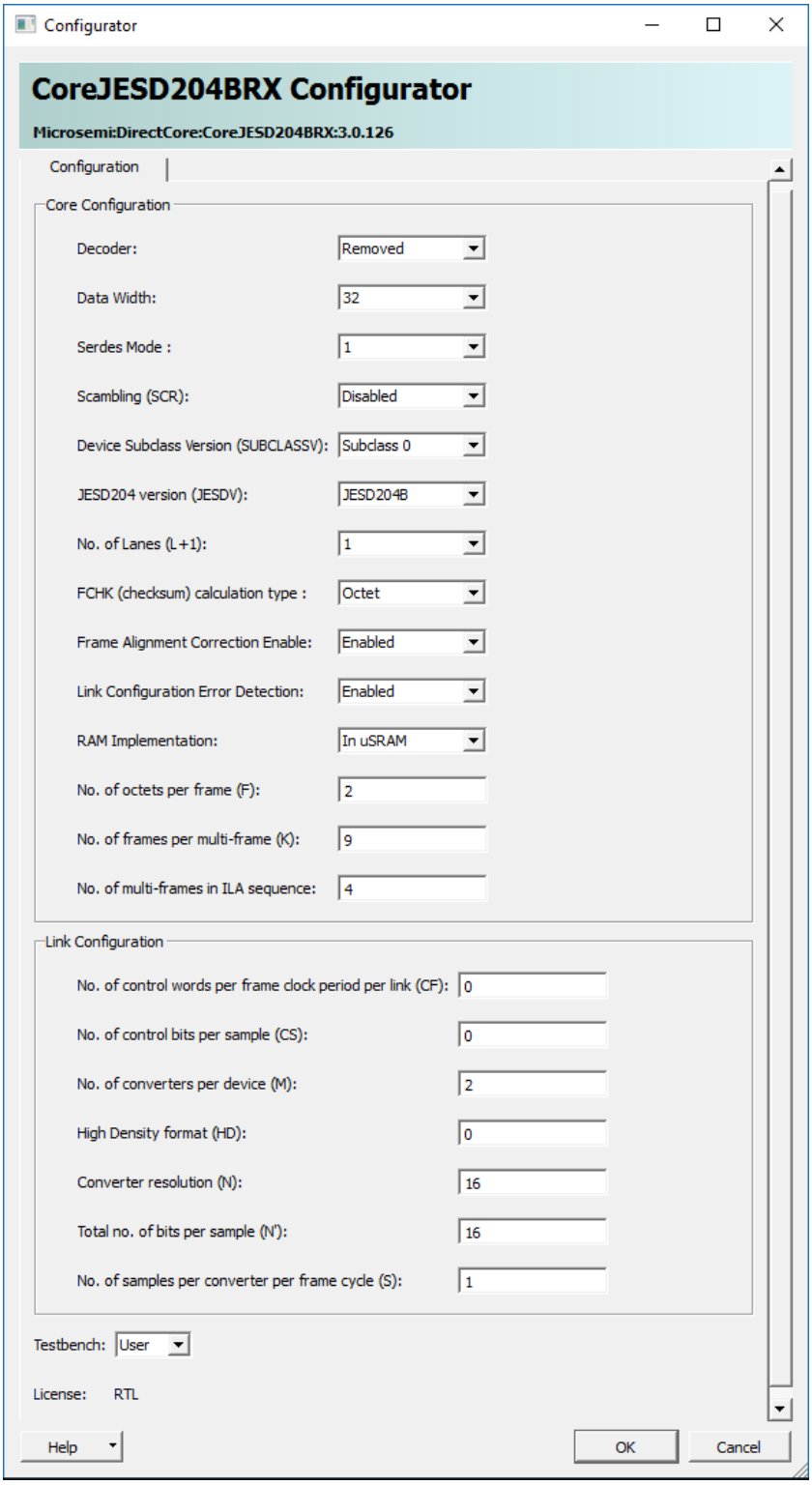
Figure 3 • **CoreJESD204BTX Configurator**



2.3.2.10 CoreJESD204BRX

CoreJESD204BRX is the receiver interface of the JEDEC JESD204B standard. For this demo design, this IP core is configured in Libero SoC PolarFire v2.2 as shown in the following figure. For more information about CoreJESD204BRX, see *CoreJESD204BRX Handbook*.

Figure 4 • **CoreJESD204BRX Configurator**



2.3.2.11 Transceiver Interface

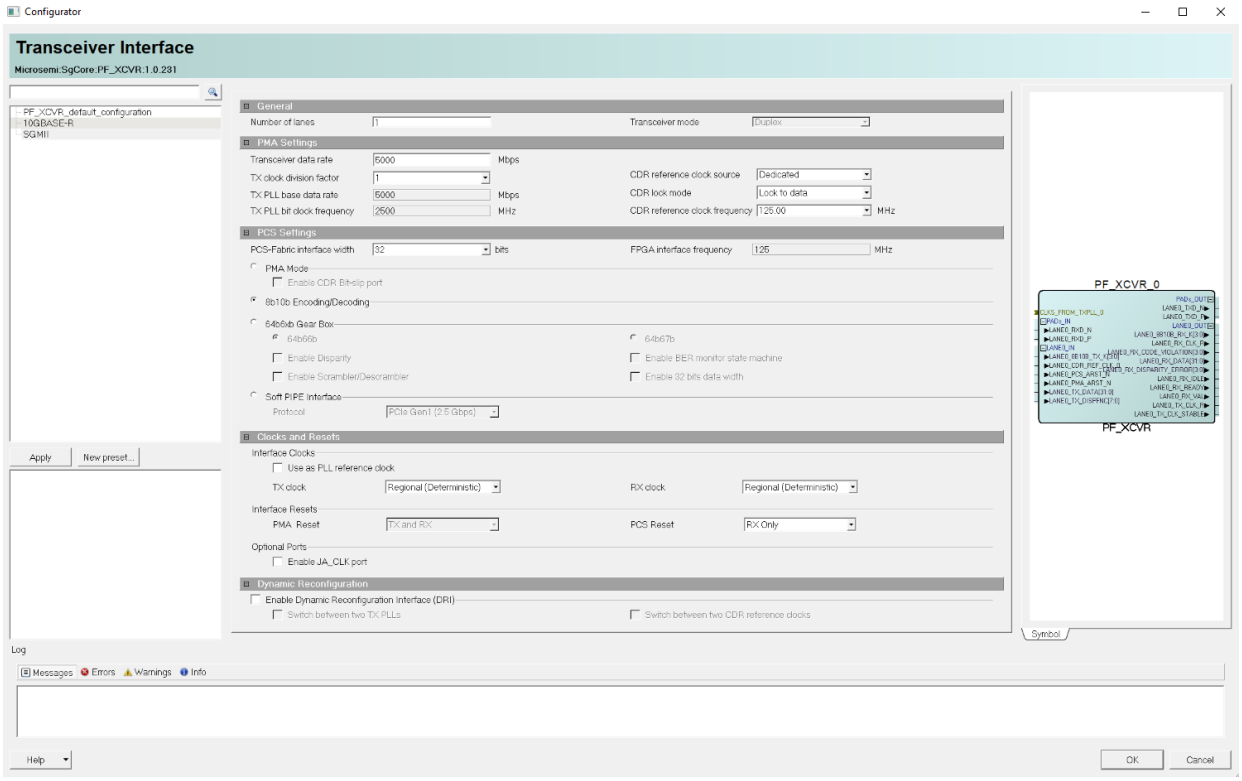
The PolarFire high-speed transceiver (PF_XCVR) is a hard IP block that supports high-speed data rates ranging from 250 Mbps to 12.5 Gbps.

In this demo, the transceiver block (PF_XCVR) is configured in 8b10b mode with a CDR reference clock of 125 MHz to support 5.0 Gbps data rate.

The PolarFire transmit PLL (PF_TX_PLL) sends the reference clock feed to the transceiver. The dedicated reference clock (PF_XCVR_REF_CLK) drives the PF_TX_PLL to generate the desired output clock for the 5.0 Gbps data rate.

The following figure shows the Transceiver interface configuration.

Figure 5 • **Transceiver Interface Configurator**



2.4 Clocking Structure

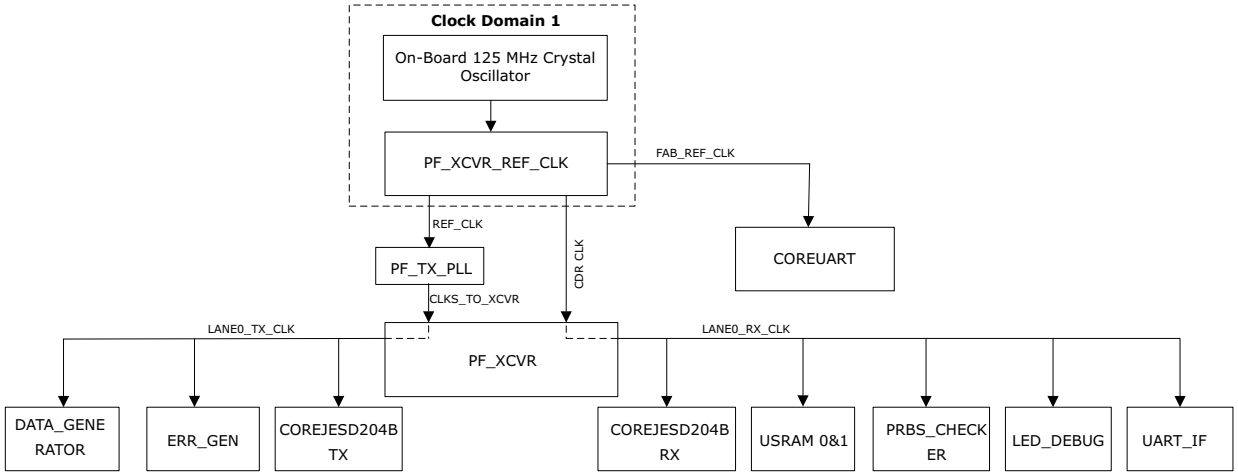
In the reference design, there are three clock domains:

- RX_CLK (125 MHz)
- TX_CLK (125 MHz)
- FAB_REF_CLK (125 MHz)

The on-board 125-MHz crystal oscillator drives the XCVR reference clock, which provides clock to the DATA_GENERATOR, CoreJESD204BTX, ERR_GEN, CoreJESD204BR, LED_DEBUG, PRBS_CHECKER, USRAM 0 &1, COREUART, and UART_IF blocks.

Note: If there is a change in the data rate or reference clock of the transceiver, you must reconfigure COREUART.

Figure 6 • **Clock Structure**



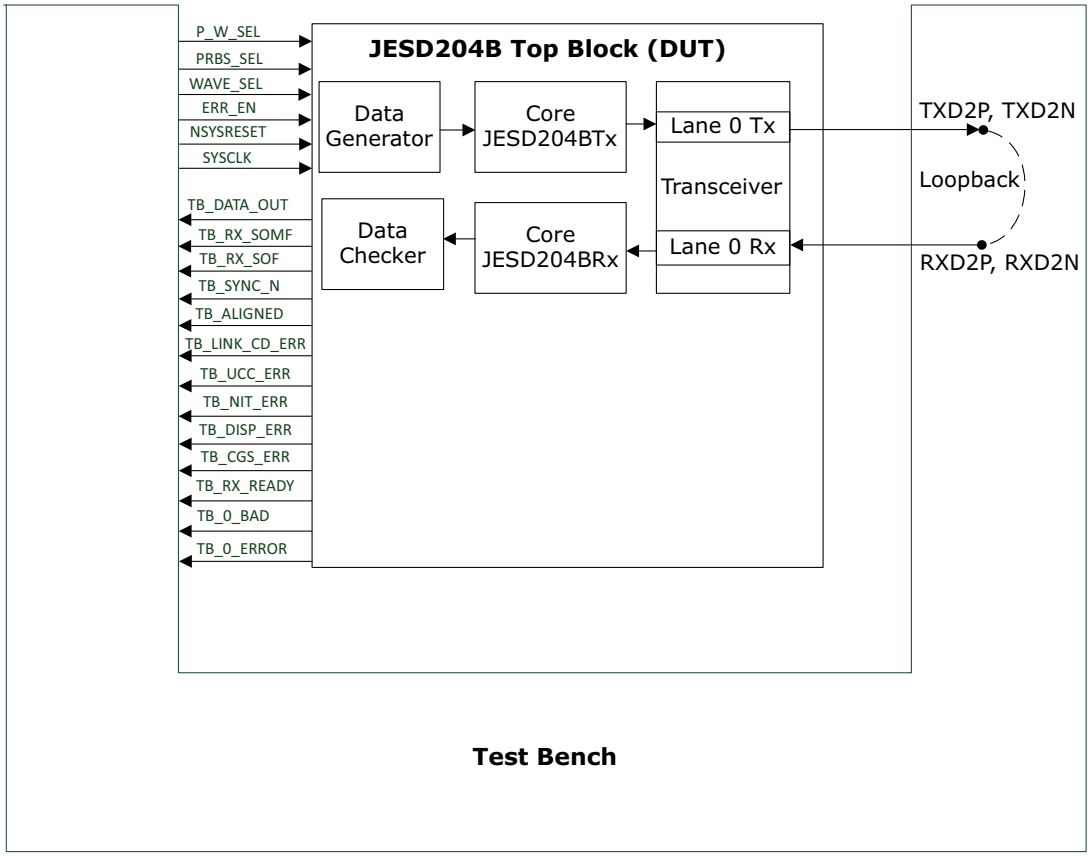
2.5 Simulating the PolarFire JESD204B Design

Before you start:

1. Start Libero SoC PolarFire, and select **Project** > **Tool Profiles...**.
2. In the **Tool Profiles** window, select **Synthesis** and **Simulation** on the **Tools** panes and select the latest active installation directory paths for these two tools.
3. In the **Project** menu, click **Open Project**.
   The **Open Project** dialog box opens.
4. Browse the design files folder, `mpf_dg0796_liberosocpolarfirev2p2_df\LiberoProject\PF_JESD204B_SA`, and select the `PF_JESD204B_SA` PRJX file. Then, click **Open**.
   The PolarFire JESD204B project opens in Libero SoC PolarFire.
5. Download the following IP cores from Libero SoC PolarFire Catalog:
   - CoreJESD204BTX
   - CoreJESD204BRX
   - PF_XCVR
   - PF_TX_PLL
   - PF_XCVR_REF_CLK
   - PF_URAM
   - COREUART
   - PF_INIT_MONITOR

A testbench is provided to simulate the JESD204B PRBS pattern and waveform selection. The following figure shows the interaction between testbench and the design.

Figure 7 • **Testbench and JESD204B Demo Design Interaction**



The testbench generates the test selection for the PRBS input (PRBS7, PRBS15, PRBS23, and PRBS31) and waveform input (sine wave, sawtooth wave, triangle wave, and square wave). It also monitors the JESD204B output status signals (SYNC_N, ALIGNED, and CGS_ERR) for the verification of JESD204B phases, and PRBS checker output status signals O_BAD and O_ERROR[4:0]. The following table lists the simulation signals.

Table 3 • **Simulation Signals**

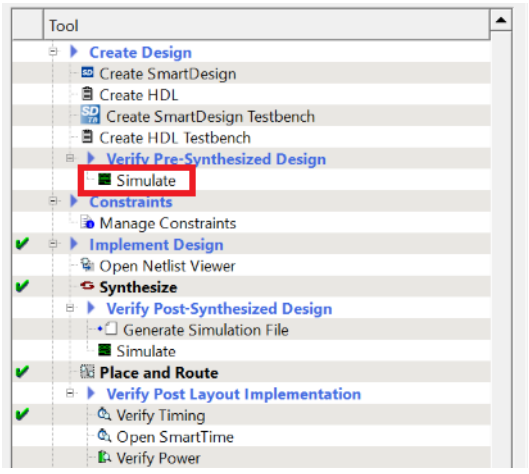
Signal	Description
Input Signals	
P_W_SEL	Input to select the PRBS pattern or waveform
WAVE_SEL[1:0]	Input to select the type of waveform
PRBS_SEL[1:0]	Input to select the type of PRBS pattern
ERR_EN	Input to enable error in the PRBS pattern
NSYSRESET	Active low reset signal
SYSCLK	125-MHz generated clock
Output Signals	
TB_DATA_OUT	Output data from CoreJESD204BRX

Table 3 • **Simulation Signals**

Signal	Description
Input Signals	
TB_RX_SOMF	This is the SOMF_0[3:0] signal received from the CoreJESD204BRX block
TB_RX_SOF	This is the SOF_0[3:0] signal received from the CoreJESD204BRX block
TB_SYNC_N	This is the SYNC_N signal, which indicates the link status
TB_ALIGNED	This is the ALIGNED signal, which indicates that all transceiver lanes are aligned
TB_LINK_CD_ERR	This is the LINK_CD_ERR[0] signal, which indicates a link configuration data mismatch error
TB_UCC_ERR	This is the UCC_ERR[0] signal, which indicates an unexpected control character error
TB_NIT_ERR	This is the NIT_ERR[3:0] signal, which indicates the “not in table” error. This signal is controlled by LANE0_RX_CODE_VIOLATION[3:0]
TB_DISP_ERR	This is the DISP_ERR[3:0] signal which indicates the disparity error. This signal is controlled by LANE0_RX_DISPARITY_VIOLATION[3:0]
TB_CGS_ERR	This is the CGS_ERR signal, which indicates the code group synchronization error. This signal is controlled by the CGS_ERR[0] signal.
TB_RX_READY	This is the LANE0_RX_READY signal received from the transceiver block
TB_0_BAD	Error flag
O_ERROR[4:0]	Number of errors occurred during PRBS check.

In the **Design Flow** tab, double-click **Simulate** under **Verify Pre-Synthesized Design** to simulate the design. The **Simulate** option is highlighted in Figure 8, page 11.

Figure 8 • **Simulating the Design**



When the simulation is initiated, ModelSim compiles all the design source files, runs the simulation, and configures the waveform viewer to show the simulation signals.

2.5.1 Simulation Flow

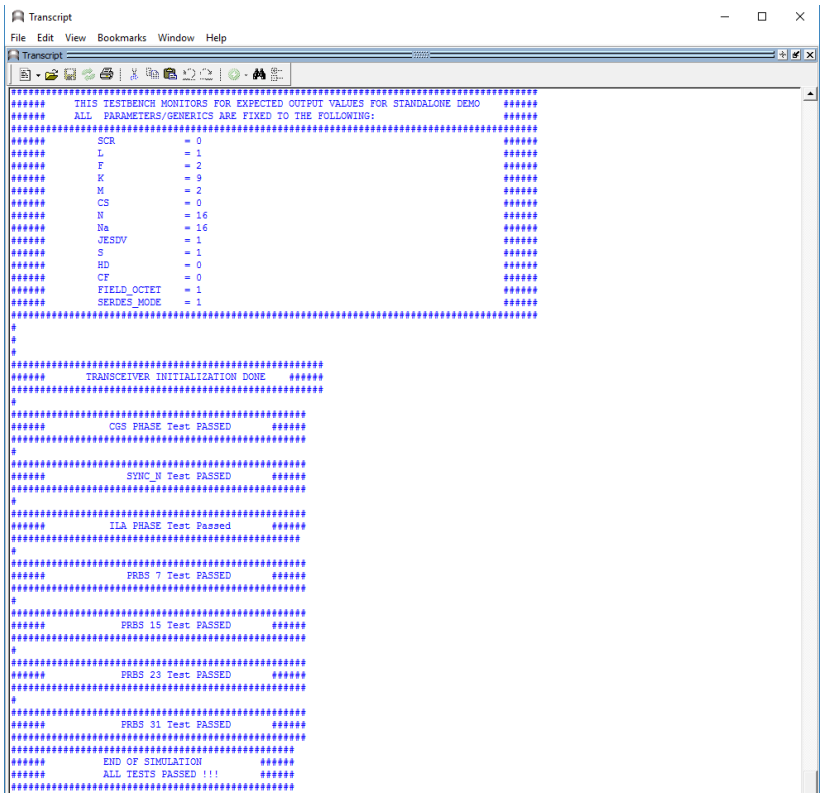
The following steps describe the JESD204B testbench simulation flow:

1. At the start, the NSYSRESET signal resets all of the components.
2. After the transceiver block is initialized, the TB_RX_READY signal is asserted high.
3. The JESD204BRX issues a synchronization request by driving the TB_SYNC_N pin low.
4. The JESD204BRX block checks the k28.5 characters transmitted by the JESD204BTX block.
5. The CGS and ILA phase starts after the TB_SYNC_N signal is asserted high.
6. The testbench checks whether the CGS_ERR signal asserts low or not, and completes the code group synchronization phase.
7. The JESD204BRX link asserts the TB_SYNC_N signal to high.
8. After the successful completion of the CGS phase, the JESD204BTX block starts the ILA (Initial Lane Alignment) sequence by transmitting four multi-frames in the following sequence:
   - First frame at TB_TX_SOMF = 0x8
   - Second frame at TB_TX_SOMF = 0x2
   - Third frame at TB_TX_SOMF = 0x8
   - Fourth frame at TB_TX_SOMF = 0x2
9. The JESD204BRX link starts receiving four multi-frames in the following sequence:
   - First frame at TB_TX_SOMF = 0x8
   - Second frame at TB_TX_SOMF = 0x2
   - Third frame at TB_TX_SOMF = 0x8
   - Fourth frame at TB_TX_SOMF = 0x2

   The ILA phase test passes if all JESD204BRX DATA_OUT is properly received with frame alignment.
10. After successful completion of the ILA phase, the JESD204BTX block enters in to the data phase.
11. In the data phase, the following data is fed to the JESD204BTX block:
    PRBS7, PRBS15, PRBS23, and PRBS31 using the PRBS generator.
12. Sine, Square, Saw, and triangular waves are generated from the waveform generator.
13. The data checker checks the received PRBS pattern against the expected PRBS pattern.
14. The waveform output can be viewed in the simulation window on corresponding wave selection as shown in Figure 10, page 13.
15. If no error is detected by the data checker, the testbench issues a TESTBENCH PASSED message stating that the simulation was successful. If an error is detected, the testbench issues a TESTBENCH FAILED message to indicate that the testbench has failed.

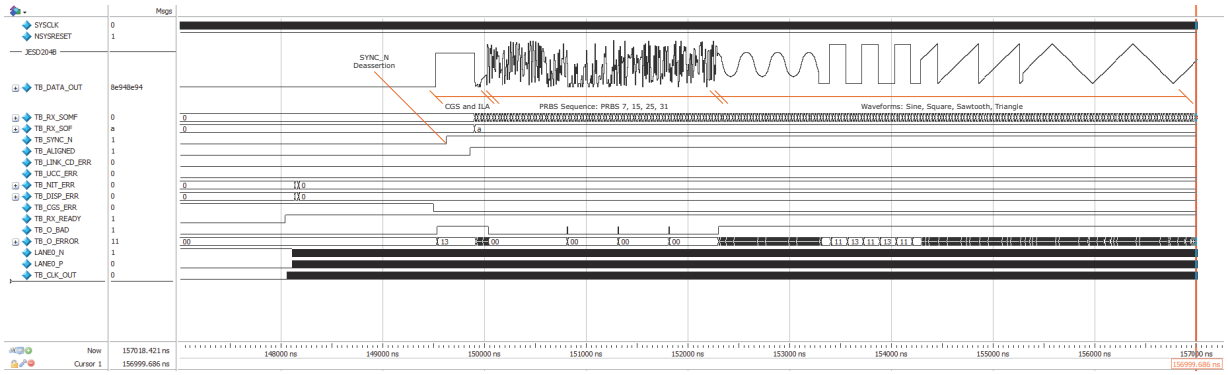
While the simulation is running, you can see the status of the test cases in the **Transcript** window of ModelSim, as shown in the following figure.

Figure 9 • **Transcript Window**



After simulation, the **Waveform** window displays the simulation waveforms as shown in the following figure.

Figure 10 • **Simulation Waveform Window**



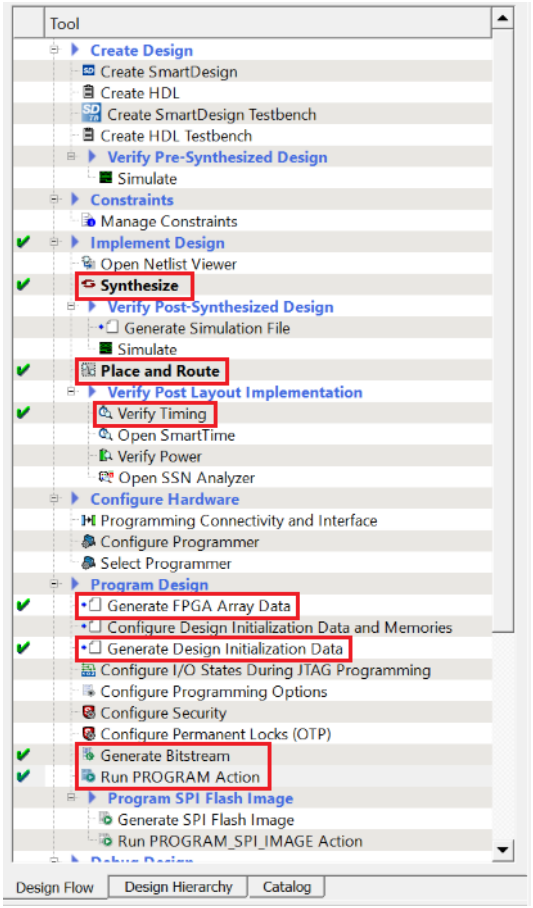
3 Libero Design Flow

This chapter describes the Libero design flow, which involves the following steps:

- Synthesize, page 14
- Place and Route, page 14
- Verify Timing, page 15
- Generate Bitstream, page 16
- Run PROGRAM Action, page 16

The following figure shows these options in the **Design Flow** tab.

Figure 11 • **Libero Design Flow Options**



3.1 Synthesize

To synthesize the JESD204B design:

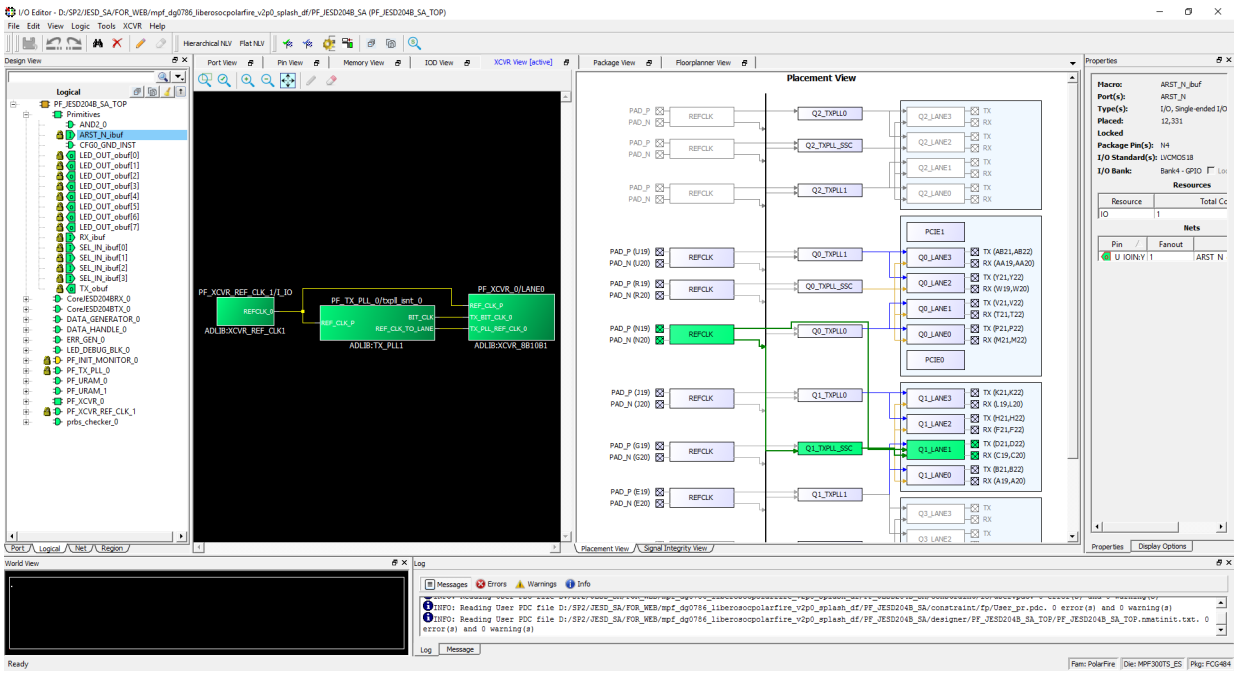
1. Double-click **Synthesize** from the **Design Flow** tab.
   When the synthesis is successful, a green tick mark appears as shown in the preceding figure.
2. Right-click **Synthesize** and select **View Report** to view the synthesis report and log files in the **Reports** tab.

3.2 Place and Route

To place and route the JESD204B design:

1. Using the I/O Editor in the Libero SoC PolarFire Constraint Manager, place TX_PLL, XCVR_REF_CLK, and PF_XCVR as seen in the following figure. In this demo design, the transceiver is placed in Quad 1, Lane 1. For more information about the PolarFire transceiver, see *UG0677: PolarFire FPGA Transceiver User Guide*.

Figure 12 • **I/O Editor XCVR View**



2. Click **Save** to save the placement.
   The PDC file required for placing and routing the design is generated.
3. Double-click **Place and Route** from the **Design Flow** tab.
   When place and route is successful, a green tick mark appears as shown in the Figure 11, page 14.
4. Right-click **Place and Route** and select **View Report** to view the place and route report and log files in the **Reports** tab.

3.2.1 Resource Utilization

The following table lists the resource utilization of the JESD204B loopback design after place and route. These values may vary slightly for different Libero runs, settings, and seed values. For IP-wise utilization, see the respective handbooks.

Table 4 • **Resource Utilization**

Type	Used	Total	Percentage
4LUT	5415	299544	1.81
DFF	4797	299544	1.59
I/O register	0	242	0.00
Logic element	7488	299544	2.50

3.3 Verify Timing

To verify timing:

1. Double-click **Verify Timing** from the **Design Flow** tab.
   When the design successfully meets the timing requirements, a green tick mark appears as shown in Figure 11, page 14.

2. Right-click **Verify Timing** and select **View Report** to view the verify timing report and log files in the **Reports** tab.

3.4 Generate Bitstream

To generate the bitstream:

1. Double-click **Generate Bitstream** from the **Design Flow** tab.
   When the bitstream is successfully generated, a green tick mark appears as shown in Figure 11, page 14.
2. Right-click **Generate Bitstream** and select **View Report** to view the corresponding log file in the **Reports** tab.

3.5 Run PROGRAM Action

After generating the bitstream, the PolarFire device must be programmed. Follow these steps to program the PolarFire device:

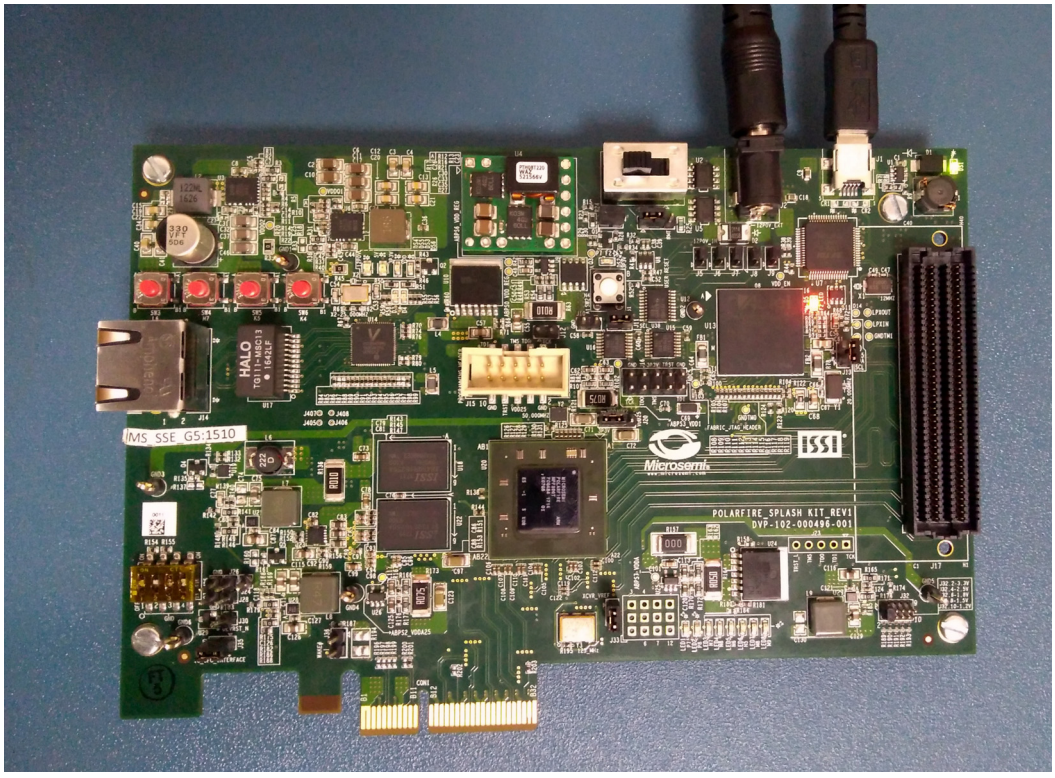
1. Ensure that the jumper settings on the board are same as listed in the following table.

Table 5 • **Jumper Settings**

Jumper	Description	Default
J11	Jumper to select either external JTAG or on-board FTDI chip for programming the device.	Closed
J3	Jumper to select the core voltage.	Open
J10	Jumper to select either FTDI chip or external SPI Flash for programming the device.	Open

2. Connect the power supply cable to the J2 connector on the board.
3. Connect the USB cable from the host PC to the J1 (FTDI port) on the board.
4. Power on the board using the SW1 slide switch.

Figure 13 • **Board Setup**



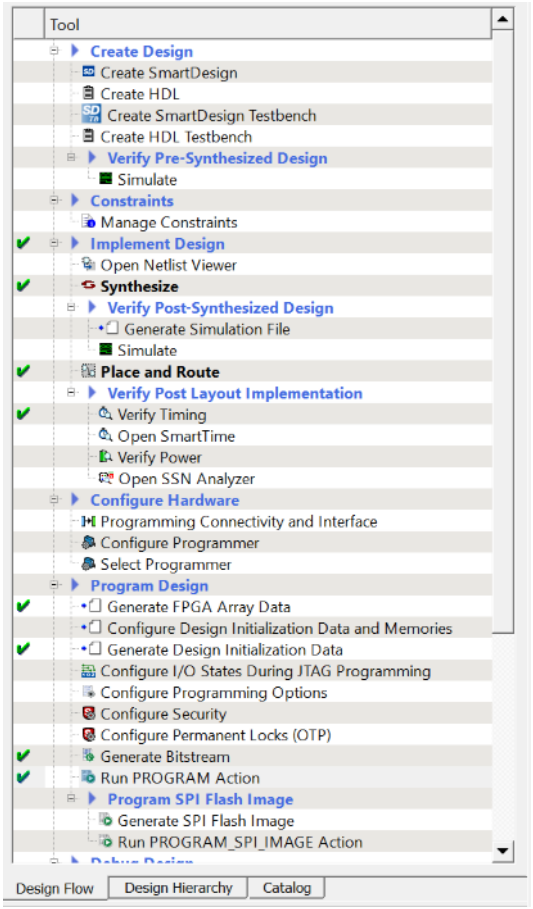
When the board is powered up, power supply LEDs 1 to 4 glow. For more information about LEDs on the PolarFire Splash Board, see *UG0786: PolarFire FPGA Splash Kit User Guide*.

5. Double-click **Run PROGRAM Action** from the Libero **Design Flow** tab.

Right-click **Run Program Action** and select **View Report** to view the corresponding log file in the **Reports** tab.

When the device is successfully programmed, a green tick mark appears as shown in the following figure. See Running the Demo, page 19 for information about how to run the JESD204B standalone demo.

Figure 14 • **Device Programming Completed**



4 Programming the Device Using FlashPro

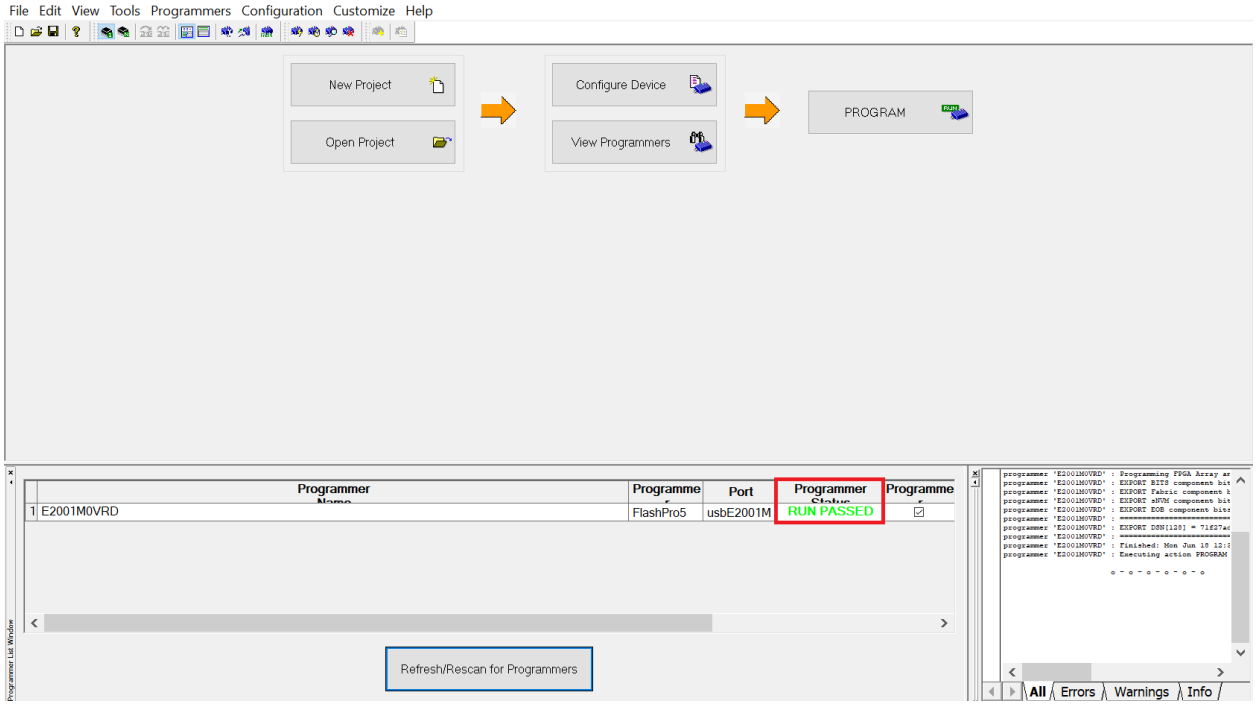
This chapter describes how to program the PolarFire device with the stp programming file using FlashPro. The stp file is available at the following design files folder location:

`mpf_dg0796_liberosocpolarfirev2p2_df\Programing_file`

Follow these steps:

1. Connect the jumpers and set up the PolarFire Splash Board as described in steps 1 to 4 of Run PROGRAM Action, page 16.
2. On the host PC, start the FlashPro software.
3. Click **New Project** to create a new project.
   In the New Project window, do the following, and click OK:
4. Enter a project name.
5. Select **Single device** as the programming mode.
6. Click **Configure Device**.
7. Click **Browse**, and select the `PF_JESD204B_SA.stp` file from the **Load Programming File** window.
8. From the **View Programmer** pane, select the on-board FlashPro5 programmer as shown in the following figure.

Figure 15 • **Selecting the on-board FlashPro5**



9. Click **Program** to program the device.
   The Programmer List Window in the FlashPro, shows the Programmer Name, Programmer Type, Port, Programmer Status, and the Programmer Enabled information.

When the device is programmed successfully, a Run Program PASSED status is displayed. The device is successfully programmed. See Running the Demo, page 19 for information about how to run the JESD204B standalone demo.

5 Running the Demo

This chapter describes how to use the JESD204B GUI to run the JESD204B demo on the PolarFire Splash Board.

5.1 Installing the GUI

To run the demo, you must first install the JESD204B GUI. The GUI allows selection of different PRBS test patterns as input, and displays the JESD204B status signals and the PRBS status received from the board. The Waveform tab of the GUI displays the output waveforms received from the board for each waveform selected as input.

To install the JESD204B GUI:

1. Extract the contents of the `mpf_dg0796_liberosocpolarfirev2p2_df.rar` file.
2. From the GUI folder of the extracted RAR file, double-click the `setup.exe` file.
3. Follow the instructions displayed by the installation wizard to complete the installation.

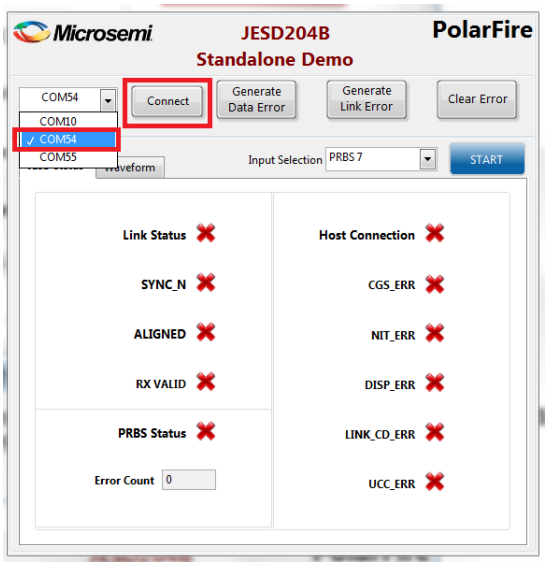
After successful installation, JESD204B_GUI appears on the Start menu of the host PC desktop.

5.2 Running the Demo Design

Follow these steps to run the JESD204B demo.

1. Connect the jumpers and set up the PolarFire Splash Board as described in steps 1 to 4 of Run PROGRAM Action, page 19.
2. In **Device Manager** on the host PC, note the COM port associated with the USB serial converter C. To determine the COM port, check the **Location** field in the properties of each COM port.
3. On the **Start** menu of the host PC, click **JESD204B_GUI**.
4. From the list of COM ports, select the COM port identified in the step 2, and click **Connect**, as shown in the following figure.

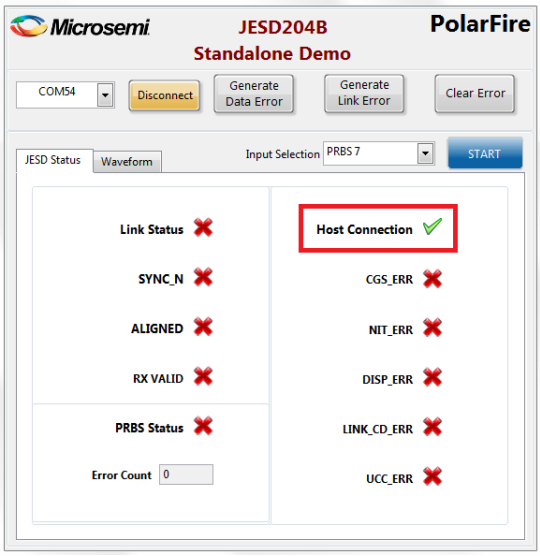
Figure 16 • **COM Port Selection**



Note: Port numbers may vary. In this example, COM port 54 is the correct port to select.

After successful connection, the **Host Connection** indicator turns green, as shown in the following figure.

Figure 17 • **Successful Host Connection**



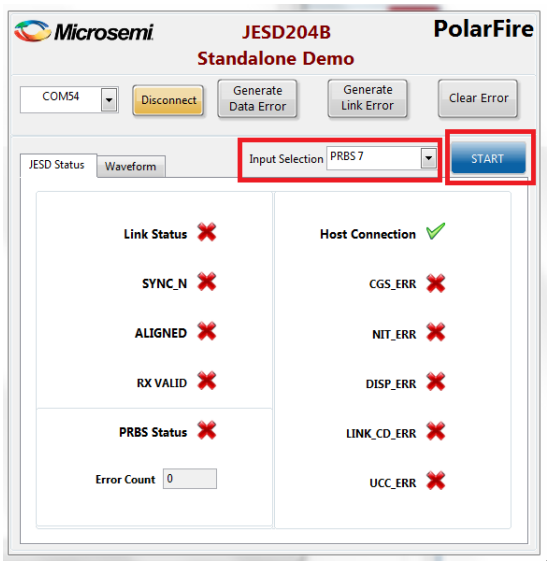
The following table lists the status signals displayed in the JESD204B GUI.

Table 6 • Status Signals in JESD204B GUI

Signal	Description
Host Connection	Shows the UART communication status.
Link Status	Shows the communication link status between TX and RX.
SYNC_N	Indicates the JESD204B status.
ALIGNED	Indicates that all transceiver lanes are aligned.
RX VALID	Indicates that RX data is valid. In 8b10b mode, indicates that comma alignment has occurred and the CDR is locked.
PRBS Status	Indicates PRBS error.
Error Count	Provides the number of e.rrors that occurred during PRBS check
CGS_ERR	Indicates a code group synchronization error.
NIT_ERR	Indicates a “not in table” error.
DISP_ERR	Indicates a disparity error.
LINK_CD_ERR	Indicates a link configuration data mismatch.
UCC_ERR	Indicates an “unexpected control character” error.

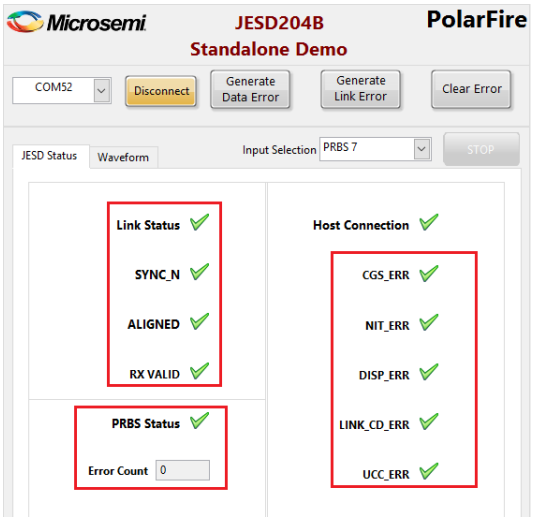
5. From the **Input Selection** list, select the pattern to be transmitted, and click **START**, as shown in the following figure.

Figure 18 • **Pattern Selection**



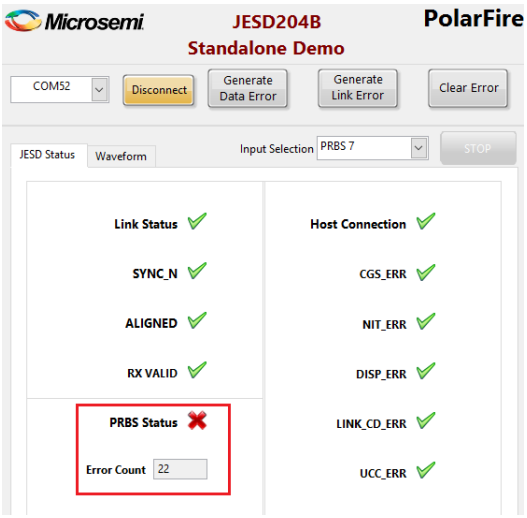
The selected pattern is sent over the serial transmit link and received by CoreJESD204BRX, which checks for errors. At any time, the JESD204B status can be monitored using the status signals on the GUI, as shown in the following figure.

Figure 19 • **Link Status and JESD204B Status**



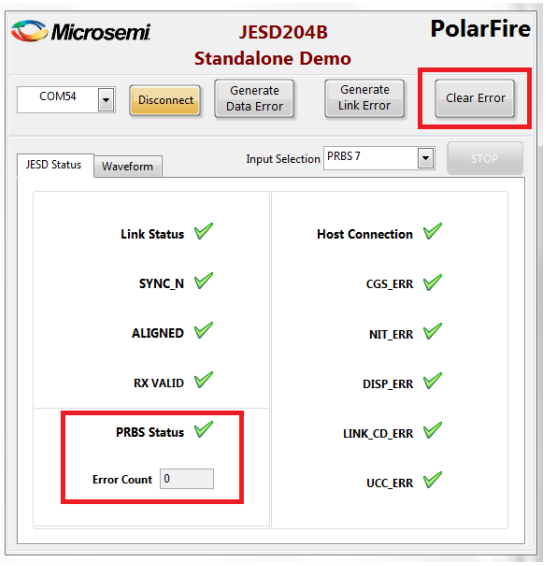
6. To generate an error in the PRBS data, click **Generate Data Error**.
   The **PRBS Status** indicator turns red and the **Error Count** field displays the number of errors, as shown in the following figure.

Figure 20 • **Data Error**



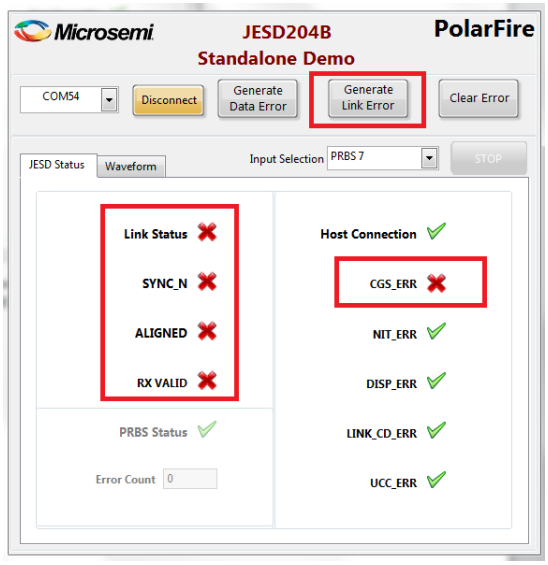
7. Click **Clear Error** to clear the errors in the PRBS data and reset the PRBS status.
   The **PRBS Status** indicator turns green, and the **Error Count** changes to 0, as shown in the following figure.

Figure 21 • **Data Error Cleared**



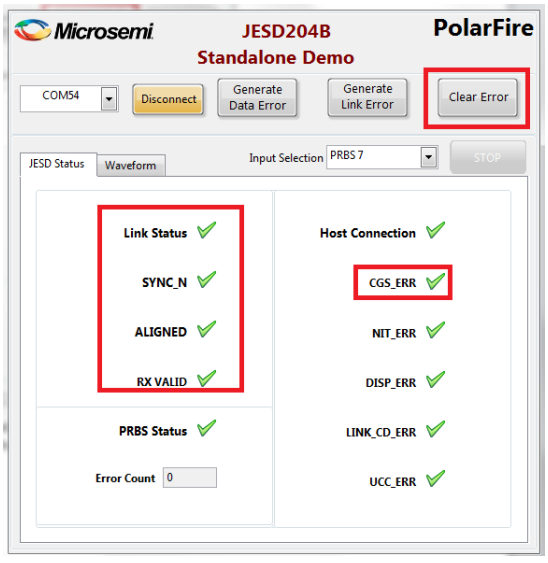
8. To generate a link error between CoreJESD204BTX and the transceiver lane, click **Generate Link Error**.
   The Link Status, SYNC_N, ALIGNED, RX VALID, DISP_ERR, and CGS_ERROR indicators turn red, as shown in the following figure.

Figure 22 • **Link Error**



9. Click **Clear Error** to clear the link error.
   The status indicators turn green, as shown in the following figure.

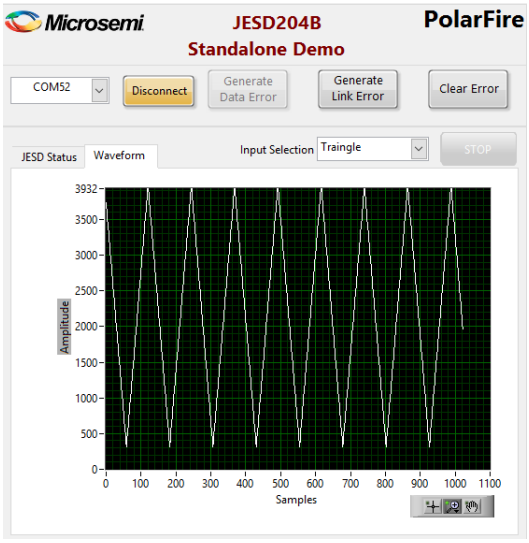
Figure 23 • **Clear Link Error**



10. To change the pattern, select **Triangle** from the **Input Selection** list.
    The selected pattern is sent over the serial transmit link and received by CoreJESD204BRX. At any time, the JESD204B status can be monitored using the status signals on the GUI.

11. Click the **Waveform** tab to view the waveform received from CoreJESD204BRX, as shown in the following figure.

Figure 24 • **Triangle Waveform**



12. Click **Stop** to end the demo and close the GUI.

6 Appendix: References

This section lists documents that provide more information about the JESD204B standard and IP cores used in the demo design.

- For information about the JESD204B interface standard, visit the *JEDEC website*.
- For information about PolarFire transceiver blocks, PF_TX_PLL, and PF_XCVR_REF_CLK, see *UG0677: PolarFire FPGA Transceiver User Guide.*
- For more information about PF_URAM (PF Micro SRAM), see *UG0680: PolarFire FPGA Fabric User Guide*.
- For more information about CoreJESD204BTX, see *CoreJESD204BTX Handbook*.
- For more information about CoreJESD204BRX, see *CoreJESD204BRX Handbook*.
- For more information about Libero, ModelSim, and Synplify, see the *Microsemi Libero SoC PolarFire webpage*.