Reliability Monitoring and Outgoing Quality Report

Q3 & Q4 2018 - ESC Division

July 2019

1 Revision History

1.1 Revision 1.0

Revision 1.0 is Initial Release of this document published in July 2019.

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2 INTRODUCTION

Reliability of Microsemi ESC Division product is ensured via initial process and product qualification and through ongoing reliability monitoring. The reliability activities and results for each quarter are summarized in the Reliability Monitoring and Outgoing Quality Report for that quarter. This report also monitors the mechanical and electrical average outgoing quality levels of Microsemi ESC Division's products. Historical reliability and AOQL results are provided in a graphical format.

3 SCOPE

3.1 General

This document contains the Reliability Monitoring and Outgoing Quality Results for the third and forth quarters of 2018 (i.e., from 1/7/2018 to 31/12/2018).

4 DEFINITIONS

Word	Definition
AOQL	Average Outgoing Quality Level
Assem. X	Single letter code used to identify device assembler
CABGA	Chip Array Ball Grid Array
CAR	Corrective Action Request
DPTM	Double Poly, Triple Metal
EOS	Electrical Over-Stress
ESD	Electro-Static Discharge
Fab X	Single letter code used to identify wafer foundry
Fails	Number of devices failing test
FRR	Failure Request Report
Legacy Devices	Devices inherited by Microsemi ESC Division (PMC-Sierra then) from Sierra Semiconductor
Lot #	Wafer fab lot #
MQFP	Metric Quad Flat Pack
Package	Pin count and style of package
PAR	Preventive Action Request
PBGA	Plastic Ball Grid Array
PLCC	Plastic Leaded Chip Carrier
Process	Minimum geometry, # of polysilicon layers, # of metal layers, presence of ESD Implant on wafer process
Process #	Foundry dependent process code
Qty.	Quantity of devices tested
RR #	Microsemi ESC division number which references full record of reliability results
SAM	Scanning Acoustic Microscopy
SMQFP	Slugged Metric Quad Flat Pack
SPDM	Single Poly, Double Metal
SPMQFP	Thermally enhanced (Spreader) Metric Quad Flat Pack
SPPM	Single Poly, Penta Metal
SPTM	Single Poly, Triple Metal
TEBGA	Thermally Enhanced Ball Grid Array
TMCL	Thermal Cycles

5 REFERENCES

5.1 Standards

Type	Test Name	Standard
Latch	Latch-up	JESD78 (100 mA Class II)
ESD-HBM	ESD	JESD22-A114-B
ESD-CDM	ESD-CDM	JESD22-C101-C
XRAY	XRAY	MIL STD 883D 2012.6
Flam.	Flammability	UL94 V0
Solder	Solderability	MIL STD 883D Method 2003.7
Solvents	Resistance to Solvents	MIL STD 883D 2015.8
Dim.	Physical Dimensions	MIL STD 883D Method 2016
Bond	Bond Strength	MIL STD 883D 2011.7 Cond. D
Shear	Die Shear	MIL STD 883D2019.5
PC	Pressure Cooker	JESD22-A102-B
Cond	Pre Conditioning	JESD-22 (A113)
T/C TMCL	Temperature Cycling	JESD22-A104-B Cond.B (-55 to 125°C), Cond C (-65 to 150°C)
HTOL	Operating Life	JESD22-A108-B (Tj =145°C for static, and 125°C for Dynamic)
HAST	Highly Accelerated Stress Test	JESD22-A110-B (Ta= 130C, 85% RH)
THB	Temperature-Humidity Bias	JA113 (Ta= 85 C. 85% RH)
T/S	Thermal Shock	MIL STD 883D 1011.9 -55 to 125
Moisture	Moisture Content	PMC-1940702
AOQL	Acceptable Outgoing Quality Level	Mil-105D

5.2 Reliability Procedures

- PMC-1930103 IC Qualification Plan
- PMC-1931208 Procedure for Statistical Techniques
- PMC-1930504 Product Failure Analysis Procedure
- PMC-1940220 Reliability Monitoring Plan for ICs

6 FA RESULTS FROM 2018 RELIABILITY MONITORING

2018 Q2 Reliability Monitoring:

One device from QFP package was failed functional after completing 264 hours of uHAST test. Investigation showed this is false failure which was caused by contact issue during ATE testing. Therefore, the failure was excluded from 18Q2 rel mon data.

One device from 28nm node failed functional tests after 1000 hours of HTOL test. ATE datalog showed no power rails or OS pins issues, such observation is typically attributed to random early life failure.

2018 Q3 Reliability Monitoring:

Two devices from 28nm node failed functional tests after 1000 hours of HTOL test, datalog review also found leakage failure as well. However, FA result revealed the tester findings of leakage failure cannot be replicated at curve trace. Therefore, this failure was concluded to be caused by random early life failure.

2018 Q4 Reliability Monitoring:

One device from FCBGA package failed massive scan failure after TCB test, shmoo data confirmed hard failure. While this is a valid die level failure, the FA result showed to be inconclusive as such failure is unlikely attributed by package stress.

7 HTOL FAILURE RATE CALCULATION

$$FailRate = \frac{ChiSq}{2 \times N \times t \times AF}$$

Where: ChiSq = Chi Squared Distribution; function of CL (confidence level) and number of failures:

- FailRate = FIT rate = # of failures / billion device-hours
- N = Number of units HTOL tested
- t = Duration of HTOL testing
- AF = Acceleration Factor = AF(T) x AF(V)
- AF(T) = Temperature Acceleration Factor from Test to Use Conditions
- AF(V) = Voltage Acceleration Factor

$$AF(T) = \exp\left[\frac{Ea}{k}\left(\frac{1}{Tuse} - \frac{1}{Tstress}\right)\right]$$

Where: Ea = 0.7eV

- k = Boltzmann’s constant
- Tuse = 55C = 328 K
- Tstress = 140 C (413 K) for static HTOL and 125 C (398 K) for dynamic HTOL

$$AF(V) = \exp\left[\beta \times (Vstress - Vuse)\right]$$

Where: β = 10.9 (0.13um), 12.3 (90nm), 13.4 (65nm), 7.00 (55nm), 20.8 (40nm), 20.8 (28nm) according to fab reliability data

- Vstress = stress voltage
- Vuse = use voltage

8 DPM CALCULATIONS

Microsemi ESC Division calculates the DPM (Defects Per Million) based on the number of samples selected for QA testing from every lot. The sampling plan is based on the MIL-105D-STD and Microsemi samples for a 0.1% AOQL

Table 1 AOQL Sampling Plan

AOQL	0.1%		
Lot Size	**Sample Size**	**Accept**	**Reject**
2-8	all	0	1
9-15	all	0	1
16-25	all	0	1
26-50	all	0	1
51-90	all	0	1
91-150	125	0	1
151-280	125	0	1
281-500	125	0	1
501-1200	125	0	1
1201-3200	125	0	1
3201-10000	125	0	1
10001-150K	200	0	1

To calculate DPM:

$$DPM = \frac{TotalNumberofFails}{TotalSampleSize} \times 1{,}000{,}000$$

9 Q3 & Q4 2018 RELIABILITY MONITORING & OUTGOING QUALITY

The following pages contain the Reliability Monitoring and Outgoing Quality Results for the third and fourth quarter of 2018.

9.1 HTOL Data by Process

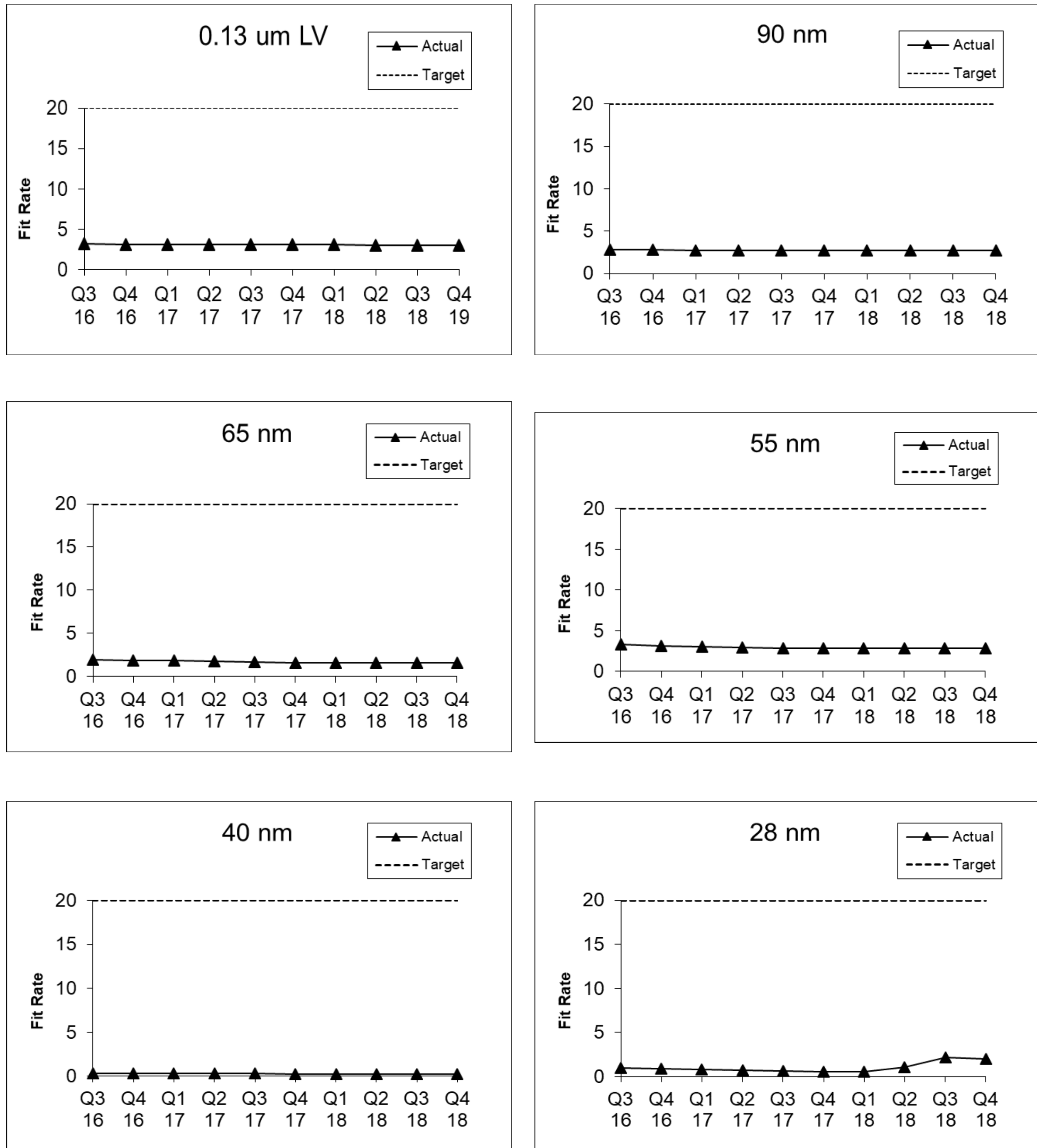
Table 2 High Temperature Operating Life (HTOL) Data

Technology	No. of Quarters of Data Included	No. of Samples	Device Hours at Burn-in Temperature	Device Hours at Tj=55 deg C	Failures in Quarters Q3 & Q4	Total Cumulative Failures Observed	FIT RATE (60% Confidence Level)	FIT RATE (90% Confidence Level)	Test Condition
0.35 um SPTM & DPTM	53	8,385	7,864,172	7.3673E+08	0	2	4.22	7.22	A, Vstress=3.63V
0.25 um SPTM & DPTM	29	2,728	2,723,000	2.7230E+06	0	0	4.03	10.12	A, Vstress=2.75V
0.25 um LV	31	8,355	1,191,932	4.7571E+09	0	8	1.98	2.73	B, Vstress=3.3V
0.18um LV	44	28,958	5,855,325	3.3082E+09	0	13	4.42	5.73	B, Vstress=2.0V
0.18 um G	48	4,888	4,710,544	1.9966E+09	0	1	1.01	1.95	B, Vstress=1.89V
0.13um G	30	3,140	3,140,000	1.2471E+09	0	3	3.35	5.36	B, Vstress=1.38V
0.13um LV	55	9,725	3,487,341	1.3851E+09	0	3	3.01	4.82	B, Vstress=1.45V
90nm	59	2,114	2,114,000	1.9160E+09	0	4	2.73	4.17	B, Vstress=1.20V
65nm	25	1,120	1,120,000	1.2653E+09	0	0	1.60	3.07	B, Vstress=1.25V
55nm	15	1,099	1,099,000	3.2499E+08	0	0	2.82	7.09	B, Vstress=1.10V
40nm	28	1115	1,115,000	3.6503E+09	0	0	0.25	0.63	B, Vstress=1.08V
28nm	11	635	635,000	2.0782E+09	2	3	2.01	3.21	B, Vstress=1.08V

Test Condition A: JESD22-A108-B. Tj = 140ºC for static HTOL and 125ºC for dynamic HTOL. FIT Rates and Device Hours Calculated using Tj = 55ºC, Ea = 0.7 eV; voltage acceleration not included in FIT rate.

Test Condition B: JESD22-A108-B. Tj = 125°C for dynamic HTOL. FIT Rates and Device Hours Calculated using Tj = 55°C, Ea = 0.7 eV

Figure 1 HTOL FIT Rate Trend (60% Confidence level) – 0.13um LV, 90nm 65nm, 55nm, 40nm & 28nm processes.



9.2 Temperature Cycle Data by Package

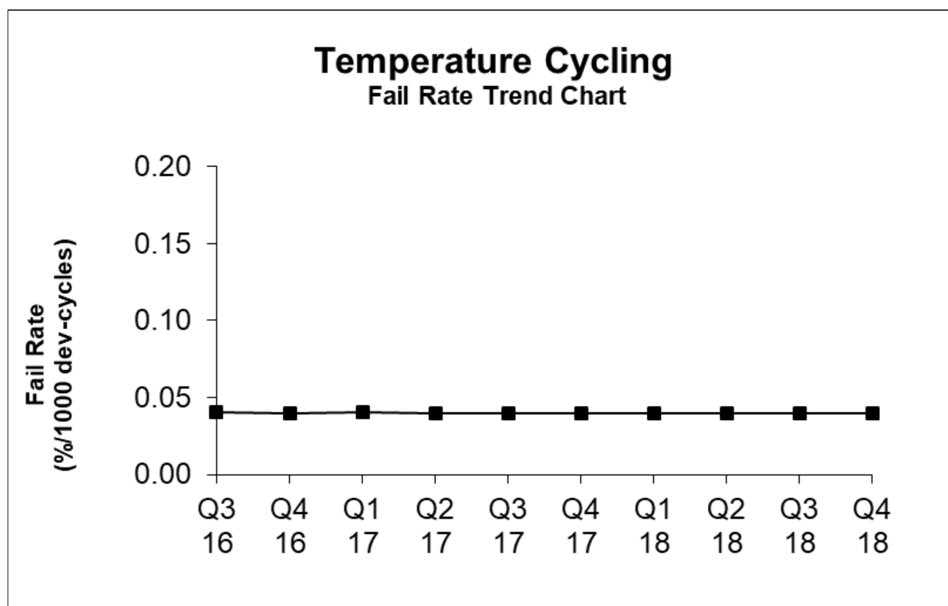
Table 3 Temperature Cycle Data

Package	No. of Quarters of Data Included	Total Samples	Device Cycles	Failures in Quarters Q3 & Q4	Total Cumulative Failures Observed	Failure Rate %/1000 Dev-Cycle	Test Condition	Note
QFN/ QFP/ EPAD	79	9,114	1.0278E+08	0	7	0.0068%	B	
BGA	84	20,255	1.9679E+07	0	31	0.1575%	B	
FCBGA	64	7,553	7.5530E+06	1	3	0.0265%	B	
HSBGA	51	3,359	3.3590E+06	0	1	0.0298%	B	
TBGA	45	4,410	1.2878E+07	0	1	0.0078%	B	

Test Condition B: JESD22-A104-B, Condition B; -55 to +125 °C, 1000 cycles. This test condition is applied on all devices except for devices with smqfp package and devices with mask sets of TM4093B, TM7098C and TM2555D. For these devices a test point at 400 cycles is used as a failure criteria gate.

Test Condition C: JESD22-A104-B, Condition C; -65 to +150 °C, 500 cycles

Figure 2 Temperature Cycling Data Trend (all technologies) – Cumulative Rate

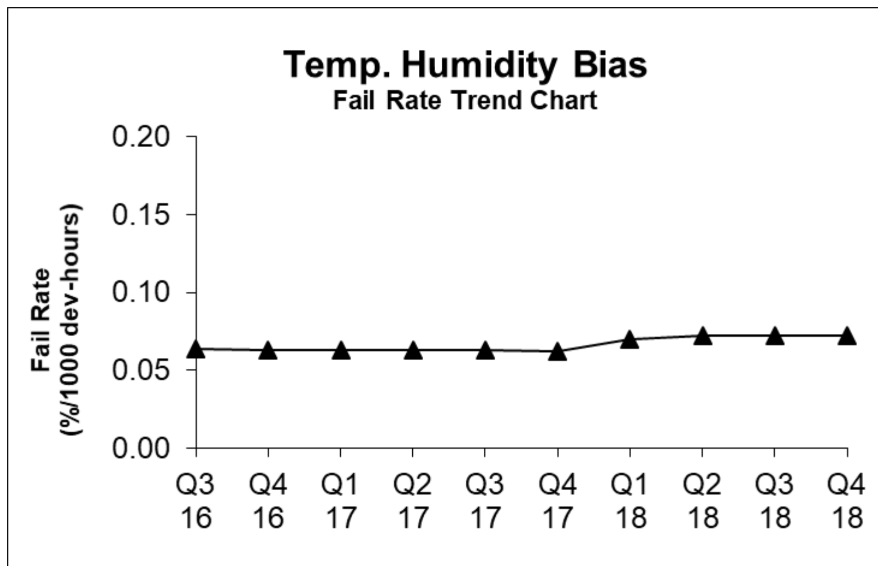


9.3 THB/HAST/UHAST Data by Package

Table 4 THB / HAST / UHAST Data

Package	No. of Quarters of Data Included	Total Samples	Device Hours	Failures in This Quarter	Total Cumulative Failures Observed	Failure Rate %/1000 Dev-Hours
QFP	89	17,830	1.6760E+07	0	12	0.0716%
BGA	83	13,322	1.2552E+07	0	5	0.0398%
FCBGA	49	7,399	3.6601E+06	0	3	0.0820%
HSBGA	42	2,480	1.6851E+06	0	3	0.1780%
TBGA	8	400	4.0000E+05	0	0	0.0000 %

Figure 3 THB Data Trend (all technologies) – Cumulative Rates

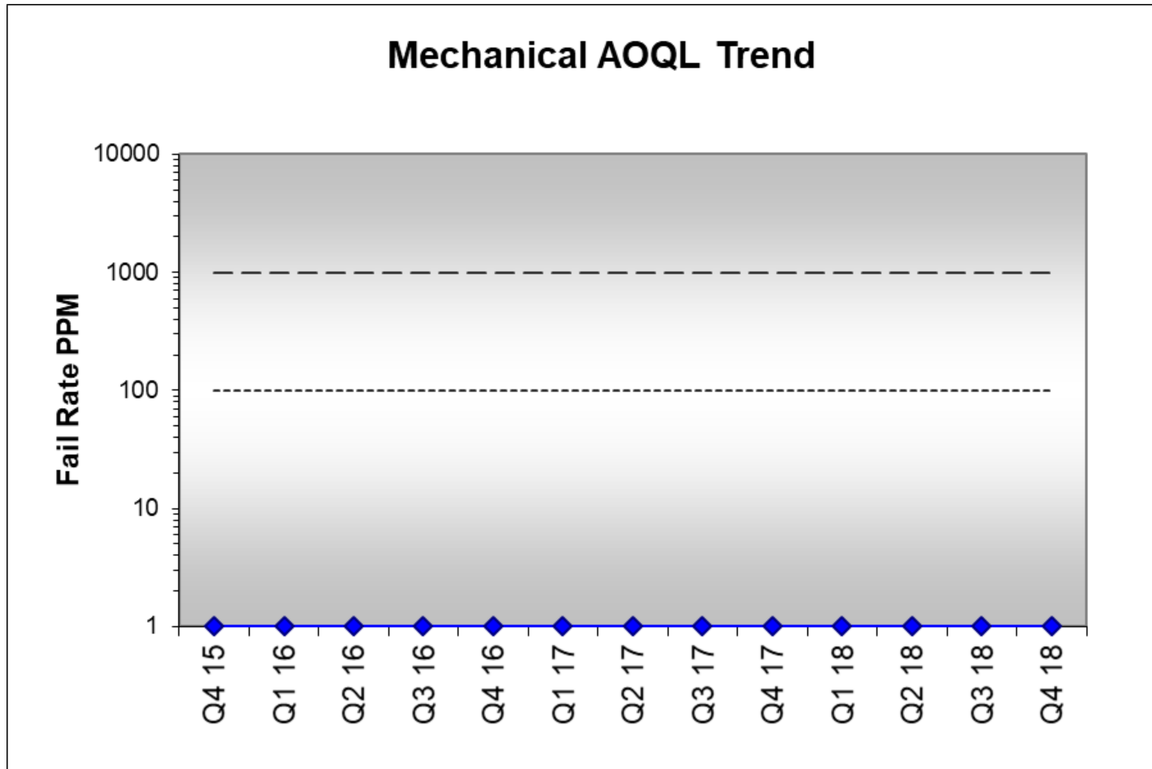


10 MECHANICAL AOQL LEVEL

Test Conditions: Package Drawings as per PMC-1970340, PMC-1960133, PMC-2020755, PMC-2001184.

No mechanical QA failures in Q3 & Q4 2018.

Figure 4 Mechanical AOQL Trend Chart

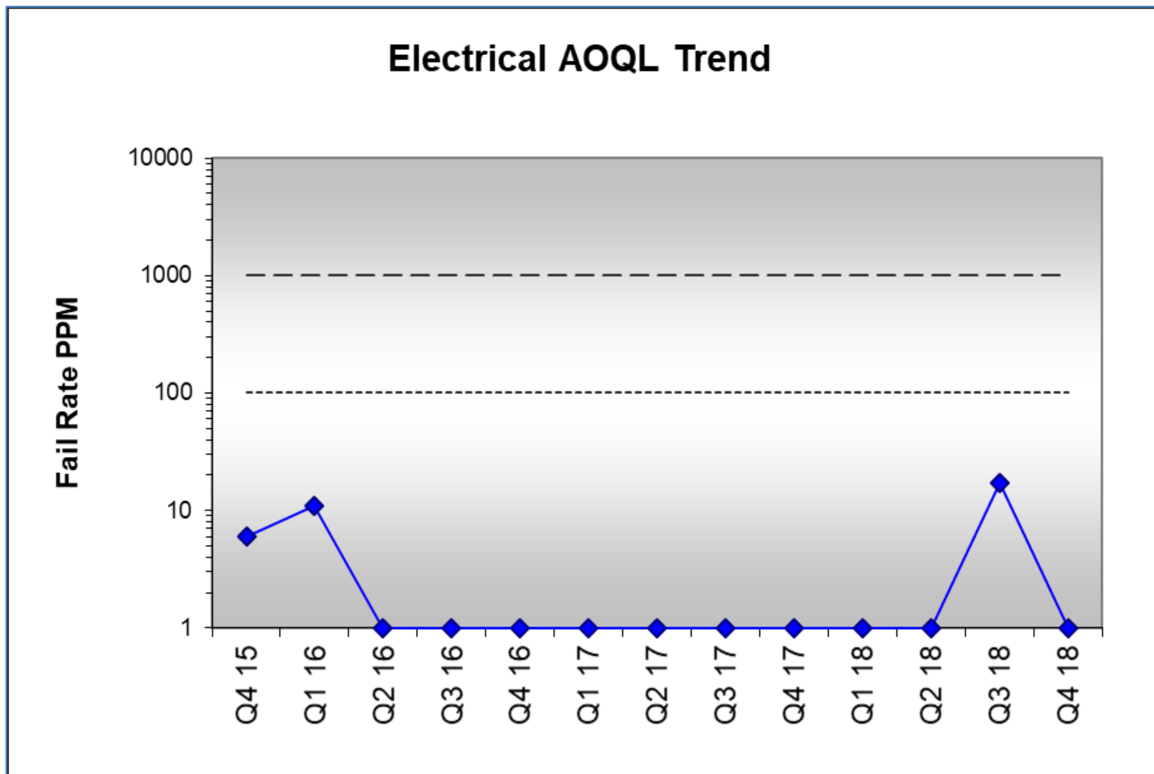


11 ELECTRICAL AOQL LEVEL

Test Conditions: Per device specific QA test work instructions.

There are 2 incidents of QA electrical failure reported in Q3 2018. The affected lots were retest with 100% QA testing again and all parts are passing without any issue.

Figure 5 Electrical AOQL Trend Chart



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