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RTG4 Radiation Update
Space Forum 2017

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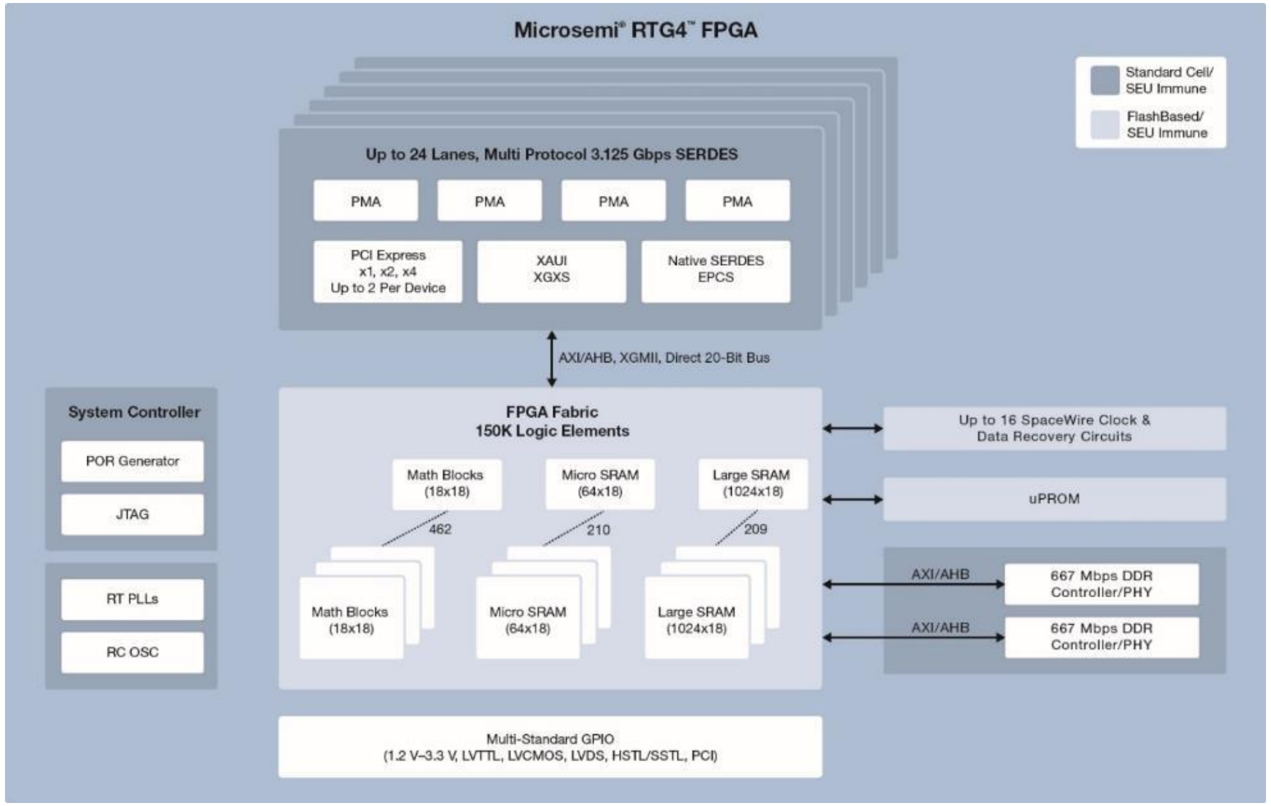
Agenda

- Introduction
- Chip Level TID and SEE Update
- Single Event Effects Update
  - Fabric Circuit Heavy-Ion Testing
  - PLL and SERDES Heavy-Ion Testing
  - Reprogramming in Space Flight
- Summary and Further Radiation Testing

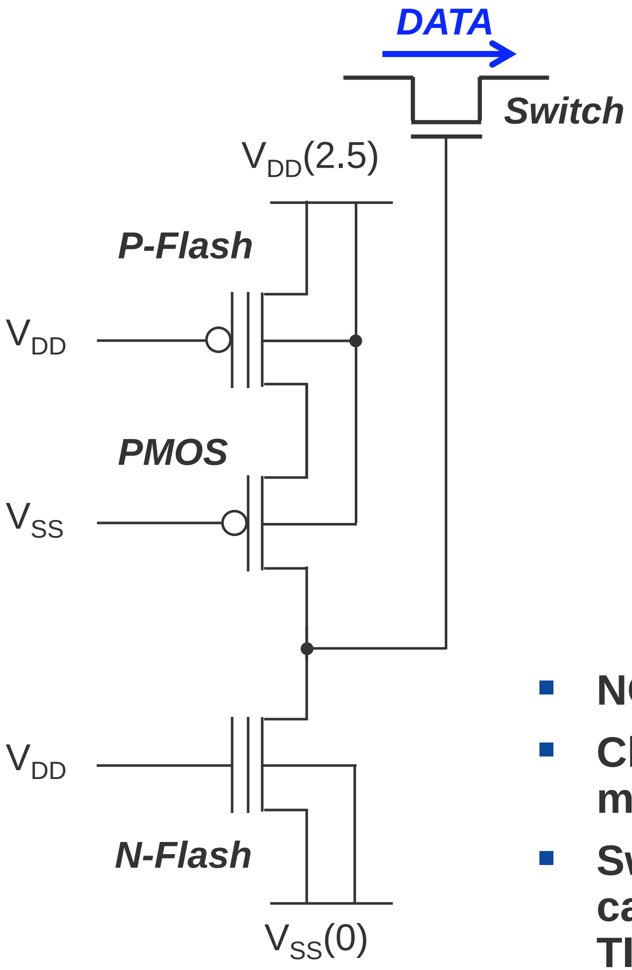
RTG4 FPGAs

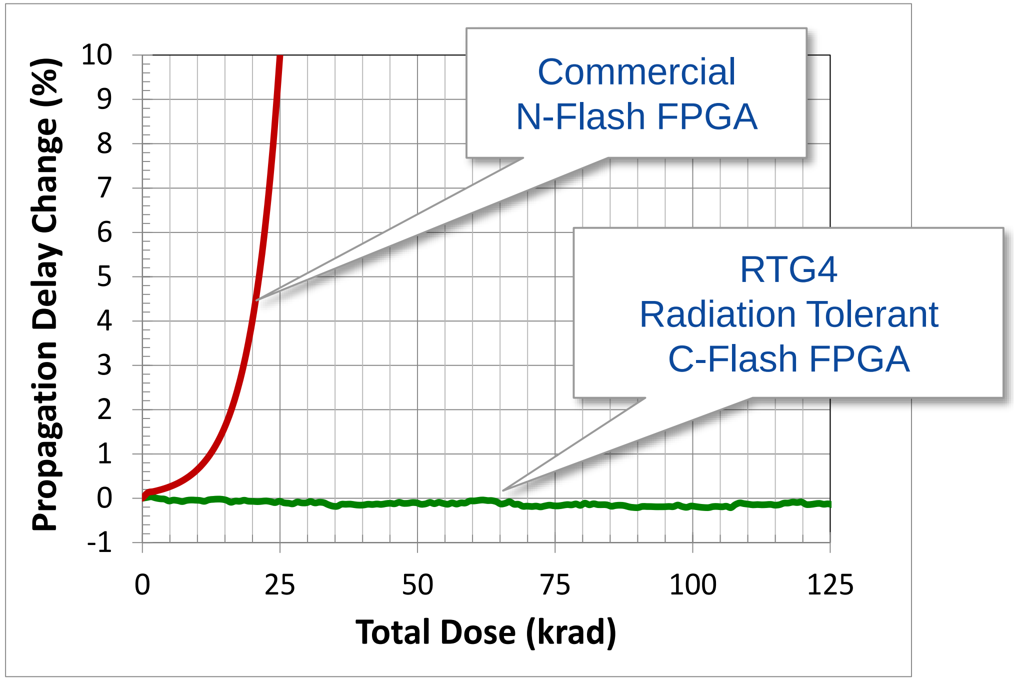


- Radiation tolerant Flash-based FPGA manufactured by UMC 65nm technology
- High-Speed Signal Processing
  - 300 MHz
  - 150K LE (STMRFF)
  - 5 Mbit SRAM (EDAC)
  - 462 Multipliers (DSP)
  - RT-PLL
  - 24 x 3.125 Gbps SERDES
- Hardened for both TID and SEE
  - TID > 100 Krad
  - SEL immune
  - SEU/SET/SEFI

Flash-Cell Radiation Hardening

TID and SEE Hardened C-Flash Cell

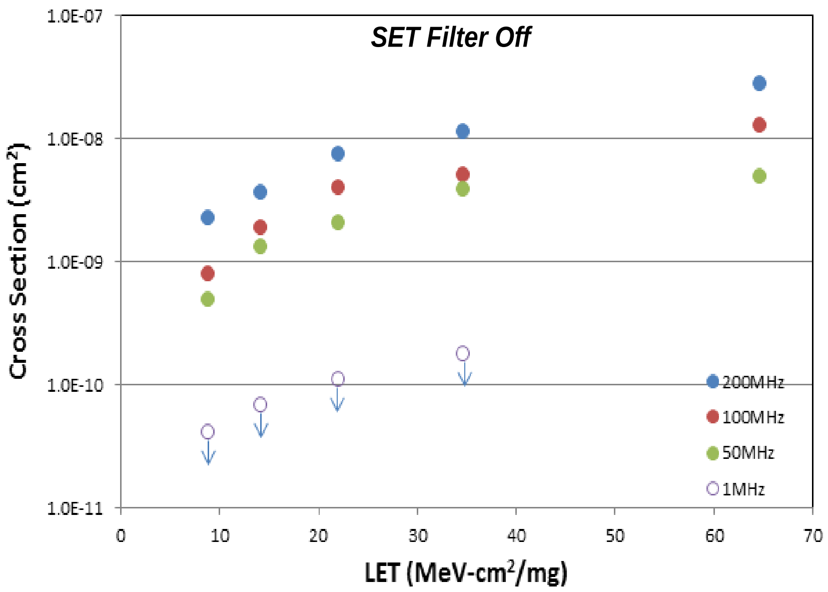


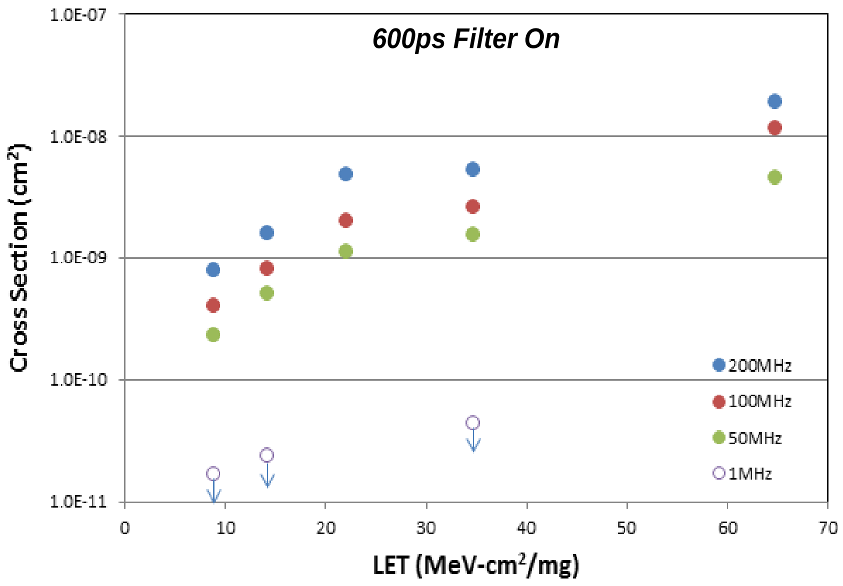


- **NOR Flash architecture**
- **Charge storage for N-Flash or P-Flash is >10X of N-Flash memory; small V_T change (ΔV_T) by HI**
- **Switch has no degradation until Flash changes state and can tolerant V_T shift but still maintain performance: TID > 125krad**
- ***Reprogramming succeeds after irradiated high LET-ion with high fluence (can reprogram every irradiated part)***

Fabric Circuits Radiation Update

Fabric FF (STMRFF) SET Filter Enable—2X Error Reduction





- No error observed at 1 MHz

⇒ Flip-flop TMR works to eliminate SEU at 1 MHz

⇒ Errors observed at 50 MHz, 100 MHz, and 200 MHz were all SET and not SEU

- Filter reduced SET by half

Device Family	Error Rate for GEO Min (Errors/bit-day)
SmartFusion2 @ 1MHz	1.76×10^{-7}
RTG4 @ 1MHz	2.60×10^{-12}
RTG4 @ 200MHz	4.20×10^{-8}

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LBNL—RTG4 Mathblock SET Filter Testing

- Mathblock design with SET Filter enabled vs disabled are tested
  - Parallel Math Block Chains (25 stages)
    - Configured using cascade mode uses dedicated math block routing—Not going through the fabric
    - Frequencies : 50 MHz and 100 MHz
    - SET filter enabled (600 ps) vs disabled

- Hard Multiplier Accumulator macro (accumulation enabled) was tested with heavy ion and the sensitivity is confirmed for LET as low as 2.8 MeV.cm2/mg
  - The (SET/SEU) errors accumulate and a reset is required

- Hard Multiplier AddSub macro (accumulation disabled)
  - Errors do not accumulate, SET errors are captured but no reset is necessary
  - SET Filter enabled vs. SET Filter disabled are tested
  - SET Filter is very efficient
    - The SET filter is able to mitigate most of the errors up to an LET of ~ 37 MeV.cm2/mg

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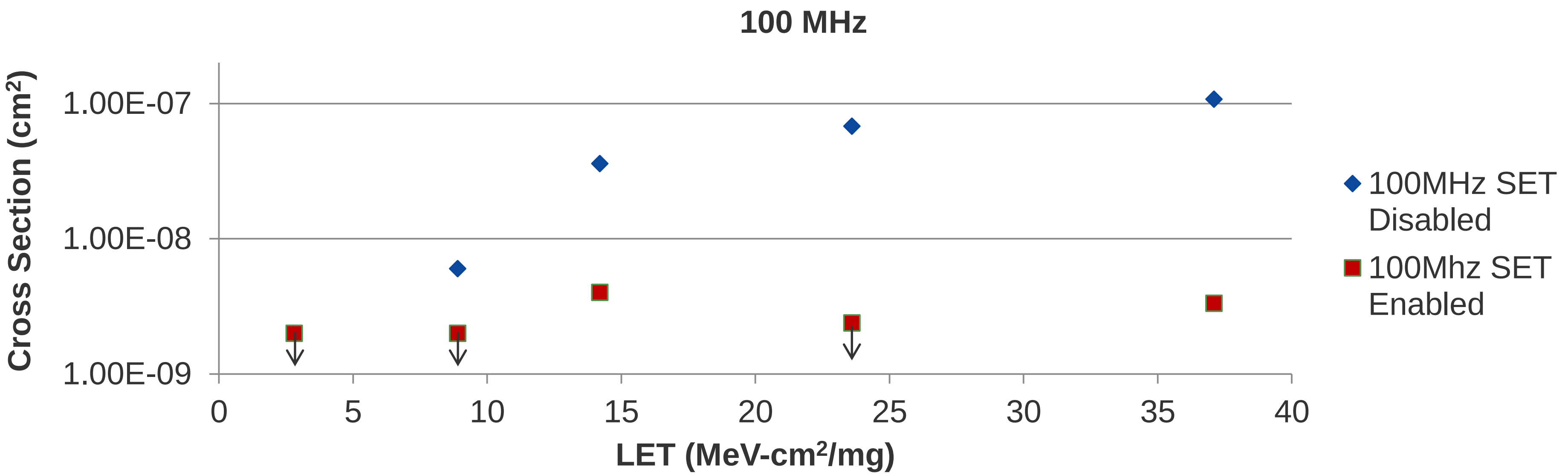
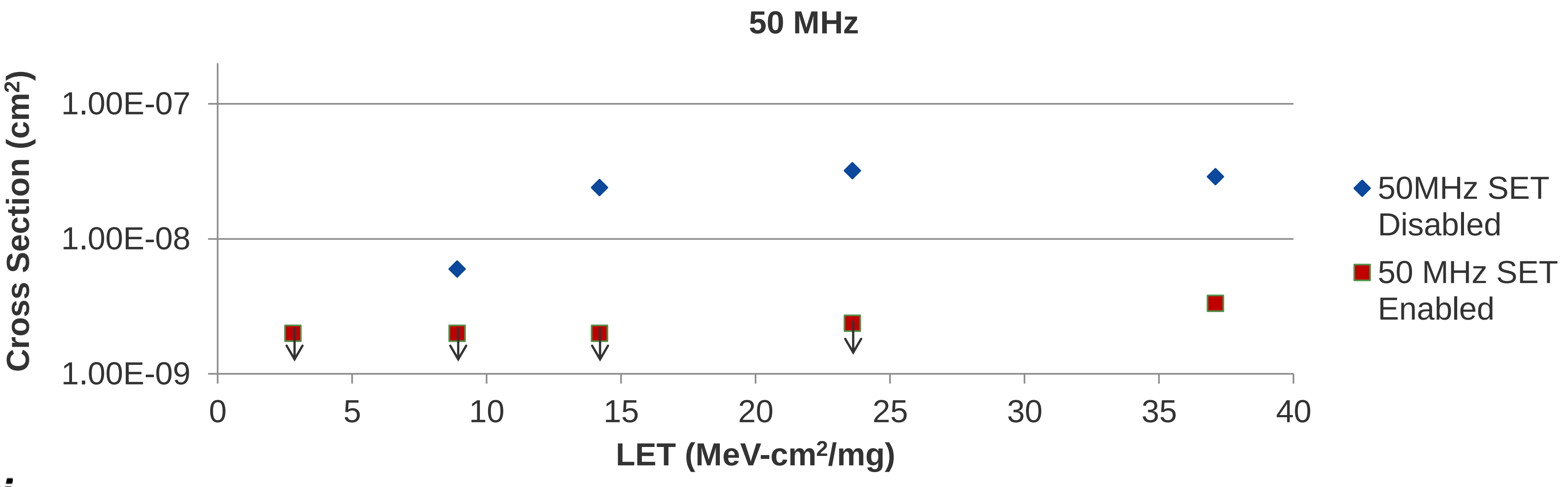
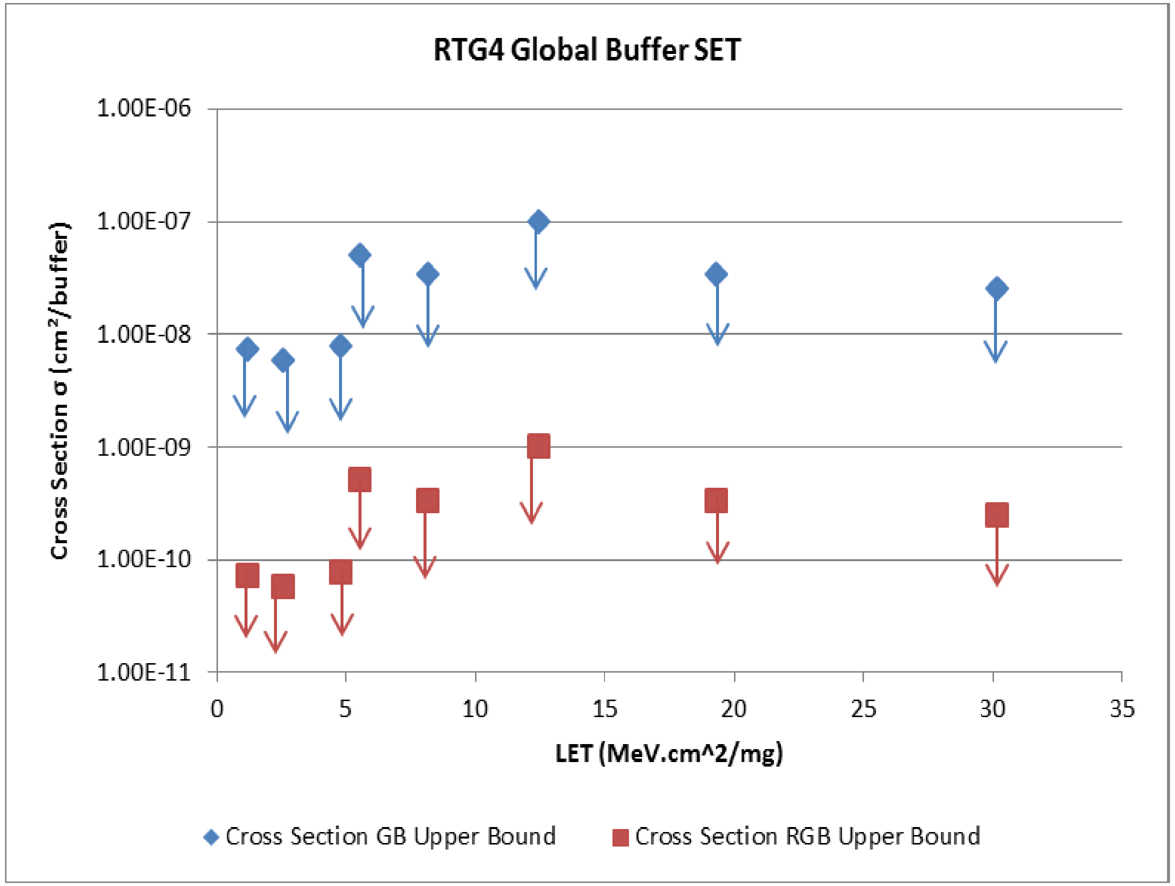
Math Blocks SET Filter Enable—10X Error Reduction





Global Clock Buffer

- No SET observed in Global Buffer or Row Global Buffer for LET < 30 MeV-cm2/mg

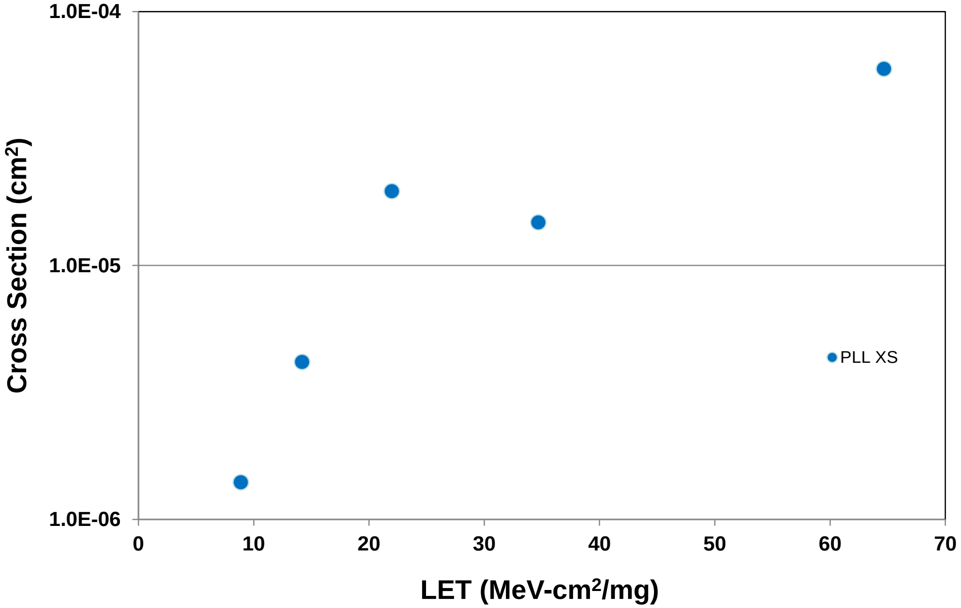


Notes: Data points indicate testing limits.

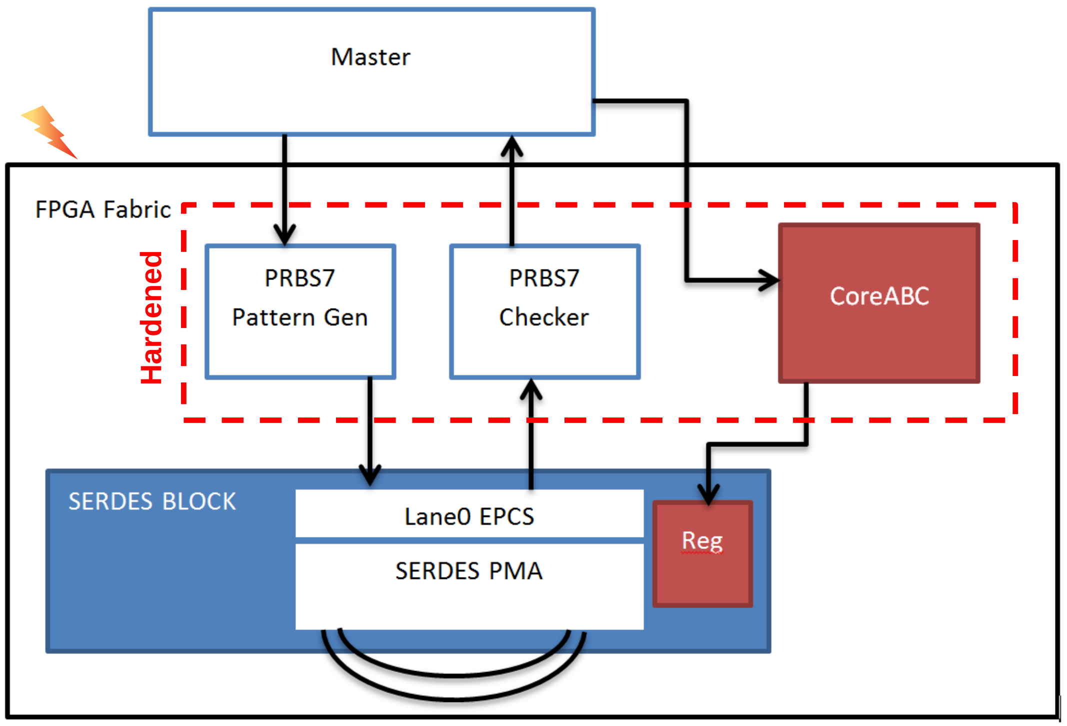
PLL and SERDES Radiation Update

PLL

- PLL Single Event Functional Interrupt (SEFI) is defined by PLL loss of lock
- Heavy-Ion SEE Testing Results
  - PLL lost lock and self-recovers at LET < 65 MeV-cm2/mg
  - PLL lost lock and can be recovered by reset at LET = 65 MeV-cm2/mg
  - Lock loss < 100 us
- More testing is planned



SERDES SEE Test and SEFI Auto-Recover



1. Controller in external master chip manages the testing system.
2. Configuration register in SERDES is SEE hardened but has upset.
3. When SERDES SEFI occurs, controller detects the event based on looped back data.
4. A command is sent to on-chip CoreABC, also built from SEE-hardened fabric logics, to refresh the configuration.

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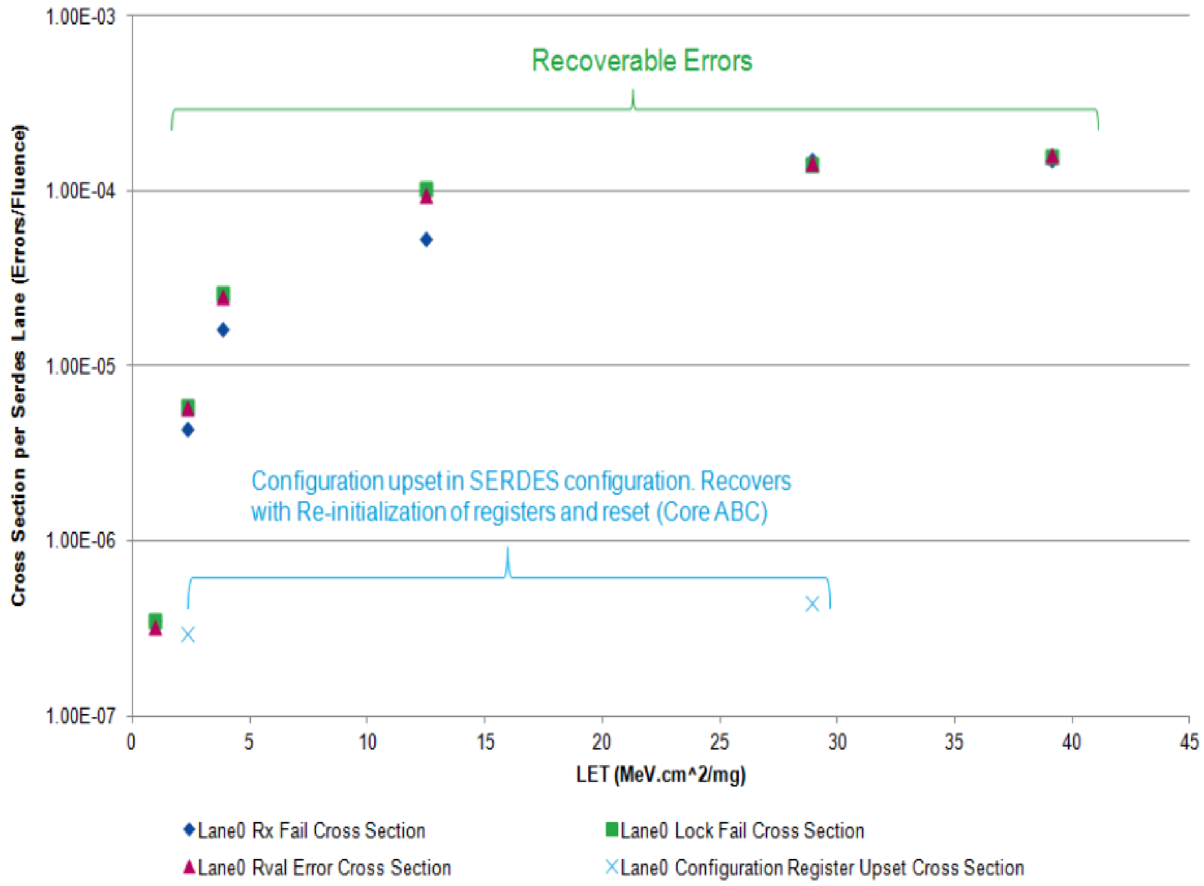
SERDES SEFI Results

- SERDES SEFI is defined by loss of link
  - Several signals were monitored
  - Loss of link is when returned data is invalid for 2+ consecutive cycles



SERDES Summary

- No DEVRST_N was required to recover link loss
- Most SEFI were self-recoverable
  - Others required reinitializing SERDES configuration registers using CoreABC
- Link loss was recoverable with duration in sub-millisecond range
- Plan for next testing:
  - Improve SERDES test design and measurement
    - Increase counter register size to prevent error saturation
    - Collect bit error rate with error correction for multiple transmissions

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In-Flight Reprogramming—In-Beam Reprogramming Test

In-Beam RTG4 Reprogramming

- FlashPro used by customers
- Reprogramming in beam often gets interrupted
- No damage at LET ≤ 30.5
- Reprogram off-beam always successful after tried in beam, implying no destructive damage

Run	Effective LET	Effective Flux (Ion/cm^2/s)	Fluence until Prog Fail	Fluence (Ion/cm^2)	Reprogram Attempts	Reprogram Passed	Reprogram Functional	Off-Beam Reprogram Pass
23	1.2	1.00E+04	1.40E+06	1.40E+06	1	0	0	1
24	1.2	1.00E+04	3.40E+05	1.40E+06	1	0	0	1
25	1.2	1.00E+04	1.80E+05	6.00E+05	1	0	0	1
26	2.6	1.00E+04	4.30E+05	6.00E+05	1	0	0	1
27	8.2	1.00E+04	2.40E+05	1.41E+06	1	0	0	1
28	8.2	1.00E+04	2.55E+06	1.00E+07	8	0	0	1
29	11.6	1.00E+04	8.62E+05	1.00E+07	8	0	0	1
30	19.3	3.00E+03	4.86E+05	2.20E+06	3	0	0	1
31	19.3	3.00E+03	1.16E+06	2.20E+06	6	0	0	1
32	30.5	9.00E+02	2.99E+05	2.00E+06	12	0	0	1
33	30.5	9.00E+02	3.87E+05	2.00E+06	13	0	0	1
34	30.5	9.00E+02	3.36E+05	2.00E+06	13	0	0	1

- This data implies that users can attempt re-programming multiple times until successful.
- In space, the probability of a heavy-ion strike is low during short-cycle reprogramming

In-Beam Reprogramming Error

- Example: Run 24, Bit stream error

In- Beam

```
programmer '87254' : Scan Chain...
programmer '87254' : Scan Chain PASSED.
programmer '87254' : Executing action PROGRAM
programmer '87254' : EXPORT ISC_ENABLE_RESULT[32] = 00004404
programmer '87254' : EXPORT CRCERR: [1] = 0
programmer '87254' : EXPORT ECCRCVR: [1] = 0
programmer '87254' : TEMPGRADE: ROOM
programmer '87254' : EXPORT TEMP: [8] = 44
programmer '87254' : Programming FPGA Array...
programmer '87254' : Bitstream Error.
programmer '87254' : blockNo: 12082
programmer '87254' : EXPORT DATA_STATUS_RESULT: [32] = 22a04024
programmer '87254' : EXPORT ERRORCODE: [5] = 04
programmer '87254' : EXPORT BSERRCODE: [8] = 40
programmer '87254' : EXPORT READ_DEBUG_INFO[128] = c444f07f0000000000000000000010001
programmer '87254' : ================================================================================
programmer '87254' : EXPORT DSN[128] = 0000000000000000014b39070006001c
programmer '87254' : ================================================================================
programmer '87254' : ================================================================================
programmer '87254' : EXPORT DSN[128] = 00000000000000000000000000000000
programmer '87254' : ================================================================================
programmer '87254' : Finished: Wed Jul 01 21:45:19 2015 (Elapsed time 00:02:17)
programmer '87254' : Executing action PROGRAM PASSED.
```

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Off-Beam

```
programmer '87254' : Scan Chain...
programmer '87254' : Scan Chain PASSED.
programmer '87254' : Executing action PROGRAM
programmer '87254' : EXPORT ISC_ENABLE_RESULT[32] = 00004404
programmer '87254' : EXPORT CRCERR: [1] = 0
programmer '87254' : EXPORT ECCRCVR: [1] = 0
programmer '87254' : TEMPGRADE: ROOM
programmer '87254' : EXPORT TEMP: [8] = 44
programmer '87254' : Programming FPGA Array...
programmer '87254' : ================================================================================
programmer '87254' : EXPORT DSN[128] = 0000000000000000014b39070006001c
programmer '87254' : ================================================================================
programmer '87254' : Finished: Wed Jul 01 21:51:23 2015 (Elapsed time 00:03:59)
programmer '87254' : Executing action PROGRAM PASSED.
```

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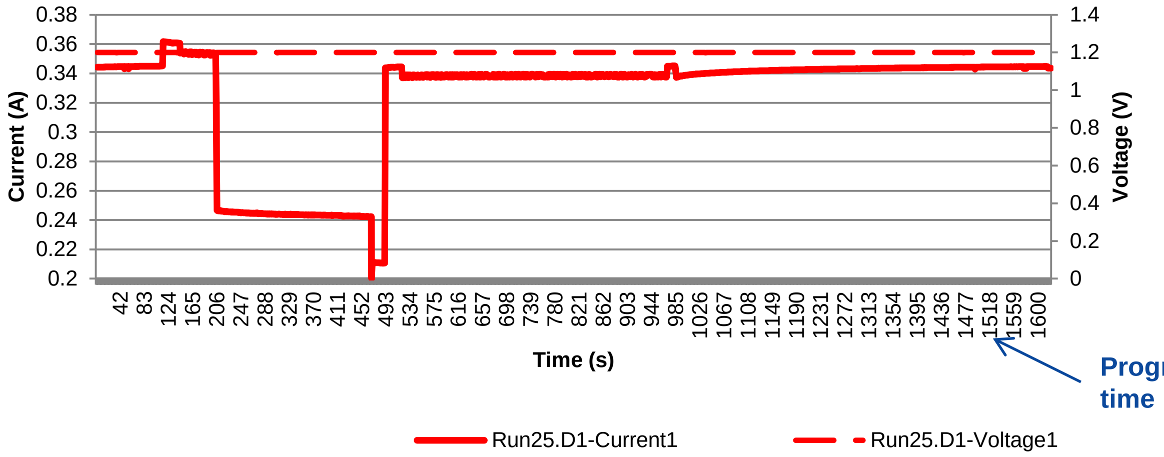
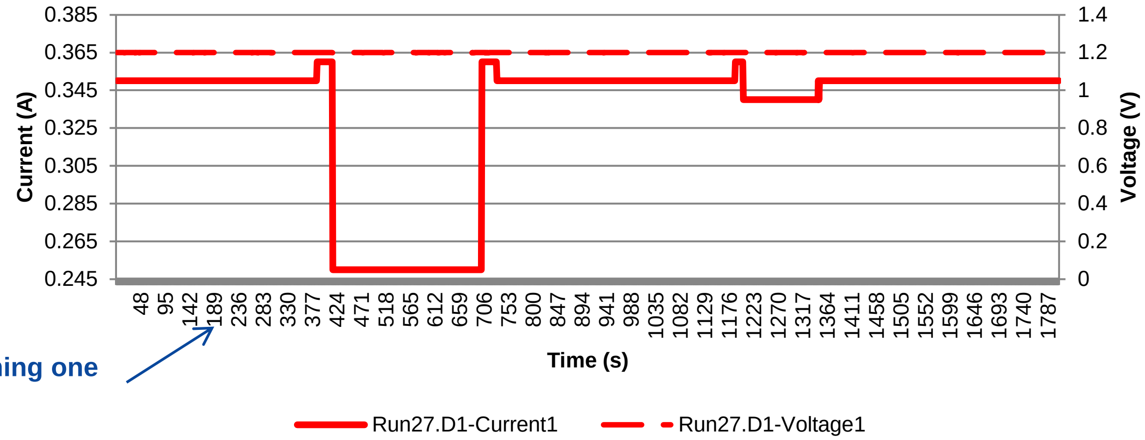
In-Beam Reprogramming SEFI—Register Upset

Run 25, Nominal, Tilt: 0 LET: 1.23, Fluence: 6.00E+05, Temperature: Room



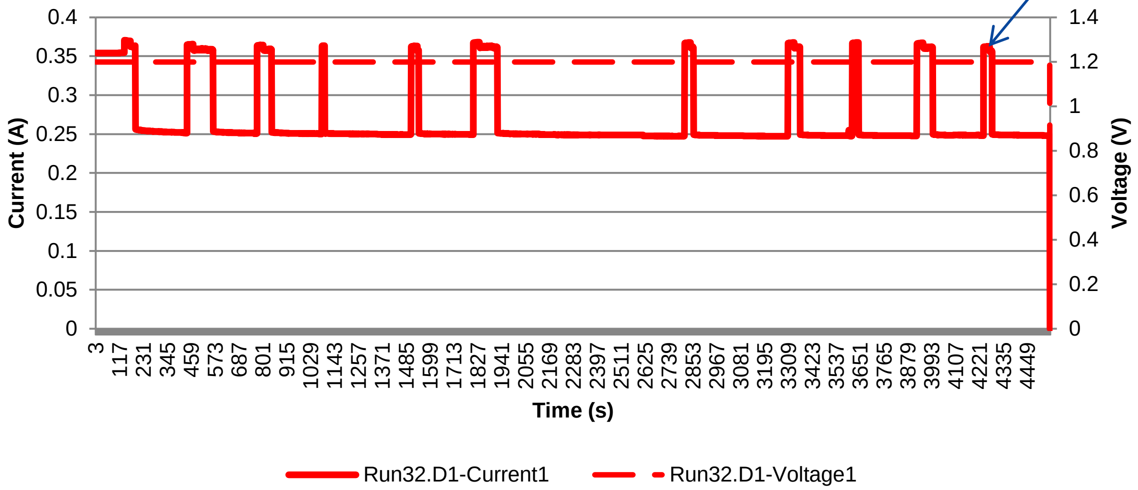
Run 27, Nominal, Tilt: 0 LET: 8.17, Fluence: 1.41E+06, Temperature: Room

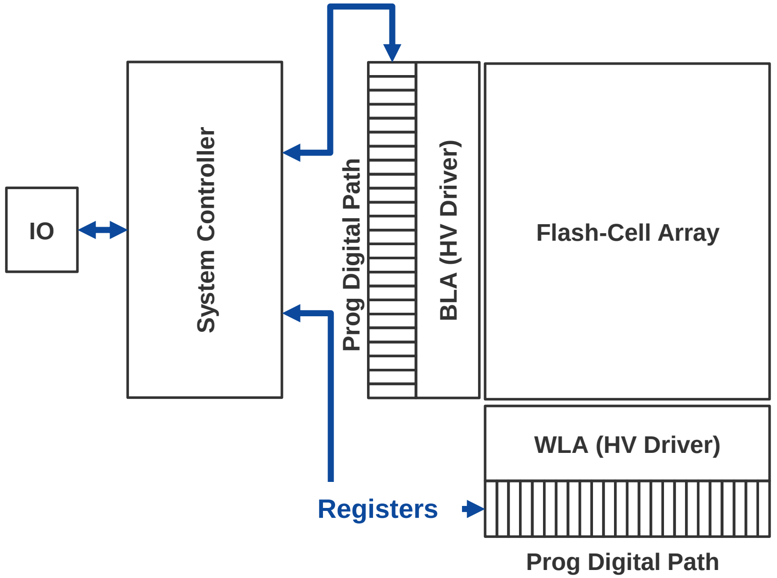


Programming one time

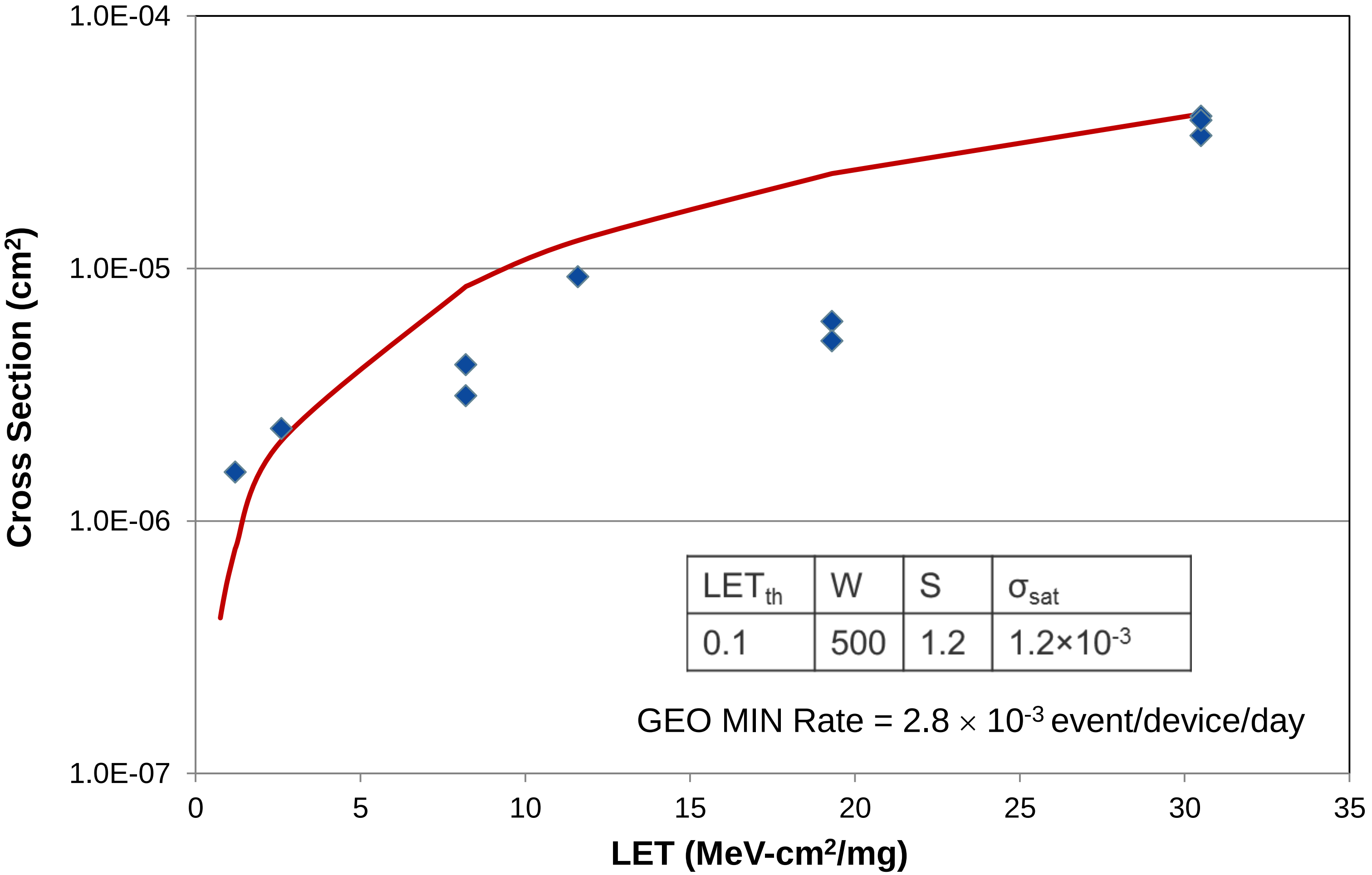
Programming in succession

Run 32, Nominal, Tilt: 0 LET: 30.5, Fluence: 1.00E+06, Temperature: Room





In-Beam Reprogramming Soft SEFI—Cross Section and Error Rate



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In-Flight Reprogramming Guidance

- Preliminary guidance
  - Highly unlikely that a destructive event will occur during programming in space
  - Probability of success for programming in GEO is estimated ~ 99% or higher
  - It is highly likely that in space, no ion will disrupt programming
  - If an ion strike does disrupt programming, it is highly likely that the next programming attempt will succeed
  - Reprogramming after TID
    - Reprogramming can be accomplished at TID levels up to 50Krad
    - Sufficient for 10 years of GEO and > 20 years of LEO

- Further tests are planned

- Solutions for reprogramming in-flight
  - Use Microsemi DirectC programming algorithm on processor—Available Today
  - Use Microsemi RTG4 programming controller—Coming Soon
  - See video presentation Remote Programming of RTG4 FPGAs on orbit in today's Space Forum event

Prompt-Dose/Dose-Rate Testing

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RTG4 Radiation Summary

Total Ionizing Dose	Stays within parametric limits > 125 Krad (Si)	
Single Event Latch-Up	No failure at facility limit of 103 MeV-cm^2/mg, 100°C	
Configuration Upset	No failure at facility limit of 103 MeV-cm^2/mg, 100°C	
Flip-Flop SEU	2.6E-12 errors/bit-day, GEO solar minimum, 1MHz	
LSRAM SEU	4.03E-8 errors/bit-day, GEO solar min (no EDAC)	1.1E-11 errors/bit-day, GEO solar min (with EDAC)
uSRAM SEU	3.33E-8 errors/bit-day, GEO solar min (no EDAC)	2.7E-13 errors/bit-day, GEO solar min (with EDAC)

- Test plan 2017 and Conference Papers and Publications
  - SET: Fabric, clocks, SpaceWire, MSIO, MSIOD
  - SEFI: PLL, SERDES, PCIe, DDR controllers, System Controller
  - Independent testing in progress (Aerospace Corp, NASA, JPL, ESA)
  - SEE Symposium and MAPLD Power Point presented in 5/2016 by Melanie Berg, NASA GSFC
  - 2016 HEART RTG4 Radiation Update
  - A Novel 65 nm Radiation Tolerant Flash Configuration Cell Used in RTG4 Field Programmable Gate Array
  - TID and SEE characterization of Microsemi's 4th generation radiation tolerant RTG4 flash-based FPGA
  - WP0191: Mitigation of Radiation Effects in RTG4 Radiation-Tolerant FPGAs
  - SEE Symposium /MAPLD May17 – "SEE Induced VT Shift in Flash Cells of Flash-Based FPGAs"
  - NSREC July 17 – "Investigation of TID and Dynamic Burn-In Induced VT Shift on RTG4 Flash-Based FPGA"

Thank You

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