Single Event Effects Hardening on 65 nm Flash-Based Field Programmable Gate Array

Jih-Jong Wang, Durwyn Dsilva, Nadia Rezzak, Sean Cui, Stephen Varela, Harvey Chen, Minh Nguyen, Ken O'Neill, Frank Hawley, John McCollum, and Esmat Hamdy

***Abstract*-- the single event effects hardening and heavy-ion testing of a radiation-hardened Flash-based field programmable gate array, RTG4, are presented. The hardened logic circuits include fabric flip-flops, fabric SRAM, global clocks, PLL, and SERDES. SEL is hardened for the whole chip. Lastly, the in-space programming is hardened as the consequence of the above hardening activities. Test results show the effects of hardenings.**

I. Introduction

This paper presents the single event effects (SEE) hardening and heavy-ion testing results of the radiation-hardened 65 nm Flash-based field programmable gate array (FPGA) RTG4.

The radiation-hardened by design (RHBD) techniques are applied both in the hardware and software: the fabric flip-flop (FF) is triple-module redundant (TMR) to reduce single event upset (SEU) and also has filtering function to reduce the soft errors caused by single event transients (SET); the fabric SRAM is protected by an error detection and correction (EDAC) technique of single error correction double error detection (SECDED) coding, also the minimum distance between separate bits in a word is maximized to avoid multiple bits upset in a word; the global clock distribution networks have hardened buffers, including a global buffer (GB) and row global buffers (RGB), which are sized up, low-pass filtered, and/or triplicated; the phase locked loop (PLL) is hardened to auto-recover the lock condition after an SET occurred; SERDES blocks, which are soft IPs, are hardened by design rules, glitch filters, and TMR; lastly single event latch-up (SEL) is hardened through layout-design rules and well-doping engineering.

SEE heavy-ion testing and results will be presented in the following sections. Every aforementioned hardening is scrutinized. In addition, an in-beam reprogramming experiment to simulate in-space reprogramming radiation effects and its results are also presented.

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J. Wang, N. Rezzak, S. Varela, H. Chen, M. Nguyen, K. O'Neill, F. Hawley, J. McCollum, and E. Hamdy are with the Microsemi-SoC, San Jose, CA95134, USA (telephone: 408-643-6302, e-mail: jih-jong.wang @microsemi.com).

D. Dsilva, was with the Microsemi-SoC. He is now with Susquehanna International Group, Bala Cynwyd, PA19004, USA (email: durwyn.dsilva@sig.com).

S. Cui, was with the Microsemi-SoC. He is now with the University of Toronto, Toronto, Canada (email: seancui94@gmail.com).

II. Heavy-Ion Experiments

Heavy-ion testing is performed in Cyclotron Facility at LBNL (Lawrence Berkeley National Laboratory), Berkeley, CA. and Cyclotron Institute at TAMU (Texas A&M University), College Station, TX. In LBNL, 16 MeV/n cocktails are used and 15 MeV/n beam is used in TAMU. Since the DUT, RT4G-150 is in a flip-chip package, its backside silicon is grinded down to be penetrated through by heavy-ions to reach the front-side circuits.

III. SEE Hardening and Heavy-Ion Testing Results on Fabric Components

This section will discuss the SEE hardening implemented in the fabric components including fabric FF, fabric clock distribution network, PLL, and fabric SRAMs.

A. Fabric Flip-Flop—*STMRFF*

As shown in Fig. 1, the fabric flip-flop is hardened by a SET-filter connected to the input and followed by triplicated control logics, flip-flops, and majority voters. It is officially named SET-filtered TMR Flip-Flop, acronym STMRFF.

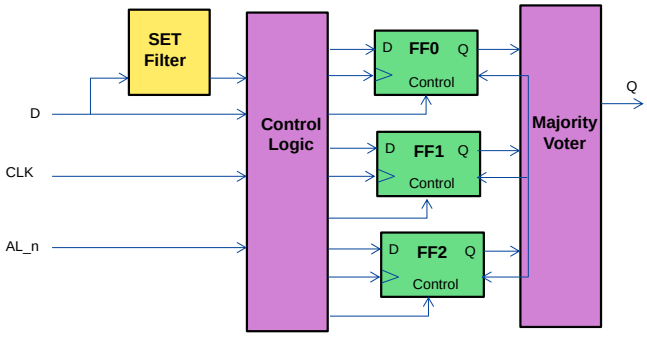


Fig. 1 Schematic shows an SET-filtered and TMR-hardened flip-flop.

The basic design for heavy-ion testing is a 1000-stage shift register. Totally there are 24 shift registers evenly distributed and controlled among 4 different clocks of 1, 50, 100, and 200 MHz respectively. These clocks are generated by the on-chip PLL with a 20 MHz reference clock coming from a separate controller chip.

Fig. 2a and 2b show the test results, for without and with SET filter respectively, plotted as upset cross-section versus linear energy transfer (LET). Non-observable upsets at 1 MHz indicate the TMR part of hardening is very effective

and also indicate the observed upsets for 50, 100, and 200 MHz are all due to SET. The origin can come from the local buffers and configuration switches.

For LET up to about 35 MeV-cm^2/mg, the upsets in the FF without filter are just over 2 times of upsets in the FF with 600ps-filter. Note that the upsets for either with or without filter at 65 MeV-cm^2/mg are very close. The reason is likely because the SET width is exceeding the 600ps. TCAD simulations done previously during the development stage of RTG4 support this statement.

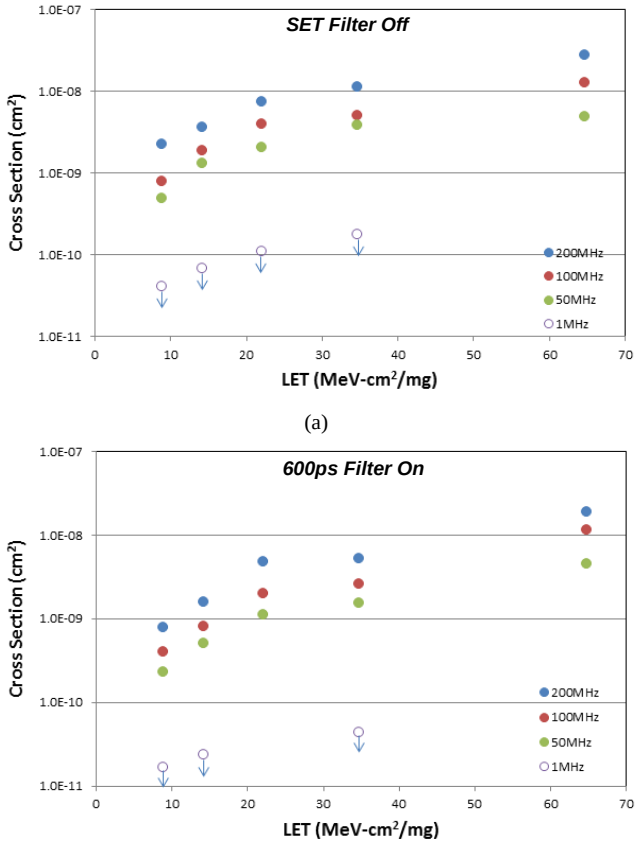


Fig. 2 STMRFF 1, 50, 100, and 200 MHz upset cross-section versus LET: (a) without SET filter; (b) with default 600ps filter.

B. Clock Distribution Network

The global buffers in the clock distribution network are hardened by various techniques; include sizing up transistors, inserting low-pass filters, and triplicating with analog voting.

For SEE testing, as shown in Fig. 3, the FPGA SEE-testing design at the layout level [1] has to be meticulously placed and routed manually so that all FFs in a shift register will be controlled by the same RGB. This action is to observe SETs in a RGB: when there is a burst-upset event in the shift register whose clock is controlled by this RGB, it counts as a RGB-upset event. Note that shift registers always use a checkerboard data pattern during the SEE testing. There is no need for similar FPGA design actions for testing SET in GB because GB controls all clocks in the chip; the event will be bursting upsets simultaneously happening in multiple shift registers.

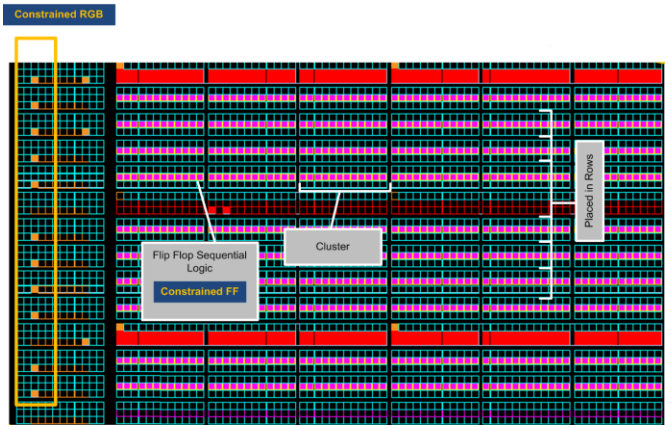


Fig. 3 Designer layout shows the place and route of FFs in a shift register to assure them controlled by the same RGB.

The test results are shown in Fig. 4: the SET cross-section versus heavy-ion LET is plotted. There is no observable SET in either GB or RGB for LET up to 30 MeV-cm^2/mg. The cross-section of each data point is the reciprocal of the total fluence of the ion-beam, which is specified by its LET.

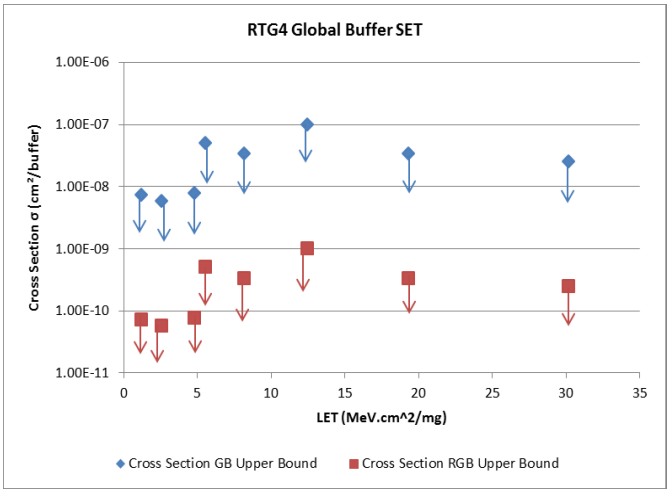


Fig. 4 Global buffer (GB) and row global buffer (RGB) upsets cross-section versus LET. No upset has been observed; data points indicate testing limits.

C. Phase Locked Loop (PLL)

The PLL lock mechanism is SEE-hardened so that PLL will self-recover after a functional interruptive SEE (SEFI) event. It is a hardened descendant of the PLL in SmartFusion2 (SF2) RTG4's commercial sibling. In SF2, the PLL can suffer lost-lock SEFI and need reset to recover [2].

The SEE testing design and heavy-ion beam testing are the same as that for fabric flip-flop. Fig. 5 shows the cross-section versus LET plot for transient lost-lock events. Only at the highest LET, 65 MeV-cm^2/mg, there is one PLL-unlock event needing reset to recover. Comparing to the unhardened SF2-PLL losing lock by event caused by low-LET ions, the hardening in RTG4-PLL is very effective.

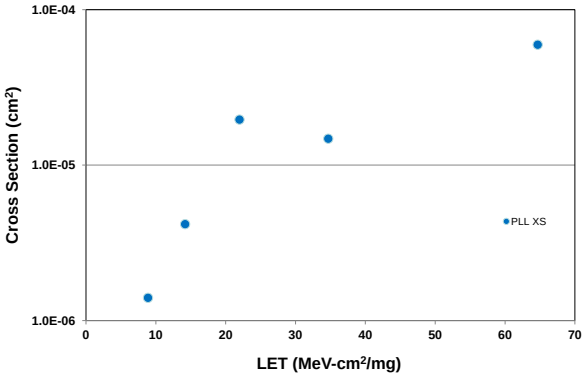


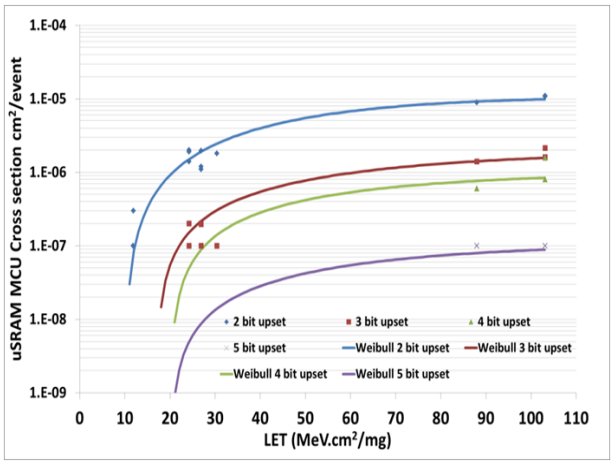
Fig. 5 PLL self-recovered SEFI cross-section versus LET. The SEFI event is defined by PLL lost lock.

D. LSRAM and µSRAM

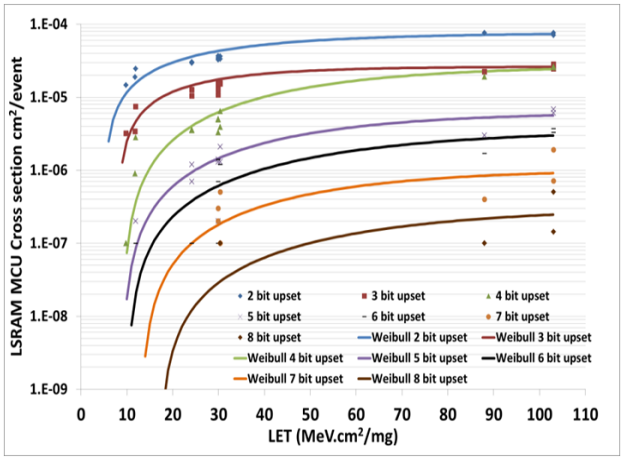
The SRAM in the FPGA fabric has two types: the µSRAM and LSRAM. The cell circuit, for either µSRAM or LSRAM, is the same for both RTG4 and SF2. However, RTG4's cells have more well-ties to harden SEL, and the bits separation in the same word is increased from 3-bit in SF2 to 9-bit in RTG4 for the SEU hardening. Since both products has the same EDAC scheme-SECDEC-to mitigate the soft error, the multiple cell upset for adjacent bits will determine the hardness. The bits in a word in RTG4 is separated wider to ensure the EDAC scheme is hardened even for very high LET.

The SEE testing to evaluate the EDAC has to be able to identify the physical location of every upset bit by a single ion strike. The location identification is done by user software; single-strike upsets in multiple bits can be identified by time-tag the upsets. Therefore a cluster of bits upsetting simultaneously by a single strike can be identified as a multiple cells upset (MCU) event. An MCU event is different from a multiple bits upset (MBU) event which is defined as a MCU event upsetting multiple bits in the same word. Since the bit to bit distance in a word is 9-bit, the possibility of an MBU event can be evaluated from the size of an MCU. Directly measuring errors in the EDAC-coded words by testing is problematic because the extremely high flux in the beam testing cannot mimic the very low-flux space environment.

Fig. 6a and 6b show plot MCU cross-section versus LET. beam-test data. With testing limit of 10^{-9} cm^2 for cross-section measurement, the largest MCU event can be detected in µSRAM is 5-bits MCU and in LSRAM is 8-bits. The size difference in these two SRAMs, LSRAM is about half of µSRAM, explains their different results.



(a)



(b)

Fig. 6 Cross-section versus LET: (a) MCU in µSRAM; (b) MCU in LSRAM. Note that the physical size of a µSRAM is larger than the size of a LSRAM.

IV. SEE Hardening on SERDES

Within the high-speed SERDES block, radiation hardening techniques are applied to the system controller, APB, REFCLK, SPLL-used with XAUI and PCIE blocks, path from REFCLKP to GLOBAL_0_OUT (fabric global clock), path from REFCLKN to GLOBAL_1_OUT. This is done with several types of mitigation techniques including TMR logic triplication and self-correcting latches as well as added digital delay buffers. The asynchronous resets are hardened using glitch-suppression filters and by using special buffers for reset distribution in all areas of the circuit.

The SEE testing design is illustrated in Fig. 7: the target is 4 parallel EPCS lanes. A loop-back design with pseudo-random-bit-string (PRBS) data is used to detect upsets. Note that the loop-back is within the DUT. The PRBS generator and checker are built from SEE hardened fabric logics to reduce their upsets contribution to negligible.

As shown in the figure, a controller in an external Master chip manages the testing system. The configuration register in PLL is SEE hardened but still has measurable upset. When its upset causes a functional failure in SERDES, the

controller will detect the event based on the looped back data. Then a command will be sent to on-chip CoreABC, built also from SEE hardened fabric logics, to refresh the configuration.

Fig. 8 shows the SEE testing results plotted as data points in cross-section versus LET. The soft errors, marked recoverable errors, are distributed like a typical Weibull curve. The configuration upset is very rare; they can always recover by the CoreABC refreshing action.

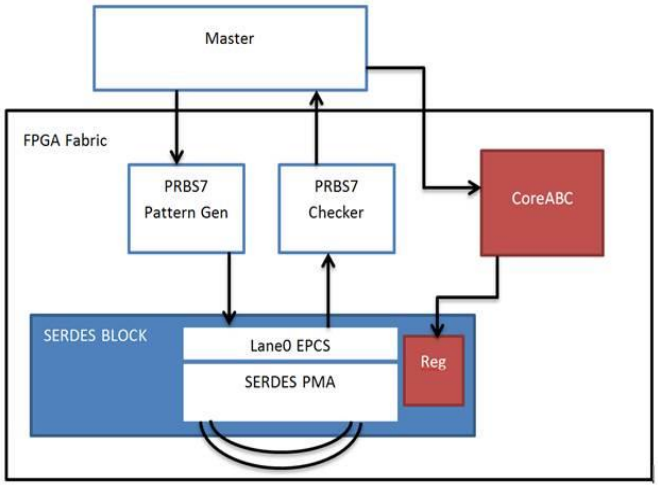


Fig. 7 Block diagram illustrates SERDES SEE testing design: 4 parallel EPECS lanes in a SERDES block configured as EPCS serial interface; each lane is running loop-back PRBS data for measuring soft errors.

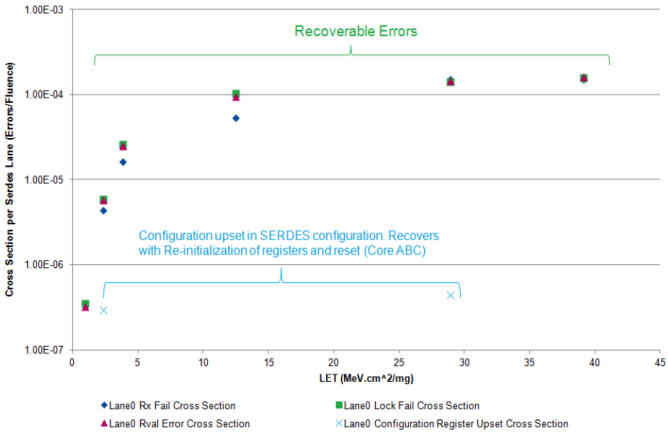


Fig. 8 Cross-section versus LET plot data points of soft errors and SEFIs.

V. SEL Hardening

The SEL hardening is implemented by design rules: the body ties have rules to ensure their high density; the input-output (IO), which performs at 2.5/3.3 VDC, has guard rings at the well boundaries. The fabrication process has been optimized to reduce the gain of the parasitic bipolar.

Test results on five RTG4 devices are listed in Table 1. It shows that at 100 C no SEL event occurs by irradiated with ions with effective LET of 10^3 MeV-cm^2/mg for fluence of 1.25×10^8 ions/cm^2.

Table 1

Temp	LET (MeV-cm^2/mg)	SEL Count	Fluence (ions/cm^2)
Room Temp	9.8	0	7.89×10^7
	13.74	0	1.10×10^8
	26.9	0	1.05×10^8
	31.06	0	5.00×10^7
	89	0	5.00×10^6
	103	0	2.60×10^7
100°C	58	0	4.00×10^7
	89	0	1.11×10^8
	103	0	1.25×10^8

VI. SEE Hardening on In-Space Programming

This section discusses RTG4 SEE issues related to in-space programming. The in-beam programming testing results shows that the in-space programming of RTG4 has very high SEE tolerance. The good result is probably a consequence of the hardening efforts toward the normal operations.

The Flash cells in RTG4 are hardened for both total ionizing dose (TID) and SEE [4]. As shown in Fig. 9, the C-Flash configuration cell is comprising of a pull-up P-Flash and pull-down N-Flash in a complementary structure. The PMOS in the middle functions as a resistor to mitigate a P-Flash reliability concern. Additionally, the high-voltage devices, in both programming and normal operational circuits, are also hardened.

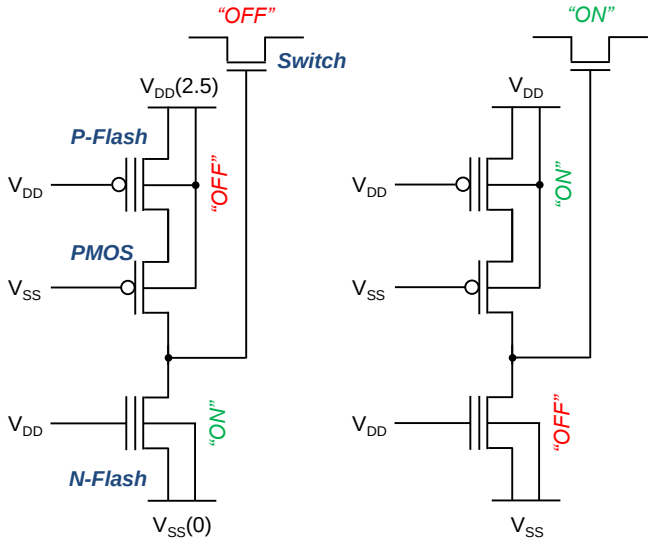


Fig. 9 Schematics illustrates the C-flash configuration cell in RTG4.

Fig. 10 depicts the timing diagram of the core power-supply current (I_{DD}) during an in-beam programming. When an SEE event stops the programming action, the current drop sharply for approximately 100 mA, this value is confirmed with SPICE simulation. The reprogram is always successive that is indicated by the sharply recovering of I_{DD}. This SEFI occurs for heavy-ions with LET as low as 1 MeV-cm^2/mg.

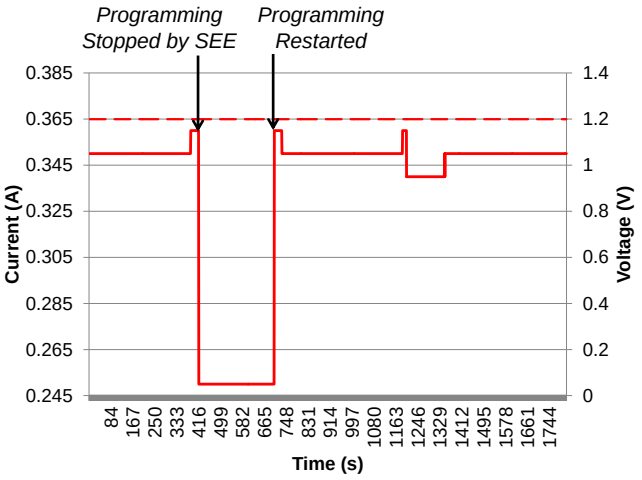


Fig. 10 In-beam program timing diagram for I_{DD} (solid line) and V_{DD} (dashed line): SEE interruption shows a sudden drop of I_{DD} by 100 mA; restart programming shows a jump of I_{DD} by 100 mA.

Preliminary two-photon absorption (TPA) laser scanning experiments indicate that the SEU in the registers of the digital path block of the programming circuits (Fig. 11) causes this SEFI. Only when the TPA laser spot is scanning on the programming digital path area, the SEFI with signature of I_{DD} drop occurs.

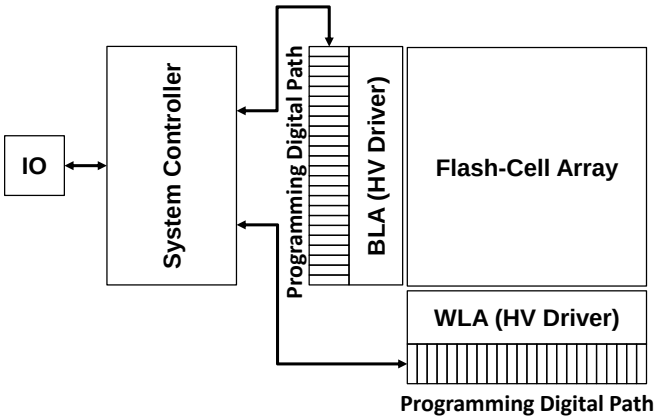


Fig. 11 Block diagram illustrates the relative layout locations of programming circuits and Flash cell arrays.

Multiple DUT have been tested to investigate this non-destructive SEFI event, and the resulted cross-section versus LET data is plotted in Fig. 12. Weibull parameters are extracted: onset LET = 0.1 MeV-cm^2/mg; width = 500 MeV-cm^2/mg; power = 1.2; plateau = 1.2×10^{-3} cm^2. CRÈME96 calculates the probability of failure for continuous programming in GEO MIN with 100 mil-Al shielding to be 6.7×10^{-4} event/device/day. In real application, the rate has to be scaled with the duty cycle which is 20 min for each programming. For example, if program the FPGA once a day, the rate equals 6.7×10^{-4} event/device/day times 20 min dividing by 1440 min and results 8.4×10^{-6} event/device/day.

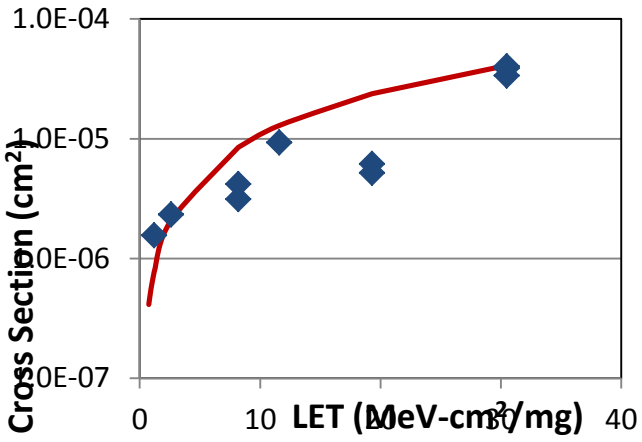


Fig. 12 In-beam reprogramming: cross section versus LET data points and four-parameter Weibull fitting curve (solid line).

VII. Conclusion

SEE hardenings are done in every functional block: fabric flip-flops are hardened by temporal filtering and TMR; clock networks hardened by sizing, LP filter and triplication; SRAM hardened by SECDED and bit separation; PLL hardened for Lock; SERDES hardened by design rules, glitch filters, sizing and TMR; chip SEL hardened by design rules and well doping. SEE testing results confirm efficacy of every hardening. Additionally, in-space programming hardened as the consequence of above hardening efforts.

References

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