Total Ionizing Dose (TID) Radiation Testing of the Microsemi LX7730 Telemetry Controller (100krad(Si) exposure)

Test information

Location: Defense Microelectronics Activity (DMEA) Science and Engineering Gamma Irradiation Test Facility in McClellan, California
Radiation Source: Co-60
Date: 5th june 2017
Lot #: Die1: T77090 - Die2: E33371
Date Code: 1710
Quantity tested: 4; Serial Numbers: 139, 141, 143 and 148
Test Method: MIL-STD-883J, Test Method 1019.9, Condition A (Dose rate 50rad(Si)/s)
Irradiation Temperature: Room
Irradiation Bias (VCC/VDD): Static at 15V/3.3V
Annealing: Biased - Room temperature for 168 hours
Pre and Post Test facility: Microsemi AMS - San Jose

Summary

The LX7730 performance after 100krad(Si) exposure is overall very stable and comparable to pre-radiation.
Similarly to previous lots, a few shifts that could push some parameters outside the pre-radiation specification were observed:

- Programmable current source
    - Full scale decreases by up to 5%
- Instrumentation amplifier
    - Offset variation of up to 6mV at gain=0.4, 3.0mV at gain=2 and 3.5mV at gain=10 were observed
    - At max VCC, offset variation of up to 4mV at gain=0.4 and 2mV at gain=2 and 3mV at gain=10 were observed
    - At min VCC, offset variation of up to 14mV at gain=0.4, 10mV at gain=2 and 4mV at gain=10 were observed
- Adjustable threshold Bi-level MUX and DAC
    - The threshold might shift by up to 50mV and the hysteresis might decrease by up to 55% when the comparator input is biased between 0 and 5V
    - The threshold might shift by up to 12% (0.6V) and the hysteresis might decrease by up to 60% when the comparator input is biased at a negative voltage
- Fixed Threshold Bi-Level Inputs
    - The threshold might shift by up to 40mV and the hysteresis is reduced by 20%
    - The propagation delays increase by up to 120%

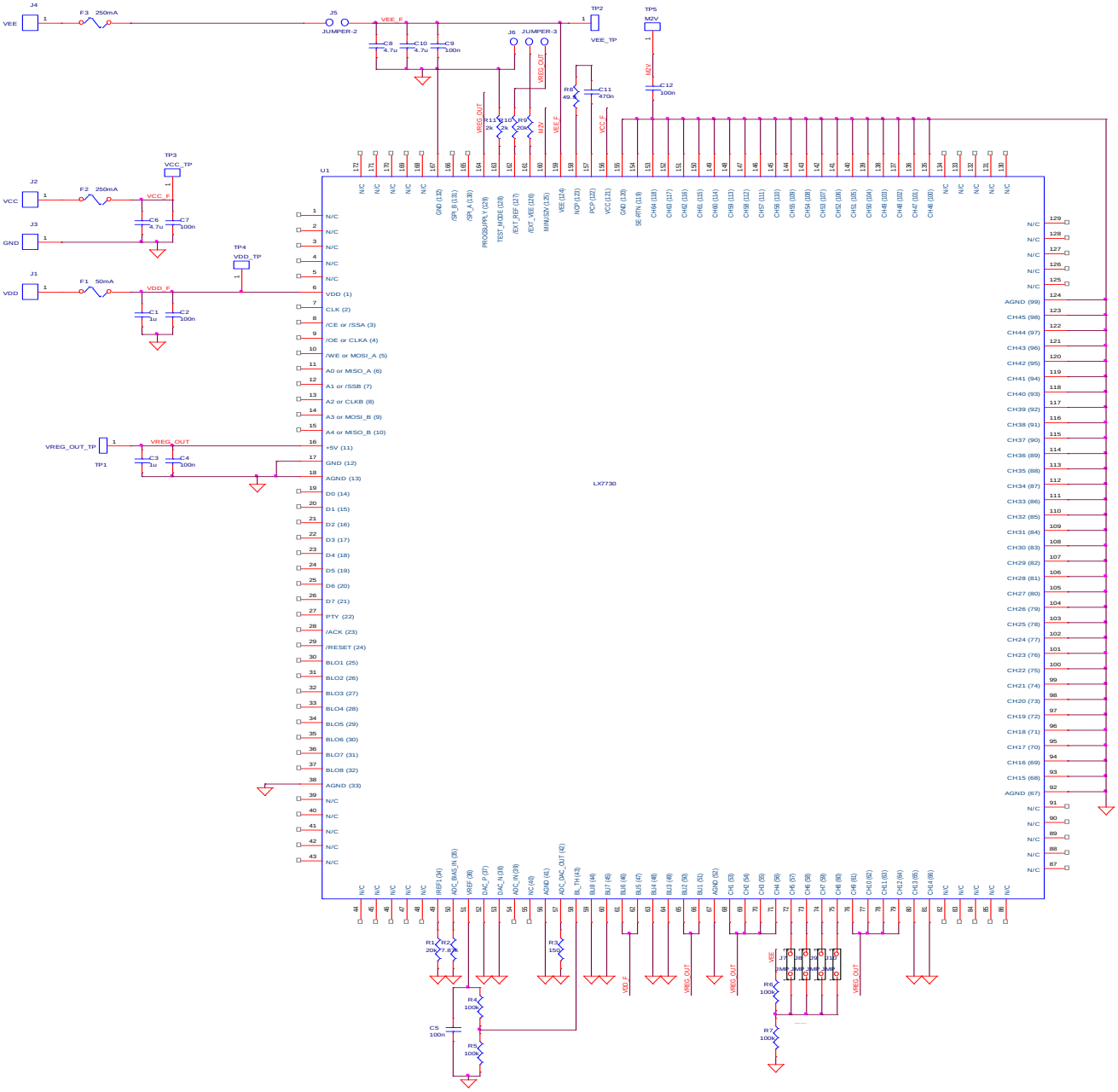
Conclusions

The test results indicate that after 100kRad exposure, the performance of the LX7730 is consistent with the pre-radiation results.

The few observed performance degradations can be mitigated at the system level as follows:

- Programmable current source full scale shift
    - Providing a method to calibrate the variation in programmable current using a precision current sense resistor on a dedicated calibration channel
- Instrumentation amplifier offset shift
    - The offset voltage can be assessed using a 100mV reference from a VREF voltage divider on a dedicated channel.
- Adjustable threshold Bi-level MUX and DAC shift
    - The threshold shift can be minimized by ensuring the comparator input is not biased with a negative voltage.

Bias circuit



Detailed Data

The pre Radiation specifications apply over the operating ambient temperature of -55C ≤ T_A ≤ 125C except where otherwise noted with the following test conditions: VCC = 15V, VDD = 3.3V; R_{IREF} = 20kΩ; $R_{ADC\_BIAS\_IN}$ = 7.87kΩ; $R_{ADC\_DAC\_OUT}$ = 158Ω; / EXT_VEE open, /EXT_REF open. CH1 and CH2 selected and CH2 grounded. CLK = 500kHz. Reg 7 =001010xx. Typical parameter refers to T_J = 25°C. Positive currents flow into the pin.

Pre and Post Irradiation measurements taken at 25C.

	Pre Radiation Specification				SN 565		SN 566		SN 568		SN 569		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Comment**
Operating Current													
VCC Normal Current	38	73	84	mA	67.926	65.915	67.369	65.094	67.718	65.83	66.774	64.915	Slight decrease
VCC Standby Current	2.0	4.0	7.0	mA	4.465	4.352	4.447	4.447	4.503	4.418	4.437	4.305	Slight increase
VEE Current	-6.0	-5.0	-2.5	mA	-5.308	-4.588	-5.039	-4.347	-5.172	-4.432	-5.155	-4.462	Slight decrease
Under Voltage Detection													
VCC UVLO	9.5	10	10.5	V	9.945	9.985	9.94	9.925	9.965	9.97	9.945	9.955	Very stable
VCC UVLO Hyst	150	200	400	mV	0.195	0.195	0.200	0.200	0.200	0.200	0.205	0.205	Very stable
VEE UVLO	-7.5	-8.00	-8.20	V	-8.05	-8.105	-8.07	-8.13	-8.005	-8.05	-8.07	-8.135	Very stable
VEE UVLO Hyst	150	200	400	mV	0.190	0.190	0.195	0.205	0.190	0.190	0.190	0.190	Very stable
+5V UVLO	3.9	4.15	4.40	V	4.125	4.125	4.115	4.105	4.155	4.15	4.145	4.15	Very stable
+5V UVLO Hyst	0	200	400	mV	0.195	0.200	0.200	0.200	0.200	0.200	0.190	0.190	Very stable
Internally Regulated Voltages and Currents													
VCC to VEE voltage drop	1.5	2.5	3.0	V	2.784	2.617	2.722	2.496	2.718	2.558	2.719	2.474	Slight decrease
+5V voltage	4.75	5.00	5.25	V	4.988	4.994	5.014	5.02	5	5.001	4.972	4.966	Very stable
VREF voltage	4.95	5.00	5.05	V	5.002	5.004	5.003	4.995	5.003	5.005	5.003	5.011	Very stable
IREF pin voltage	1.568	1.60	1.632	V	1.608	1.608	1.589	1.586	1.599	1.6	1.6	1.602	Very stable
Analog MUX													
Differential Range	0		5	V	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	
Common Mode Range	-5		5	V	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	
Voltage Clamp power applied	15	16	17	V	16.013	15.951	16.013	16.013	16.011	16.017	16.021	16.025	Very stable
	-23	-17	-15	V	-20.880	-21.048	-20.888	-21.050	-21.095	-21.257	-21.080	-21.219	Very stable
Voltage Clamp (VCC=VEE=0)	15	20	23	V	20.829	20.846	20.671	20.856	20.942	21.112	21.065	21.242	Very stable
	-23	-20	-15	V	-20.788	-20.944	-20.792	-20.965	-20.997	-21.166	-20.988	-21.131	Very stable
Settling Time			10	us	2.68	4.03	3.03	4.32	2.27	3.76	2.9	4.29	50% increase
Bias Current	-200	0	200	nA	-1.529	-1.161	-1.558	-0.746	-1.595	-1.19	-1.595	-1.171	Very stable
Leakage Current	-200	0	200	nA	0.614	1.85	-1.40	3.21	2.61	1.84	-0.472	4.296	Very stable
Programmable Current Source													
Full scale current	1.880	1.940	2.000	mA	1.932	1.877	1.922	1.862	1.938	1.886	1.906	1.853	~2.5-3.5% Decrease
Integral nonlinearity	-7.5	0	7.5	µA	2.462	1.046	2.754	1.117	3.178	1.275	3.477	2.031	Decrease
Differential nonlinearity	-5.0	0	5.0	µA	2.185	1.214	2.522	1.079	3.061	1.848	2.940	2.873	Decrease
Full scale current	3710	3840	3950	µA	3.809	3.716	3.782	3.686	3.796	3.713	3.752	3.669	~2-3% Decrease
Integral nonlinearity	-15		15	µA	9.362	5.664	9.991	7.373	9.991	5.586	12.217	8.823	Decrease
Differential nonlinearity	-15		15	µA	7.687	5.53	8.497	7.687	8.497	4.181	11.194	9.71	Decrease
At DAC=31	290	300	310	uA	299.838	286.999	301.632	286.527	303.142	288.981	302.009	288.226	~4-5% Decrease

	Pre Radiation Specification				SN 565		SN 566		SN 568		SN 569		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Comment**
Integral nonlinearity	-2.0		2.0	uA	0.634	1.177	1.271	0.389	0.805	1.191	0.635	1.061	Stable
Differential nonlinearity	-2.0		2.0	uA	0.999	0.737	0.868	0.664	1.294	1.215	0.442	0.792	Stable
Instrumentation Amplifier													
Offset Voltage, Gain = 0.4	-2		25	mV	15.95	21.41	6.91	9.53	8.29	13.02	15.21	18.55	Up to 6mV increase
Offset Voltage, Gain = 2	-3		3	mV	0.55	1.04	-0.38	-0.79	-0.29	2.73	0.07	-0.17	Up to 3mV change
Offset Voltage, Gain = 10	-3		3	mV	-1.08	-1.20	-0.73	-1.78	-0.03	3.37	-1.10	-1.63	Up to 3.5mV change
Gain Accuracy, Gain = 0.4	0.398	0.400	0.402	-	0.4000	0.3999	0.3997	0.3997	0.4002	0.4001	0.4001	0.4000	Very stable
Gain Accuracy, Gain = 2	1.992	2.000	2.004	-	1.997	1.997	1.997	1.997	1.998	1.998	1.997	1.997	Very stable
Gain Accuracy, Gain = 10	9.965	9.995	10.025	-	9.991	9.991	9.987	9.988	10.005	10.009	9.999	9.997	Very stable
400Hz 1st Pole Frequency	360	600	1000	Hz	675.933	679.839	679.839	684.375	688.281	691.558	675.933	675.933	Very stable
2kHz 1st Pole Frequency	1.4	2.8	3.8	kHz	2.469	2.484	2.492	2.492	2.523	2.523	2.477	2.477	Very stable
10kHz 1st Pole Frequency	8.8	13.5	18.2	kHz	10.812	10.812	10.812	10.812	10.852	10.852	10.812	10.812	Very stable
400Hz 2nd Pole Frequency	360	600	1000	Hz	679.839	684.375	684.375	688.281	695.464	700	679.839	679.839	Very stable
2kHz 2nd Pole Frequency	1.4	2.8	3.8	kHz	2.531	2.547	2.555	2.555	2.578	2.586	2.531	2.531	Very stable
10kHz 2nd Pole Frequency	8.8	13.5	18.2	kHz	11.047	11.047	11.047	11.047	11.086	11.086	11.086	11.047	Very stable
Output Step Rise Time, G=0.4	120	210	333	us	214.705	246.734	210.934	252.287	200.036	238.108	209.562	246.727	~15-20% Increase
Output Step Rise Time, G=2	31	52	87	us	48.366	53.102	47.71	53.711	45.719	51.255	47.548	53.038	~9-13% Increase
Output Step Rise Time, G=10	31	52	87	us	48.929	53.89	48.031	54.907	45.821	51.183	48.216	54.049	~10-14% Increase
Analog-to-Digital Converter (input at ADC_IN)													
Linear Range	0		2.0	V	Pass	Pass	Pass	Pass	Pass	Pass	Pass	Pass	
Full scale error	-2.5	0	2.5	%	-0.38	-0.29	-0.54	-0.42	-0.45	-0.39	-0.41	-0.38	Very stable
Offset Error	-10		10	mV	-3.99	-3.81	-6.36	-5.08	-4.02	-4.47	-6.02	-6.17	Very stable
Integral nonlinearity	-6		6	LSB	4.366	3.724	4.618	3.252	5.040	3.366	3.554	3.236	Very stable
Differential nonlinearity	-1		3	LSB	2.104	1.789	2.007	1.890	1.948	1.861	1.558	1.601	Very stable
Leakage current	-0.2	0	0.2	uA	0.009	-0.018	-0. 018	-0.009	-0.009	0.009	0.000	0.000	Very stable
Adjustable threshold Bi-level MUX and DAC													
Threshold DAC Max Output (If input is >=0V during TID)	4.95	5	5.05	V	4.985	5.021	4.975	5.003	4.975	5.012	4.965	5.015	Up to 50mV increase
Hysteresis DAC Max Output (If input is >=0V during TID)	0.075	0.112	0.150	V	0.130	0.060	0.125	0.054	0.115	0.063	0.120	0.063	Up to 55% decrease
Threshold DAC Max Output (If input is VEE/2 during TID)	4.95	5	5.05	V	4.995	4.423	4.965	4.387	4.985	4.393	4.965	4.381	~12% decrease
Hysteresis DAC Max Output (If input is VEE/2 during TID)	0.075	0.112	0.150	V	0.120	0.051	0.120	0.054	0.110	0.054	0.110	0.054	Up to 60% decrease
10 Bit Current DAC													
Full Scale	-2.06	-2.00	-1.94	mA	-2.009	-2.042	-1.986	-2.017	-1.986	-2.026	-2.008	-2.043	Very stable
Integral nonlinearity	-5		5	LSB	-1.461	-2.028	-1.302	-1.440	-2.521	-2.070	-0.474	-1.115	Very stable
					1.225	1.116	0.782	0.911	1.279	1.150	0.534	0.796	Very stable
Differential nonlinearity	-0.5		0.5	LSB	-0.309	-0.305	-0.316	-0.314	-0.293	-0.294	-0.320	-0.323	Very stable
					0.070	0.057	0.073	0.067	0.093	0.060	0.064	0.054	Very stable
DAC Settling Time			1	us	0.604	0.573	0.625	0.597	0.622	0.590	0.609	0.574	Very stable
Fixed Threshold Bi-Level Inputs													

	Pre Radiation Specification				SN 565		SN 566		SN 568		SN 569		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Comment**
Threshold – Internal ref (Rising Voltage)	2.45	2.50	2.55	V	2.495	2.534	2.484	2.522	2.515	2.548	2.498	2.541	Up to 40mV increase
Threshold Hysteresis – Internal reference	60	120	180	mV	0.136	0.105	0.134	0.101	0.128	0.101	0.112	0.087	Up to 20% decrease
Threshold – External 2.5V (Rising Voltage)	2.45	2.50	2.55	V	2.505	2.540	2.495	2.540	2.515	2.550	2.510	2.550	Up to 40mV increase
Threshold Hysteresis – External 2.5V	60	120	180	mV	0.140	0.105	0.130	0.105	0.125	0.105	0.115	0.090	Up to 20% decrease
Voltage Clamp (power applied) – 1mA into the pin	15	20	23	V	20.673	20.824	20.668	20.820	20.835	20.952	20.865	20.986	Very stable
Voltage Clamp (power applied) – 1mA out of the pin	-23	-20	-15	V	-20.602	-20.737	-20.598	-20.730	-20.897	-21.046	-20.909	-21.027	Very stable
Voltage Clamp (power remove) – 1mA into the pin	15	20	23	V	20.581	20.745	20.568	20.739	20.707	20.863	20.775	20.901	Very stable
Voltage Clamp (power removed) – 1mA out of the pin	-23	-20	-15	V	-20.507	-20.645	-20.506	-20.651	-20.762	-20.875	-20.816	-20.948	Very stable
Bias Current at 5V	-0.2	0	1.5	uA	0.115	0.128	0.102	0.108	0.161	0.171	0.178	0.194	Very stable
Bias Current at 0V	-0.2	0	1.5	uA	0.000	0.000	-0.001	0.000	0.000	0.000	0.000	0.000	Very stable
Leakage Current at 5V (power off)	-0.2	0	1.5	uA	0.109	0.119	0.095	0.102	0.152	0.159	0.168	0.186	Very stable
Leakage Current at 0V (power off)	-0.2	0	1.5	uA	0.000	0.000	0.000	0.000	0.000	0.000	0.000	0.000	Very stable
Propagation Delay - High to Low transition	0.3	0.8	1.3	us	0.743	1.390	0.855	1.817	0.712	1.378	0.851	1.680	~90-120% increase
Propagation Delay - Low to High transition	0.8	2.1	3.4	us	2.023	3.778	1.889	3.506	2.288	4.219	2.302	4.241	~60-90% increase
Threshold Pin Leakage at 5V	-0.2	0	2.0	uA	0.277	0.279	0.252	0.252	0.32	0.318	0.32	0.311	Very stable
Threshold Pin Leakage at 0V	-0.2	0	2.0	uA	0.001	0.017	0.014	0.019	0.007	0.022	0.007	0.017	Very stable
Logic Levels for FPGA Interface I/Os													
Input Logic Threshold at 3.3V	1.155	1.65	2.145	V	1.715	1.685	1.715	1.695	1.725	1.715	1.705	1.675	Very stable
Program pins Threshold	2.0	2.5	3.0	V	2.540	2.530	2.550	2.540	2.560	2.550	2.510	2.490	Very stable
Logic Output VOH at 4mA at 3.3V	3.0		3.3	V	3.172	3.167	3.172	3.168	3.172	3.169	3.172	3.166	Very stable
Logic Output VOL at 4mA at 3.3V	0		0.3	V	0.104	0.103	0.102	0.103	0.102	0.102	0.102	0.102	Very stable
IIH SPI_A, SPI_B (3.3V)	-2	0	2	uA	-0.001	0.023	0.01	0.029	0.053	0.075	0.017	0.029	Very stable
IIL SPI_A, SPI_B (0V)	-10	-4	-1.5	uA	-4.99	-5.02	-4.93	-4.93	-5.08	-5.06	-5.08	-5.06	Very stable
IIH Pins 2,6,8-10,14-21, 22: I/O as input (3.3V)	1.5	4	10	uA	5.19	5.16	5.07	5.06	5.2	5.14	5.22	5.15	Very stable
IIL Pins 2,6,8-10,14-21, 22: I/O as input (0V)	-2	0	2	uA	0.016	-0.002	0.012	-0.005	0.006	0.002	0.015	0.002	Very stable
IIH Pins 3-5, 7 I/O as input (3.3V)	-2	0	2	uA	0.012	0.004	0.018	0.007	0.017	0.011	0.016	0.011	Very stable
IIL Pins 3-5, 7: I/O as input (0V)	-10	-4	-1.5	uA	-5.03	-5.03	-4.95	-4.96	-5.05	-5.03	-5.07	-5.06	Very stable
IIH /EXT_VREF or /EXT_VEE = 5V	-2	0	2	uA	0.076	0.047	0.052	0.039	1.125	1.102	0.255	0.251	Very stable

	Pre Radiation Specification				SN 565		SN 566		SN 568		SN 569		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Pre**	**Post 100k**	**Comment**
IIL /EXT_VREF or /EXT_VEE = 0V	-12	-6	-1.5	uA	-7.68	-7.78	-7.58	-7.64	-7.84	-7.88	-7.68	-7.67	Very stable
IIH /RESET (5V)	1.5	4	10	uA	5.09	5.52	5	5.43	5.18	5.58	5.17	5.55	Very stable
IIL /RESET (0V)	-150	-66	-33	uA	-97	-97.4	-96.2	-96.3	-98	-97.8	-97.8	-97.5	Very stable

Parameters tested but not specified

	Pre Radiation Test Limits				SN 021		SN 070		SN 149		SN276		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Comment**
Instrumentation Amplifier													
Offset Voltage, Gain = 0.4 16V/3.3V	-2		32	mV	15.57	19.27	6.49	7.92	7.89	11.34	15.02	17.09	Up to 4mV increase
Offset Voltage, Gain = 0.4 11.4V/3.3V	-2		32	mV	15.79	26.47	5.93	14.45	8.44	23.43	15.59	24.80	Up to 15mV increase
Offset Voltage, Gain = 2 16V/3.3V	-3.5		4.5	mV	0.16	-0.13	-0.20	-2.19	-0.49	1.28	-0.15	-1.32	Up to 2mV change
Offset Voltage, Gain = 2 11.4V/3.3V	-3.5		4.5	mV	0.64	6.50	-0.76	4.45	0.30	13.99	0.81	6.62	Up to 14mV change
Offset Voltage, Gain = 10 16V/3.3V	-3.5		3.5	mV	-1.10	-2.00	-0.59	-2.63	-0.14	2.31	-1.21	-2.27	Up to 3mV change
Offset Voltage, Gain = 10 11.4V/3.3V	-3.5		3.5	mV	-1.52	1.29	-1.67	0.33	-0.23	9.65	-1.19	2.13	Up to 10mV change
Gain Accuracy, Gain = 0.4 15V/3.3V at CM=5V	0.398		0.402	-	0.3992	0.3991	0.3989	0.3989	0.3994	0.3993	0.3993	0.3992	Very stable
Gain Accuracy, Gain = 0.4 15V/3.3V at CM=-5V	0.398		0.402	-	0.3993	0.3992	0.3991	0.3990	0.3996	0.3995	0.3995	0.3994	Very stable
Gain Accuracy, Gain = 0.4 11.4V/3.3V at CM=5V	0.397		0.403	-	0.3998	0.4001	0.3995	0.3997	0.4000	0.4002	0.3999	0.4001	Very stable
Gain Accuracy, Gain = 0.4 11.4V/3.3V at CM=0V	0.398		0.402	-	0.4008	0.4009	0.4005	0.4006	0.4010	0.4011	0.4009	0.4010	Very stable
Gain Accuracy, Gain = 0.4 11.4V/3.3V at CM=-5V	0.397		0.403	-	0.3999	0.4001	0.3996	0.3998	0.4001	0.4003	0.4001	0.4002	Very stable
Gain Accuracy, Gain = 0.4 16V/3.3V at CM=5V	0.398		0.402	-	0.3991	0.3990	0.3989	0.3988	0.3993	0.3992	0.3992	0.3991	Very stable
Gain Accuracy, Gain = 0.4 16V/3.3V at CM=0V	0.398		0.402	-	0.3999	0.3998	0.3997	0.3996	0.4002	0.4001	0.4001	0.4000	Very stable
Gain Accuracy, Gain = 0.4 16V/3.3V at CM=-5V	0.398		0.402	-	0.3992	0.3992	0.3990	0.3989	0.3995	0.3994	0.3994	0.3993	Very stable
Gain Accuracy, Gain = 2 15V/3.3V at CM=5V	1.992		2.004	-	1.996	1.996	1.995	1.995	1.997	1.997	1.996	1.995	Very stable
Gain Accuracy, Gain = 2 15V/3.3V at CM=-5V	1.992		2.004	-	1.996	1.996	1.996	1.995	1.997	1.997	1.996	1.995	Very stable
Gain Accuracy, Gain = 2 11.4V/3.3V at CM=5V	1.990		2.010	-	1.996	1.996	1.995	1.995	1.997	1.996	1.996	1.995	Very stable
Gain Accuracy, Gain = 2 11.4V/3.3V at CM=0V	1.992		2.004	-	1.997	1.997	1.997	1.996	1.998	1.998	1.997	1.997	Very stable
Gain Accuracy, Gain = 2 11.4V/3.3V at CM=-5V	1.990		2.010	-	1.996	1.996	1.995	1.995	1.997	1.996	1.996	1.995	Very stable

	Pre Radiation Test Limits				SN 021		SN 070		SN 149		SN276		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Comment**
Gain Accuracy, Gain = 2 16V/3.3V at CM=5V	1.992		2.004	-	1.996	1.996	1.995	1.995	1.997	1.996	1.996	1.995	Very stable
Gain Accuracy, Gain = 2 16V/3.3V at CM=0V	1.992		2.004	-	1.997	1.997	1.997	1.997	1.998	1.998	1.997	1.997	Very stable
Gain Accuracy, Gain = 2 16V/3.3V at CM=-5V	1.992		2.004	-	1.996	1.996	1.996	1.995	1.997	1.997	1.996	1.996	Very stable
Gain Accuracy, Gain = 10 15V/3.3V at CM=5V	9.965		10.025	-	9.985	9.986	9.979	9.982	9.997	10	9.991	9.991	Very stable
Gain Accuracy, Gain = 10 15V/3.3V at CM=-5V	9.965		10.025	-	9.985	9.986	9.98	9.982	9.998	10	9.991	9.989	Very stable
Gain Accuracy, Gain = 10 11.4V/3.3V at CM=5V	9.965		10.025	-	9.985	9.988	9.979	9.984	9.998	10.002	9.992	9.99	Very stable
Gain Accuracy, Gain = 10 11.4V/3.3V at CM=0V	9.965		10.025	-	9.991	9.995	9.987	9.99	10.005	10.012	9.999	9.998	Very stable
Gain Accuracy, Gain = 10 11.4V/3.3V at CM=-5V	9.965		10.025	-	9.984	9.996	9.979	9.988	9.996	10.01	9.99	10.005	Very stable
Gain Accuracy, Gain = 10 16V/3.3V at CM=5V	9.965		10.025	-	9.984	9.986	9.98	9.983	9.998	10	9.991	9.993	Very stable
Gain Accuracy, Gain = 10 16V/3.3V at CM=0V	9.965		10.025	-	9.99	9.995	9.987	9.99	10.005	10.008	9.998	9.997	Very stable
Gain Accuracy, Gain = 10 16V/3.3V at CM=-5V	9.965		10.025	-	9.985	9.988	9.98	9.984	9.997	10	9.99	9.989	Very stable
Logic Levels for FPGA Interface I/Os													
Input Logic Threshold at VDD=2.25V	0.7875	1.125	1.463	V	1.213	1.193	1.213	1.203	1.223	1.223	1.203	1.193	Very stable
Input Logic Threshold at VDD=5.5V	1.925	2.725	3.575	V	2.785	2.765	2.795	2.775	2.805	2.795	2.775	2.735	Very stable
Logic Output VOH at 4mA at VDD=2.25V	1.95		2.25	V	2.102	2.093	2.105	2.097	2.103	2.095	2.103	2.094	Very stable
Logic Output VOL at 4mA at VDD=2.25V	0		0.3	V	0.118	0.118	0.115	0.116	0.117	0.116	0.116	0.116	Very stable
Logic Output VOH at 4mA at VDD=5.5V	5.2		5.5	V	5.383	5.382	5.383	5.383	5.384	5.385	5.384	5.380	Very stable
Logic Output VOL at 4mA at VDD=5.5V	0		0.3	V	0.094	0.094	0.093	0.093	0.092	0.092	0.092	0.093	Very stable
Programmable Current Source													
Full scale current (doubWt OFF) at VCC=11.4V	1.880	1.940	2.000	mA	1.931	1.877	1.922	1.862	1.937	1.886	1.906	1.854	~2-3% Decrease
Integral nonlinearity at VCC=11.4V	-7.5	0	7.5	µA	2.580	1.054	2.801	1.054	3.210	1.330	3.500	2.133	Decrease
Differential nonlinearity at VCC=11.4V	-5.0	0	5.0	µA	2.239	1.214	2.495	1.038	3.102	1.861	2.900	2.900	Decrease
Full scale current (doubWt ON) at VCC=11.4V	3710	3840	3950	µA	3.808	3.712	3.780	3.687	3.795	3.707	3.750	3.663	~2-3% Decrease
Integral nonlinearity at VCC=11.4V	-15		15	µA	9.205	8.600	10.070	7.088	9.677	9.384	12.194	12.509	Stable
Differential nonlinearity at VCC=11.4V	-15		15	µA	7.822	7.016	9.171	7.224	8.227	9.137	11.464	13.082	Stable
At DAC=31 at VCC=11.4V	290	300	310	uA	299.838	286.527	301.537	285.866	303.237	288.415	302.009	288.037	~4-5% Decrease

	Pre Radiation Test Limits				SN 021		SN 070		SN 149		SN276		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Comment**
Integral nonlinearity at VCC=11.4V	-2.0		2.0	uA	0.591	1.244	1.239	0.371	0.751	1.321	0.628	1.147	Slight Increase
Differential nonlinearity at VCC=11.4V	-2.0		2.0	uA	0.999	0.758	0.959	0.643	1.203	1.197	0.442	0.807	Stable
Full scale current (doubWt OFF) at VCC=16V	1.880	1.940	2.000	mA	1.933	1.879	1.923	1.864	1.939	1.888	1.907	1.856	~2-3% Decrease
Integral nonlinearity at VCC=16V	-7.5	0	7.5	µA	2.494	0.952	2.754	0.944	3.155	1.180	3.442	2.121	Decrease
Differential nonlinearity at VCC=16V	-5.0	0	5.0	µA	2.239	1.065	2.509	0.904	3.075	1.834	2.900	2.913	Decrease
Full scale current (doubWt ON) at VCC=16V	3710	3840	3950	µA	3.815	3.724	3.787	3.691	3.801	3.721	3.756	3.677	~2-3% Decrease
Integral nonlinearity at VCC=16V	-15		15	µA	8.890	5.507	9.598	7.676	9.834	6.024	12.307	9.081	Decrease
Differential nonlinearity at VCC=16V	-15		15	µA	7.957	5.799	9.171	7.822	8.092	4.316	11.599	9.576	Decrease
At DAC=31 at VCC=16V	290	300	310	uA	300.027	286.621	301.726	286.054	303.331	288.415	302.104	288.226	~4-5% Decrease
Integral nonlinearity at VCC=16V	-2.0		2.0	uA	0.610	1.283	1.224	0.439	0.764	1.347	0.653	1.165	Slight Increase
Differential nonlinearity at VCC=16V	-2.0		2.0	uA	1.008	0.764	0.874	0.557	1.209	1.200	0.435	0.816	Stable
Fixed Threshold Bi-Level Inputs													
Threshold – External 0.1V (Rising Voltage) at VCC=15V	0.0	0.1	0.2	V	0.105	0.135	0.095	0.135	0.115	0.150	0.110	0.145	Up to 40mV
Threshold Hysteresis – External 0.1V at VCC=15V	0.06	0.12	0.18	V	0.135	0.105	0.130	0.105	0.125	0.105	0.110	0.090	Up to 25mV decrease
Threshold – External 4.9V (Rising Voltage) at VCC=15V	4.8	4.9	5.0	V	4.910	4.940	4.900	4.940	4.925	4.955	4.915	4.950	Up to 40mV
Threshold Hysteresis – External 4.9V at VCC=15V	0.06	0.12	0.18	V	0.140	0.105	0.135	0.105	0.130	0.105	0.115	0.090	Up to 35mV decrease
Threshold – Internal ref (Rising Voltage) at VCC=11.4V	2.45	2.50	2.55	V	2.495	2.534	2.484	2.522	2.515	2.548	2.498	2.541	Up to 40mV
Threshold Hysteresis – Internal reference at VCC=11.4V	0.06	0.12	0.18	V	0.138	0.107	0.136	0.103	0.130	0.103	0.116	0.089	Up to 33mV decrease
Threshold – External 4.9V (Rising Voltage) at VCC=11.4V	4.8	4.9	5.0	V	4.910	4.945	4.900	4.940	4.925	4.955	4.915	4.950	Up to 40mV
Threshold Hysteresis – External 4.9V at VCC=11.4V	0.06	0.12	0.18	V	0.145	0.115	0.135	0.105	0.135	0.105	0.120	0.090	Up to 30mV decrease
Adjustable threshold Bi-level MUX and DAC													
Threshold DAC Max Output (If input is >=0V during TID) at VCC=11.4V	4.95	5	5.05	V	4.985	5.018	4.965	5.003	4.975	5.012	4.965	5.012	Up to 40mV increase
Hysteresis DAC Max Output (If input is >=0V during TID) at VCC=11.4V	0.075	0.112	0.150	V	0.130	0.060	0.120	0.057	0.115	0.066	0.120	0.063	Up to 65mV decrease
Threshold DAC Max Output (If input is VEE/2 during TID)	4.95	5	5.05	V	4.995	4.423	4.965	4.387	4.985	4.393	4.965	4.381	~12% decrease

	Pre Radiation Test Limits				SN 021		SN 070		SN 149		SN276		
Parameters	**Min**	**Typ**	**Max**	**Units**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Pre**	**100kR Post**	**Comment**
at VCC=11.4V													
Hysteresis DAC Max Output (If input is VEE/2 during TID) at VCC=11.4V	0.075	0.112	0.150	V	0.125	0.054	0.120	0.054	0.110	0.054	0.115	0.054	Up to 60% decrease
Threshold DAC=0 Output (If input is >=0V during TID) at VCC=15V	-0.05	0	0.05	V	0.015	0.048	0.005	0.042	0.025	0.048	0.005	0.045	Up to 40mV increase
Hysteresis DAC=0 Output (If input is >=0V during TID) at VCC=15V	0.075	0.112	0.150	V	0.130	0.060	0.125	0.057	0.120	0.066	0.120	0.063	Up to 60% decrease
Threshold DAC=0 Output (If input is VEE/2 during TID) at VCC=15V	-0.05	0	0.05	V	0.025	-0.550	0.005	-0.577	0.025	-0.565	0.005	-0.589	~0.58V decrease
Hysteresis DAC=0 Output (If input is VEE/2 during TID) at VCC=15V	0.075	0.112	0.150	V	0.125	0.051	0.125	0.054	0.110	0.057	0.115	0.054	Up to 60% decrease
Threshold DAC=0 Output (If input is >=0V during TID) at VCC=11.4V	-0.05	0	0.05	V	0.005	0.045	0.005	0.039	0.025	0.051	0.005	0.042	Up to 30% decrease
Hysteresis DAC=0 Output (If input is >=0V during TID) at VCC=11.4V	0.075	0.112	0.150	V	0.120	0.057	0.125	0.057	0.125	0.063	0.120	0.063	Up to 50mV increase
Threshold DAC=0 Output (If input is VEE/2 during TID) at VCC=11.4V	-0.05	0	0.05	V	0.025	-0.550	0.005	-0.577	0.025	-0.565	0.005	-0.589	Up to 25% decrease
Hysteresis DAC=0 Output (If input is VEE/2 during TID) at VCC=11.4V	0.075	0.112	0.150	V	0.125	0.051	0.130	0.054	0.110	0.057	0.115	0.054	~0.5V decrease