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Post-Integration Reprogramming of RTG4 FPGAs Using DirectC and RISC-V

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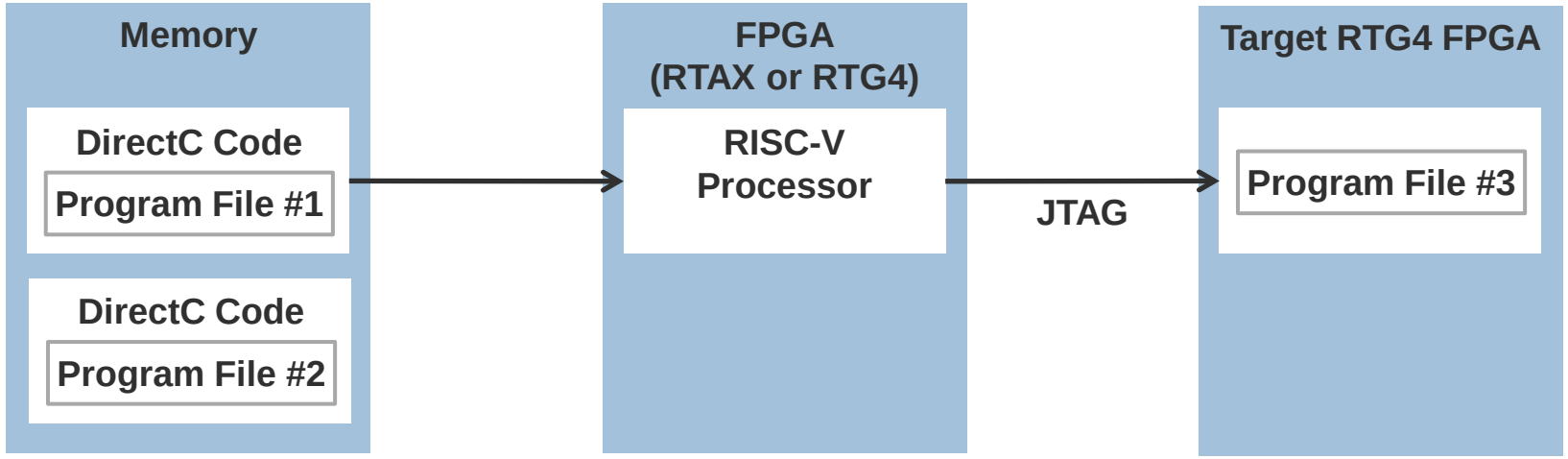
Introduction: Why Reprogram after Integration?

- Multiple reasons why it may be necessary to reprogram after integration
  - Post-launch bug fix
  - Processing algo enhancement/fine tuning after satellite deployment
  - Adapt flight hardware to previously unknown target/mission/item of interest
  - Repurposing of functioning flight hardware after mission completion

- RTG4 supports reprogramming after integration, during space flight
  - Constraints to be aware of:
    - Exceeding 200 programming cycles will result in reduced program retention time
    - Reprogramming circuits become inoperative after greater than 50 krad of total dose
    - Heavy ion radiation can cause non-destructive interruptions to programming (less than 1% probability in GEO)

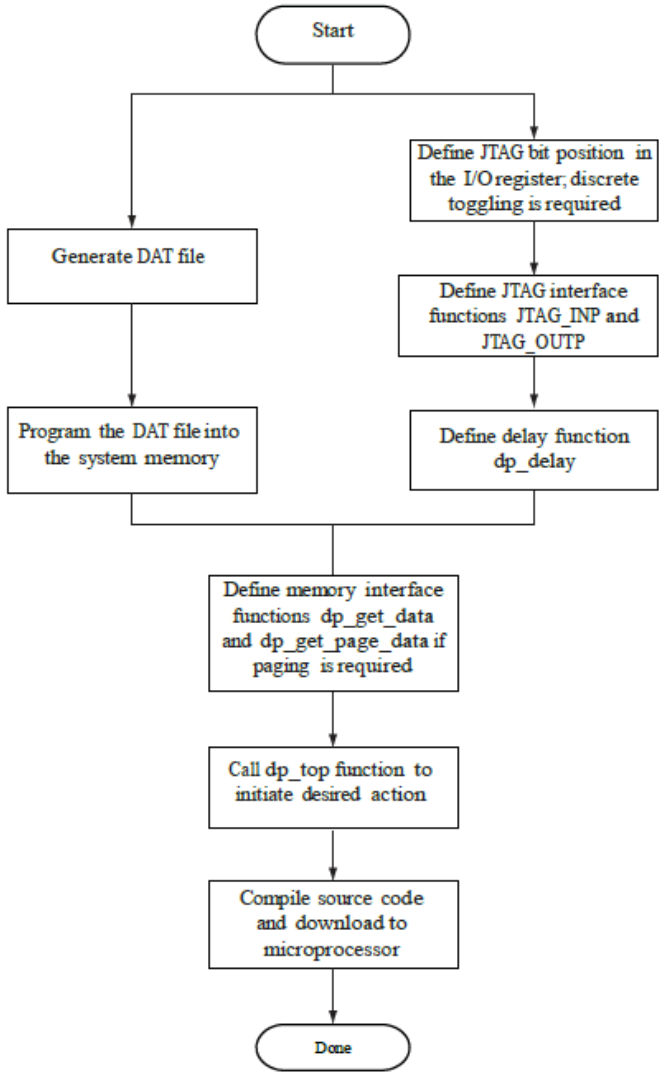
How to Accomplish Reprogramming

- A controller is required to retrieve the new programming code from memory and to upload the new code into the target RTG4 FPGA
- This requires a microprocessor . . .
  - Can use a discrete, standalone radiation-tolerant microprocessor
  - Can use a soft-IP microprocessor in another FPGA
  - In our example, we use a RISC-V processor running on another RTG4 FPGA
- . . . and also requires instruction code for the processor to execute
  - In our example, we use Microsemi DirectC embedded in-system programming code



Overview of In-System Programming with DirectC

- DirectC is a set of 'C' source code files that support embedded in-system programming for a variety of Microsemi FPGAs, including RTG4
  - Must be modified to meet needs of each specific implementation and compiled with an API
- Target FPGA design must be compiled and stored as *.dat* file
  - Microsemi Libero software is used to create the *.dat* file
  - RTG4 *.dat* files are on the order of 50 Mbits
- RTG4 requires programming through the JTAG interface
  - RTG4 requires activation of the JTAG interface in order to disable system controller suspend mode
- Refer to the Microsemi DirectC User Guide for details https://www.microsemi.com/products/fpga-soc/design-resources/programming/directc#documents



RISC-V Microprocessor Overview

- A new free and open ISA developed at UC Berkeley, initiated in 2010 through a permissible BSD license
- RISC-V is not an open-source processor, but open-source implementations will exist
- ISA designed for
  - Simplicity
  - Longevity (freeze base instructions, your code runs forever)
  - Innovation (plenty of opcode space for custom instructions)
- RISC-V Foundation
  - To direct future development, to foster adoption, and to protect the ISA

Example RISC-V Implementation in RTG4

- Flexible, open ISA permits many variations of features and performance
- Open ISA permits inspectable RTL source code
- On-shore US-based RTL developers support RISC-V on RTG4
- Initial RISC-V implementation in RTG4
  - Occupies less than 10% of available resources
  - Operates at up to 70 MHz over mil temp range

Core	TCM	LE's	Pipe	DMIPs	Cache	Mul/Div	SPFP	DPFP	Available
RV32IM	No	12K	5	1.1	Yes	Yes	No	No	Now
Others	TBD								

Reprogramming Reference Design

- Reference design for RTG4 reprogramming using two RTG4 Dev Kits
  - RTG4 Dev Kit #1 runs a design with embedded RISC-V with DirectC code
  - RTG4 Dev Kit #2 hosts the RTG4 being reprogrammed
  - Obtain reference design Libero project from Microsemi
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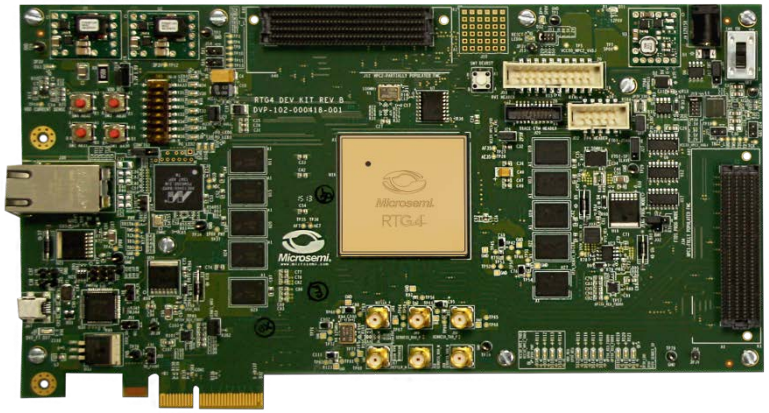
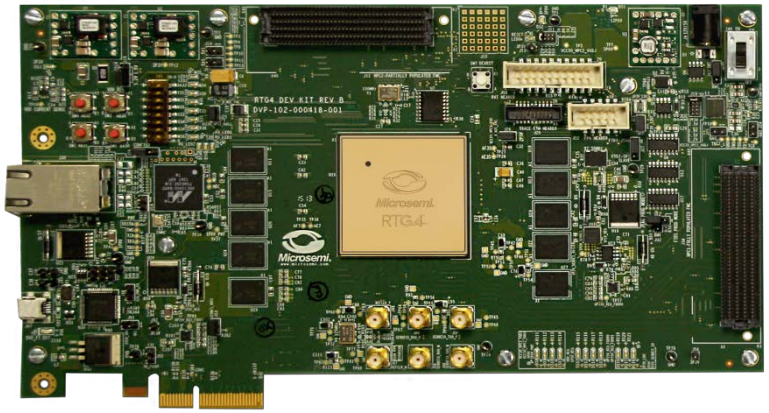


RTG4 Dev Kit #1 hosts RTG4 with embedded RISC-V processor IP, running DirectC

Reprogramming



RTG4 Dev Kit #2 hosts RTG4 to be reprogrammed by RTG4 Dev Kit #2

Thank You

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