ER0207
Errata
PolarFire FPGA - ES Devices

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document.

2 Errata for PolarFire Engineering Samples

2.1 Introduction

PolarFire™ FPGA engineering samples are subject to the limitations described in this errata. This document contains updated information about any known engineering samples specific issues and provides the available limitations and workarounds. Engineering sample issues identified in this errata will be corrected in subsequent revisions of the devices listed in the following table. Contact Microsemi Technical Support for more information.

2.2 Sample Revisions

The following table describes the sample revisions released. Errata items impact all -ES revisions listed unless specified.

Table 1 • **Sample Revisions Released per Device**

Devices	Packages	Revisions
MPF300T	FCG1152 and FCG484	0, 01

Table 2 • **PolarFire Engineering Sample Operating Conditions**

Operation Temperature Range	Program/Erase	Retention Lifetime	sNVM Endurance	FPGA Endurance
20 °C - 50 °C[1]	20 °C - 50 °C	1 year	1000 cycles	200 cycles

1. T_J = Junction temperature.

2.3 PCB Designs

For information about how to determine proper signal pinout, see *UG0726: PolarFire FPGA Board Design User Guide*. The proper signal pinout is required for all clocking, transceiver, and FPGA pin recommendations.

3 Summary of Device Errata

The following table lists the summary of device errata.

Table 3 • **Summary of PolarFire Devices Errata**

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Table 3 • **Summary of PolarFire Devices Errata *(continued)***

Errata Number	Description
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4 Descriptions and Workarounds

Power supply sequencing

Workaround

Engineering sample must follow this power-on sequence:

1. V_{DD} to V_{DD} operational minimum
2. V_{DD25} to V_{DD25} operational minimum
3. V_{DDI} and V_{DDAUX} must be powered up any time before V_{DD18} or simultaneously with V_{DD18} if supplied from same power source.
4. Last supply is V_{DD18} (V_{PP}) and followed by other supplies

See the *DS0141: PolarFire FPGA Datasheet* for information about the operational minimum voltages. The V_{DD25} power-supply can draw large currents at power-up or power cycling if this sequence is not followed.

Observe the specified power supply ramp rates specified in the *DS0141: PolarFire FPGA Datasheet*.

Bank3 V_{DDI} and $V_{DD\_XCVR\_CLK}$ and XCVR_VREF[1:2]

Bank 3 V_{DDI} and $V_{DD\_XCVR\_CLK}$ and XCVR_VREF[1:2] cannot exceed 2.5 V nominal.

Hot-swapping/cold sparing is not supported on any I/Os powered by V_{DDI3} 0or the transceiver reference clock input pins

Includes the following I/O pins:

- SDO
- SDI
- FF_EXIT_N
- IO_CFG_INTFK
- SPI_EN
- SCK
- DEVRST_N
- SS
- TCK
- TMS
- TDI
- TDO
- TRSTB
- XCVR_#A_REFCLK_P/N
- XCVR_#B_REFCLK_P/N
- XCVR_#C_REFCLK_P/N

Workaround

None

Some I/O pins do not support hot-swapping/cold sparing on erased devices

The following table describes the 35 GPIO pins that do not support hot-swapping/cold sparing on erased devices. Programmed devices do not have this errata.

Table 4 • **Unsupported GPIO Pins on Erased Devices[1], [2]**

Bank	GPIO Pins
0	HSIO169PB0, HSIO170PB0, HSIO171PB0, HSIO173NB0
1	HSIO72NB1, HSIO73PB1, HSIO74PB1, HSIO75PB1, HSIO79PB1, HSIO80PB1, HSIO81PB1
2	GPIO244NB2, GPIO246PB2, GPIO247PB2, GPIO248PB2, GPIO26PB2, GPIO27PB2, GPIO28PB2, GPIO32PB2, GPIO33PB2, GPIO34PB2, GPIO35NB2
4	GPIO174PB4, GPIO180PB4, GPIO181PB4
5	GPIO238PB5, GPIO239PB5, GPIO241PB5
6	HSIO62PB6, HSIO63PB6, HSIO64PB6, HSIO68PB6, HSIO69PB6, HSIO70PB6, HSIO71NB6

1. Applicable only on erased parts. Programmed parts do not have the errata.
2. If these pins are used as input or bi-directional buffers, an erased device will actively drive these outputs rather than being properly disabled.

Workaround

Do not use these pins if required for hot-swapping/cold sparing applications, if part is not programmed.

Calibration of FPGA I/O buffers only available at power-up

The FPGA I/O buffers have calibration circuitry to optimize and match the I/O impedance and termination within a system. The calibration occurs every time the device is powered up. After the device power-up, recalibration is not available on command.

Workaround

To recalibrate, the device requires a power-cycle to correctly recalibrate.

SmartDebug active probe speed

The live probe output cannot toggle faster than 100 MHz.

Workaround

None.

Missing global clock connection in XCVR Quad1

Designs cannot utilize two global clocks for XCVR Quad1. Designs have access to only one global clock on Quad1.

Workaround

In the Libero® SoC PolarFire Transceiver Lane Configurator, the user can select the clock resources used for transmit and receive and Global or Regional clocks. For lanes assigned to Quad1, only a single Global connection is available. This implies that only one lane in that Quad and one direction of that lane can select Global in this interface.

Inefficient usage of Asynchronous dual-port LSRAM blocks

For LSRAM blocks configured as Asynchronous dual-ports when Port A is greater than x20, twice the number of required LSRAM blocks are used.

Workaround

Two 1Kx20 LSRAM blocks are automatically instantiated by Libero SoC PolarFire to implement the single 512 × 40 LSRAM.

GPIO IOCDR SGMII

This limitation prohibits IOD CDR interfaces to be used with a >0 ppm offset. For SGMII, the PHY device and PolarFire IOD CDR must use the same reference clock.

SGMII interfaces using transceivers are not affected with this limitation.

Workaround

SGMII can be implemented with IOCDR using 0 ppm or a common clock using the same clock configuration for both TX and RX clocks.

SmartDebug active probe write

SmartDebug Active Probe write operation is not available. Active Probe read operation is operational as documented.

Workaround

None

PCIe core is not correctly initialized

PCIe is not correctly initialized after programming the device.

Workaround

Device must be power-cycled after programming if PCIe Core is used in the design.

The PCIe AXI slave interface has lower than expected throughput

Workaround

None

HSIO and GPIO drive strength may deviate by ± 20% from datasheet specifications

Workaround

None

PCIe fails to enter into transmit compliance when used with a 50 Ω load

Workaround

None

Voltage reference sensitivity issue with HSIOs when V_{DD18} and V_{DD25} supply voltage rail separation is too large

This effects the HSIO buffer banks only. This issue is managed by reducing the separation between V_{DD25} and V_{DD18}. For example, when V_{DD25} is maximum then V_{DD18} needs to be maximum or when V_{DD25} is typical then V_{DD18} needs to be typical. Respectively, if V_{DD18} and V_{DD25} are minimum and the other maximum will influence the effectiveness of the voltage references of the HSIO banks causing I/O buffers from correctly functioning.

LVDS VOS output common mode specification can vary as much as 175 mV below the datasheet specification

V_{DD} power may be 40% higher than reported by Power Estimator

The PolarFire Power Estimator v3e is currently optimistic with regard to the estimated V_{DD} static power. It is expected that designs can have 40% higher current on the V_{DD} power supply compared to the provided estimation.

Transaction layer clock behavior of PCI express block

To allow initialization of the PCIe block, PCIE_TL_CLK_125 MHz must be available immediately after the device power-up. The TL_CLK_125 MHz must be sourced from the DIV/2 OSC160 at power-up and switched to the TxPLL DIV_CLK while operating the PCIe. If not sourced, PCIe bridge registers and XCVR registers will not be initialized. For example implementation, see the PolarFire PCIe demo design https://www.microsemi.com/products/fpga-soc/fpga/polarfire-fpga#overview.

The CCC-PLL Lock output can glitch after reset has occurred using the DEVRSTN pin

The PLL lock output may glitch when a device reset has occurred via the DEVRSTN pin.

Workaround

This glitch can be mitigated by extending the PLL LOCKCNT parameter.

PLL_CTRL2 bits[12:9] register

See *UG0684 PolarFire FPGA Clocking Resources User Guide* for information about CCC register access.

LSRAM Read before Write (RBW) mode

In RBW mode, the old read data is presented until the write is completed then will change to the newly written data on the next cycle. This LSRAM mode is not available.

Workaround

None

Re-programming failure using FlashPro (JTAG programming)

Designs that are deployed device initialization to µPROM or external SPI before programming will fail reprogramming.

FlashPro Error Message:

Error: programmer 'S201Z7FK2R': Executing action PROGRAM FAILED, EXIT -38

Workaround

Error condition can be cleared by re-attempting programming. This issues is only identified in MPF300-ES Rev0 devices.

GPIO On-die termination

The on-die pull-up of the thevenin termination can be as high as 2x. This causes a weak ODT termination.

Workaround

User can select a stronger termination value for the design.

Transceiver Polarity Inversion

There is no programmable receiver polarity inversion possible on the transceivers for 8B10B, 64B6xB, and PMA.

Work around

None

5 Unsupported Features

System controller suspend mode

Flash*Freeze mode

Temperature voltage sensor (TVS)

Device zeroization

Generic I/O gearing modes

PCIe Gen 2 electrical compliance

Automated DFE, contact factory for DFE support

XCVR limitations, contact factory for solutions outside defined support

ACJTAG IEEE 1149.6 for transceiver pins

6 Engineering Sample Device Identification

PolarFire FPGA engineering sample can be identified from the Temperature Grade field in the lower left hand corner as shown in the following figure.

Figure 1 • **ES Identification Markings**