

UG0763
User Guide
MIPI CSI-2 Receiver Decoder



Power Matters.™

Microsemi Corporate Headquarters

One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113

Outside the USA: +1 (949) 380-6100

Fax: +1 (949) 215-4996

Email: sales.support@microsemi.com

www.microsemi.com

© 2017 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.

About Microsemi

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for aerospace & defense, communications, data center and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; enterprise storage and communication solutions, security technologies and scalable anti-tamper products; Ethernet solutions; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, California, and has approximately 4,800 employees globally. Learn more at www.microsemi.com.

Contents

1	Revision History	1
1.1	Revision 1.0	1
2	Introduction	2
3	Hardware Implementation	3
3.1	Design Description	3
3.1.1	Lane Management Multiplexer	3
3.1.2	Packet Decoder	4
3.2	Inputs and Outputs	5
3.3	Configuration Parameters	6
3.4	Timing Diagrams	6
3.4.1	Long Packet	6
3.4.2	Short Packet	6
3.5	Resource Utilization	7

Figures

Figure 1	Video Data Stream	2
Figure 2	Architecture of MIPI CSI-2 Core	3
Figure 3	Implementation of Lane Merger	3
Figure 4	FSM Implementation of Decoder	4
Figure 5	Timing Waveform of Long Packet	6
Figure 6	Timing Waveform of Frame Start Packet	6

Tables

Table 1	Supported Data Types	4
Table 2	Input and Output Ports of the MIPI CSI-2 Receiver Decoder	5
Table 3	Configuration Parameters	6
Table 4	Resource Utilization of the MIPI CSI-2 Receiver Decoder	7

1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document.

2 Introduction

MIPI CSI-2 is a standard specification by Mobile Industry Processor Interface (MIPI) Alliance. The Camera Serial Interface 2 (CSI-2) specification defines an interface between a peripheral device (camera) and a host processor (baseband, application engine). This user guide describes the MIPI CSI-2 Receiver Decoder (MIPI CSI-2 RxDecoder), which decodes the data from the sensor interface. The IP Core supports multi-lane (1, 2, and 4 lanes) and RAW8 data type. MIPI CSI-2 operates in two modes—high-speed mode and low-power mode. Currently, SmartFusion2 supports high-speed mode only as the I/O does not have analog front end circuitry. For more information, see [AC460: Building MIPI CSI-2 Applications using SmartFusion2 and IGLOO2 FPGAs Application Note](#). In high-speed mode, MIPI CSI-2 supports the transport of image data using Short Packet and Long Packet formats. Short packets provides frame synchronization and line synchronization information. Long packet provides the pixel information. The sequence of transmitted packets is:

1. Frame start (short packet)
2. Line Start (optional)
3. Few image data packets (long packets)
4. Line End (optional)
5. Frame End (short packet)

One long packet is equivalent to one image data line. The following illustration shows the video data stream.

Figure 1 • Video Data Stream



Note:

FS: Frame Start Packet (short packet)

Image: Pixel data of image embedded in Long Packet

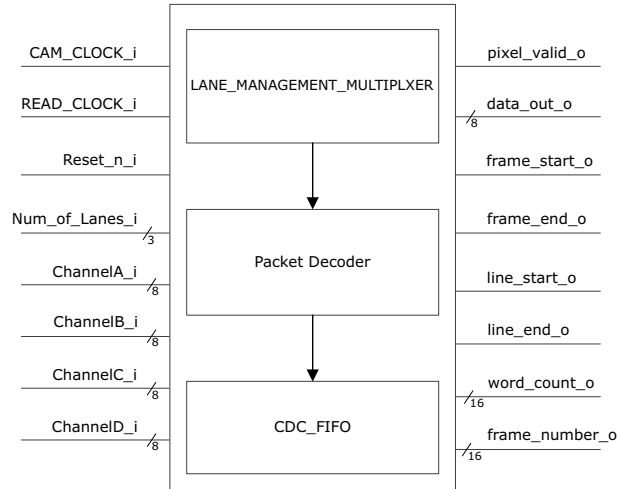
FE: Frame End Packet (short packet)

3 Hardware Implementation

This section describes the implementation details of the theta generation.

The following illustration shows the architecture of MIPI CSI-2 Core.

Figure 2 • Architecture of MIPI CSI-2 Core

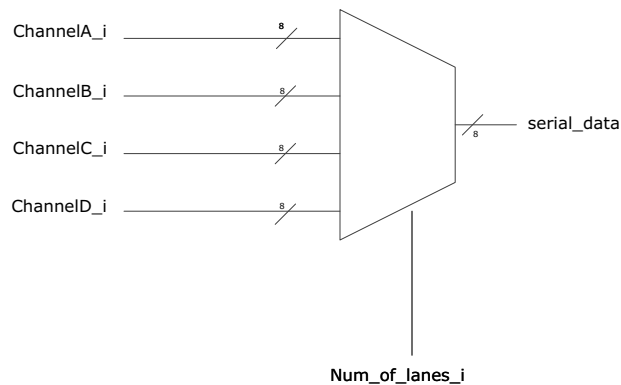


3.1 Design Description

3.1.1 Lane Management Multiplexer

The following illustration describes the implementation of lane merger.

Figure 3 • Implementation of Lane Merger



If the number of lanes is configured as one, then the incoming data is sent as it is over the `serial_data` signal. If the number of lanes is configured as two, the data from `ChannelA_i` and `ChannelB_i` are consolidated and received over the `serial_data` signal. If the number of lanes is configured as four lanes, the data from `ChannelA_i`, `ChannelB_i`, `ChannelC_i`, and `ChannelD_i` inputs are consolidated and received over the `serial_data` signal.

3.1.2 Packet Decoder

It decodes the incoming short packets and long packets and then consequently generates the `frame_start_o`, `frame_end_o`, `line_start_o`, `line_end_o`, `word_count_o`, `pixel_valid_o`, and `data_out_o`. Pixel data arrives between line start and line end signals. Short packet contains only packet header and supports various data types. Microsemi MIPI CSI-2 Receiver IP Core supports the following data types for short packets:

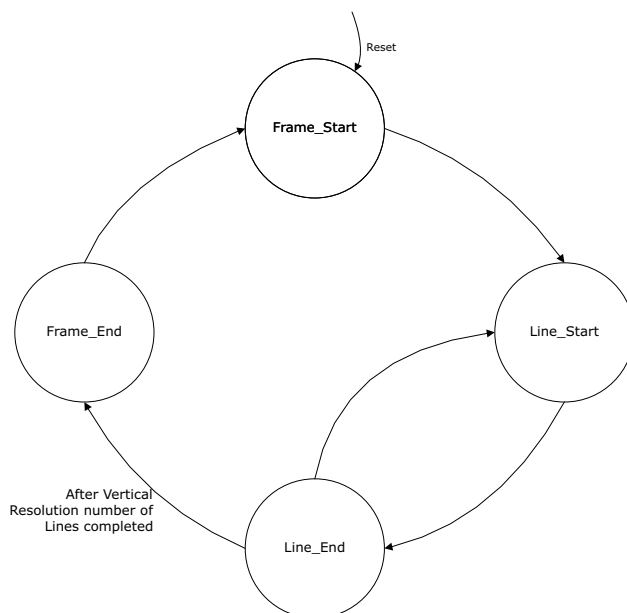
Table 1 • Supported Data Types

Data Type	Description
0x00	Frame start
0x01	Frame end

Long packet contains the image data. The length of the packet is determined by the horizontal resolution that the camera sensor is configured to. This can be seen at the `word_count_o` output signal.

The following illustration shows the FSM implementation of decoder.

Figure 4 • FSM Implementation of Decoder



1. Frame Start: On receiving the frame start packet, generate the frame start pulse and then wait for line start.
2. Line Start: On receiving the line start indication, generate the line start pulse.
3. Line End: On generating the line start pulse, store the pixel data, and then generate the line end pulse. Repeat Step 2 and 3 until the frame end packet is received.
4. Frame End: On receiving the frame end packet, generate the frame end pulse. Repeat the above steps for all frames.

The `CAM_CLOCK_I` must be configured to the image sensor frequency to process the incoming data regardless of `Num_of_lanes_i` configured to one lane, two lanes, or four lanes. `READ_CLOCK_I` must be equal or greater than `CAM_CLOCK_I`.

Currently Microsemi supports only RAW8 data type. For RAW8 data type, one pixel per clock is received on `data_out_o[7:0]`. To validate the image data, `pixel_valid_o` output signal is sent. Whenever it is asserted high, output pixel data is valid.

3.2 Inputs and Outputs

The following table lists the input and output ports of the theta generation configuration parameters

Table 2 • Input and Output Ports of the MIPI CSI-2 Receiver Decoder

Signal Name	Direction	Width	Description
CAM_CLOCK_I	Input		Image sensor clock
READ_CLOCK_I	Input		Read clock. Must be equal or greater than CAM_CLOCK_I.
RESET_N_I	Input		Asynchronous active low reset signal.
Number_of_Lanes_i	Input	3 bits	Number of data lanes configured. Supports only 1, 2, or 4 data lanes. 3'b001: One Lane 3'b010: Two Lanes 3'b100: Four Lanes
ChannelA_i	Input	[g_DATAWIDTH - 1:0]	Input data from lane one.
ChannelB_i	Input	[g_DATAWIDTH - 1:0]	Input data from lane two.
ChannelC_i	Input	[g_DATAWIDTH - 1:0]	Input data from lane three.
ChannelD_i	Input	[g_DATAWIDTH - 1:0]	Input data from lane four.
data_out_o	Output	[g_DATAWIDTH - 1:0]	Pixel data output. It is valid only when <code>pixel_valid_o</code> is asserted high.
pixel_valid_o	Output		Data valid output. Asserted high when <code>data_out_o</code> is valid.
word_count_o	Output	16 bits	Represents horizontal resolution in hex format.
frame_start_o	Output		Asserted high when frame start is detected in the incoming packets.
frame_end_o	Output		Asserted high when frame end is detected in the incoming packets.
line_start_o	Output		Asserted high when line start is detected in the incoming packets.
line_end_o	Output		Asserted high when line end is detected in the incoming packets.
frame_number_o	Output	16 bits	Frame number in hex format.

3.3 Configuration Parameters

The following table lists the description of the configuration parameters used in the hardware implementation of MIPI CSI-2 RxDecoder block. They are the generic parameters and can vary based on the application requirements.

Table 3 • Configuration Parameters

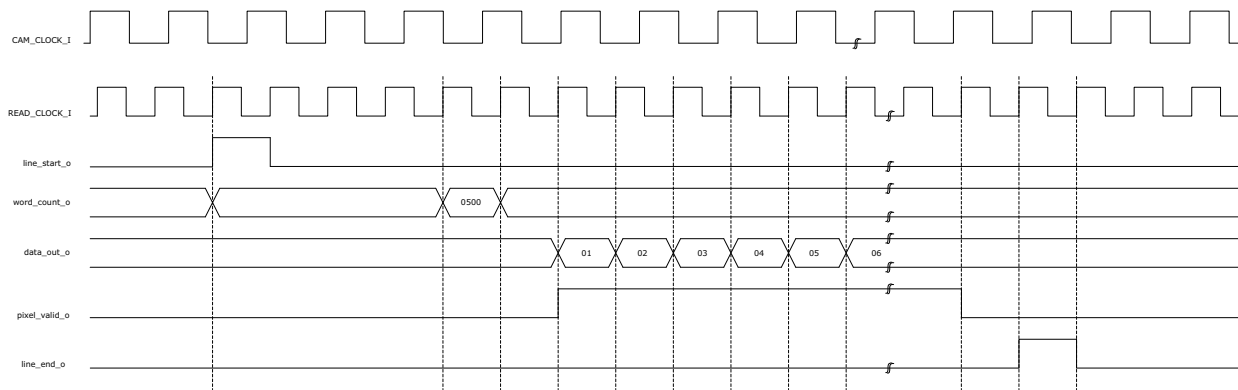
Name	Description
g_DATAWIDTH	Input pixel data width. Supports 8-bit, currently.
g_INPUT_DATA_INVERT	To invert the incoming data: 0 - does not invert the incoming data 1 - inverts the incoming data
g_BUFF_DEPTH	Depth of the buffer.

3.4 Timing Diagrams

3.4.1 Long Packet

The following illustration shows the timing waveform of long packet.

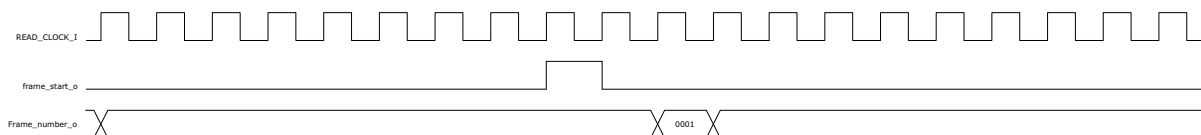
Figure 5 • Timing Waveform of Long Packet



3.4.2 Short Packet

The following illustration shows the timing waveform of frame start packet.

Figure 6 • Timing Waveform of Frame Start Packet



3.5 Resource Utilization

The following table shows the resource utilization of a sample MIPI CSI-2 Receiver Core implemented in a SmartFusion[®]2 M2S150T-1152FC device.

Table 4 • Resource Utilization of the MIPI CSI-2 Receiver Decoder

Cell Usage	Description
DFFs	925
4-input LUTs	1035
MACC	0
RAM1Kx18	0
RAM64x18	16