Libero SoC PolarFire v1.1 Service Pack 1

Release Notes

6/2017

Microsemi

Power Matters.™

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1 Revision History

Revision 3.0

- Updated Table of Cores to include links to details.
- Updated TXPLL connection information for PCIE
- Fixed incorrect display text for Link to Product Overview User Guide

Revision 2.0

- Updated Table of Cores to include "Display Name" and current Version.
- Additional documentation of TX_PLL, XCVR, and PCIE migration issues
- Links to Software download (Windows and Linux) included

Revision 1.0

This is the initial release of these Release Notes.

2 Reference Documents

PO0137: Product Overview PolarFire FPGA

DS0141: PolarFire FPGA Datasheet

UG0722: PolarFire FPGA Packaging and Pin Descriptions User Guide

Pin package Assignment Tables:

- MPF300T/MPF300TS-FCG484 Package Pin Assignment Table
- MPF300T/MPF300TS-FCVG484 Package Pin Assignment Table
- MPF300T/MPF300TS-FCSG536 Package Pin Assignment Table
- MPF300T/MPF300TS-FCG784 Package Pin Assignment Table
- MPF300T/MPF300TS-FCG1152 Package Pin Assignment Table

UG0752: PolarFire FPGA Power Estimator User Guide

UG0680: PolarFire FPGA Fabric User Guide

UG0684: PolarFire FPGA Clocking Resources User Guide

UG0686: PolarFire FPGA User I/O User Guide

UG0677: PolarFire FPGA Transceiver User Guide

UG0685: PolarFire FPGA PCI Express User Guide

UG0687: PolarFire FPGA 1G Ethernet Solutions User Guide

UG0727: PolarFire FPGA 10G Ethernet Solutions User Guide

UG0676: PolarFire FPGA DDR Memory Controller User Guide

UG0748: PolarFire FPGA Low Power User Guide

Athena TeraFire Cryptographic Algorithm Library (CAL) Users Guide

UG0743: PolarFire FPGA Debugging User Guide

UG0714: PolarFire FPGA Programming User Guide

UG0725: PolarFire FPGA Device Power-Up and Resets User Guide

UG0726: PolarFire FPGA Board Design User Guide

UG0753: PolarFire FPGA Security User Guide

DG0755: PolarFire FPGA JESD204B Interface Demo Guide

DG0756: PolarFire FPGA PCIe Endpoint Demo Guide

DG0757: PolarFire FPGA 10GBASE-R Ethernet Loopback Demo Guide

DG0759: PolarFire FPGA Multi-Rate Transceiver Demo Guide

DG0762: PolarFire FPGA DSP FIR Filter Demo Guide

Verilog Simulation Guide

VHDL Simulator Guide

PolarFire Design Flow User Guide

PolarFire FPGA Macro Library Guide

Design Constraints User Guide

PolarFire FPGA PDC Commands User Guide

PolarFire Timing Constraints User Guide

PolarFire FPGA Tcl Commands User Guide

PolarFire FPGA I/O Editor User Guide

Chip Planner User Guide

Netlist Viewer Interface User Guide

Netlist Viewer User Guide

SmartPower User Guide

Timing Constraints Editor User Guide

SmartTime Static Timing Analyzer User Guide

PolarFire SmartDebug User Guide

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3   Libero SoC PolarFire™ v1.1 SP1 Software Release Notes

The Libero® system on chip (SoC) PolarFire™ v1.1 SP1 release is a service pack release of the Libero SoC PolarFire v1.1 software for designing with Microsemi PolarFire FPGAs. PolarFire FPGAs are the fifth generation nonvolatile FPGA devices from Microsemi, built on 28-nm flash technology. The PolarFire cost-optimized FPGAs deliver lowest power at mid-range densities.

For more information about Libero SoC PolarFire devices, see the Microsemi website.

3.1   What's New in this Release

This release includes the following new features and enhancements:

- First release to support MPF100
- First Release to support Synopsys Identify tool.
    - The Identify ME Debugger version L2016.09M-G5 that supports PolarFire family is not shipped with the PolarFire v1.1 SP1 release, but is available for download **here**.
- Design and Memory Initialization Tool in Design Flow creates initialization clients for programming and improves upon previous two-stage process:
    - Stage 1 – Assertion of FPGA Core and I/O ready signals
    - Stage 2 – PCIe blocks initialized
    - Stage 3 – non-PCIe XCVR blocks and Fabric RAMs initialized

  NOTE: Initialization can now be performed from SPI Flash as well as sNVM and uPROM

  NOTE: The Design and Memory Initialization tool must be rerun for any design change. This requirement is not enforced by the Libero SoC PolarFire software in this release.

- A Transceiver Burst Mode Receiver option has been added to support protocols such as XGPON.
- Automated transceiver initialization is supported for configurations in the following range
    - Transmitter is fixed at 400mV with -3.5dB de-emphasis.
    - Receiver is fixed to short reach settings only
        - Short Reach settings are defined as connections within a board or via one connector to a daughter card with a total insertion loss of 6.5 dB @ 5 GHz. This is estimated to be less than 200 mm (~8 inches) strip-line of Nelco FR-4 with width=7mil and space=10mil.
        - The CTLE settings are fixed based on the serial data rate.

Data Rate	DC Gain	Peaking
250Mbps – 8.475Gbps	5.5 dB	2.1 dB
8.475Gbps – 10.3125G	-2.1 dB	5.4 dB
10.3125Gbps – 12.7Gbps	Not Supported	Not Supported

- Improved PolarFire I/O Editor (see PolarFire I/O Editor User Guide)
    - Memory View - For each DDR location, Max Memory Width and Max Data Rate columns have been added to let users see at a glance valid DDR locations that can accommodate the memory width and/or data rate of the DDR in the design.

- Memory View –DRC checking to ensure that DDR memory placement is feasible with respect to width, data rate, and speed grade
- SmartDebug now supported for PolarFire (see PolarFire SmartDebug User Guide), with the following features being in the Libero PolarFire v1.1 SP1 release
  - Transceiver Debugging
  - uPROM Debugging
  - Logical View
  - Live Probe
  - Probe Insertion
  - Active Probe Read
  - Fabric SRAM Read/Write
- Tamper Events Management, using the PF_TAMPER Core and configurator
- Cryptography microprocessor, using the PF_CRYPTO Core and configurator
- Full Support for the Clock Conditioning Circuitry (CCC) DLL functions:
  - Reference, phase, and injection removal clock modes
  - Phase shifting

3.2   Limitations of This Release

This release has the following limitations:

- Post-synthesis and post-layout simulations are not supported.
- IBIS generation is not supported.
- Design Block Flow (bottom-up design reuse methodology) is not supported.
- Automated transceiver initialization support is limited to ranges specified in the "What's New" section above.
  - DFE is currently not supported.
  - Contact Microsemi Technical Support for assistance with settings outside of those defined above.

3.3   System Requirements

- 64-bit OS
  - Windows 7, Windows 8.1, or Windows 10 OS
  - RHEL 5, RHEL 6, RHEL 7, CentOS 5 ,CentOS 6, or CentOS 7
    - Programming is not supported on RHEL 5, CentOS 5
- A minimum of 32 GB RAM

Note: Setup instructions for using Libero SoC on Red Hat Enterprise Linux OS are available on the Libero SoC Documents web page. As noted in that document, installation step 2 now includes running a shell script (bin/check_linux_req.sh) to confirm the presence of all required runtime packages.

3.4   Timing and Power Data

- The timing and power data in this release are in the "Advance" state. In this state, data is extracted using electrical simulation but is not yet considered final. Adjustments in future releases are still possible based on silicon measurements.

3.5 Device Support

Libero SoC PolarFire Device Support

Device	Package	Speed Grade	Core Voltage	Required License
MPF100TS_ES	**Fully bonded package**	-1	1.0/1.05V	Eval/Silver/Gold/Platinum
MPF200TS_ES	Fully bonded package	-1	1.0 /1.05V	Eval/Gold/Platinum
MPF300T_ES	FCG1152E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCG484E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCG784E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCSG536E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCVG484E	-1, STD	1.0/1.05V	Eval/Platinum
MPF300TS_ES	FCG1152E	STD	1.0 /1.05V	Eval/Platinum
		-1	1.0 /1.05V	Eval/Gold/Platinum
	FCG484E	STD	1.0 /1.05V	Eval/Platinum
		-1	1.0 /1.05V	Eval/Gold/Platinum
	FCG784E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCSG536E	-1, STD	1.0 /1.05V	Eval/Platinum
	FCVG484E	-1, STD	1.0 /1.05V	Eval/Platinum

Devices in **bold** are new in SP1.

See the Licensing web page for details.

3.5.1 Silver license users

To simulate your design:

1. Download and install ModelSim ME 10.5C from the Microsemi web site
2. Open Libero and set the tool profile to point to ModelSim
3. Go to Project -> Project Settings and at the bottom of the tree, under Simulation libraries -> PolarFire, browse to the <libero install>/lib/modelsimpro/polarfire directory
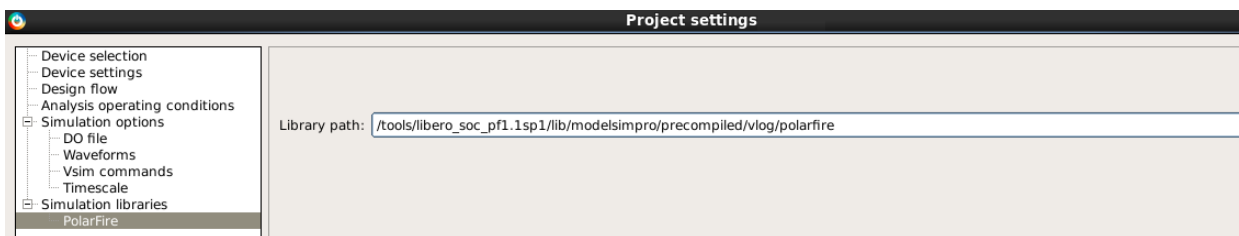
3.6 Design Migration – Cores

You must upgrade all cores to the latest version and re-generate existing designs through full implementation and timing verification flow.

Display Name	Latest Version	Change Status	Notes
Clock Conditioning Circuitry (CCC)	1.0.107	Must Upgrade	See details below
Clock divider	1.0.100	No Change	
Crypto	1.0.100	New	
DDR3	1.0.245	Must Upgrade	See details below
DDR4	1.0.236	Must Upgrade	See details below
PF Dual-Port Large SRAM	1.1.109	No Change	
PolarFire Dynamic Reconfiguration Interface	1.0.100	No Change	
PolarFire Initialization Monitor	1.0.100	No Change	
PolarFire IOD CDR	1.0.203	Must Upgrade	
PolarFire IOD Generic Interfaces	1.0.101	Must Upgrade	
Glitchless clock mux	1.0.100	No Change	
PolarFire RC Oscillators	1.0.100	No Change	
PCI Express	1.0.217	Must Upgrade	See details below
PolarFire SRAM (AHBLite and AXI)	1.1.117	Must Upgrade	
Tamper	1.0.101	New	
PF Two-Port Large SRAM	1.1.107	No Change	
Transmit PLL	1.0.105	Must Upgrade	See details below
PF uPROM	1.0.107	No Change	
PF Micro SRAM	1.1.106	No Change	
Transceiver Interface	1.0.214	Must Upgrade	See details below See also: Clocking with TX_PLL
Transceiver Reference Clock	1.0.101	Must Upgrade	

Upgrade details:

- **DDR**

  With this release, you must upgrade the version of the DDR3/4 cores to the latest version available; after upgrading the core version you must re-generate your design and run the design through the full implementation flow and timing verification flow

- **PF_CCC**

  With this release, Libero SoC PolarFire software provides full support for the Clock Conditioning Circuitry (CCC) DLL functions:
  - Reference, phase and injection removal clock modes
  - Phase shifting

  With this release, you must upgrade the version of the PF_CCC core to the latest version available; after upgrading the core version you must re-generate your design and run the design through the full implementation flow and timing verification flow.

  Note that although there have been no changes to the PLL feature available in the PF_CCC core, you still must upgrade to the latest PF_CCC core version.

- **XCVR**
  - All lanes in a single configured XCVR core are now required to have the same clocking requirements. See the 'Clocking Connectivity Changes' section below.
  - The 'Bit slip' option is now only available for the PMA mode option. Note that in the case of '8b10b' the 'bit slip' port is no longer present and the 'bit slip' function is automatically set internally as it is required to function correctly.

    If the design being migrated to PolarFire v1.1 SP1 has an XCVR core configured to use 8b10b PCS, then upon upgrade to the latest XCVR core version, the UI option 'Enable CDR Bit-slip port' now under the 'PMA Mode' PCS Settings option is enabled(checkbox is checked). But since the 'Enable CDR Bit-slip port' option is now supported only in the PMA mode, clicking OK in the configurator now will throw an error message "Error: CDR Bit-slip port must be disabled in 8b10b mode" in the XCVR configurator log window.

    - **Follow the steps** below to work around this issue:
      1. Open the XCVR configurator, select 'PMA Mode' option under the PCS Settings.
      2. Reselect '8b10b Encoding/Decoding' option.
      3. Review all other UI settings and click OK to save and exit the configuration.

      This will disable the 'Enable CDR Bit-slip port' option (uncheck the checkbox). The LANE<0/1/2/3>_RX_SLIP input port will no longer be seen and the 'bit slip' function is automatically set internally in 8b10b mode.

    - **Alternatively:** delete any current instances and create new ones using the latest XCVR version

  - Dynamic Reconfiguration options have been reorganized under the 'Dynamic Reconfiguration' group.

- **Clocking Connectivity Changes affecting PCIe, XCVR, TX_PLL**
  - To simplify the connectivity between TxPLL and XCVR/PCIe blocks various clock related signals have been bundled into a single Bus Interface port. When used within a SmartDesign, the new XCVR clock Bus Interface port simplifies the connectivity and enforces architecture rules at the same time.
  - Note that all lanes in a single configured XCVR core are now required to have the same clocking requirements. Instantiate multiple XCVR cores (with the appropriate configurations) if your lanes have different clocking requirements.

o   As a result, for a design which previously looked like this:

Pre PolarFire V1.1 -SP1 Solution

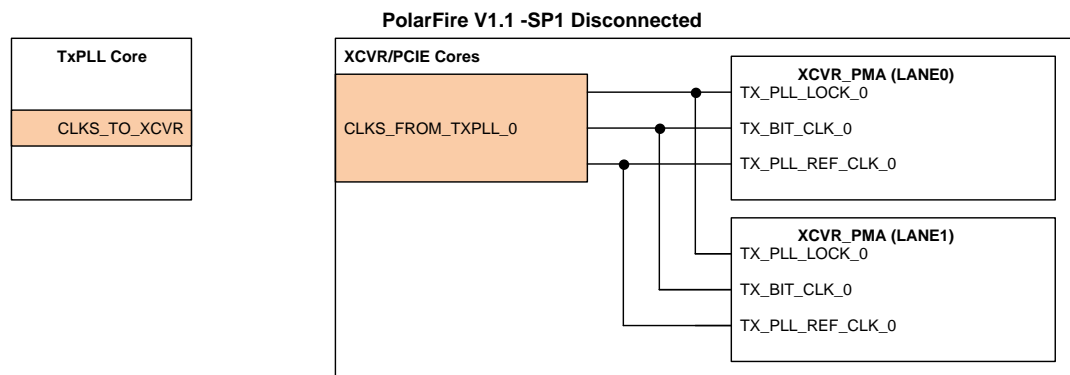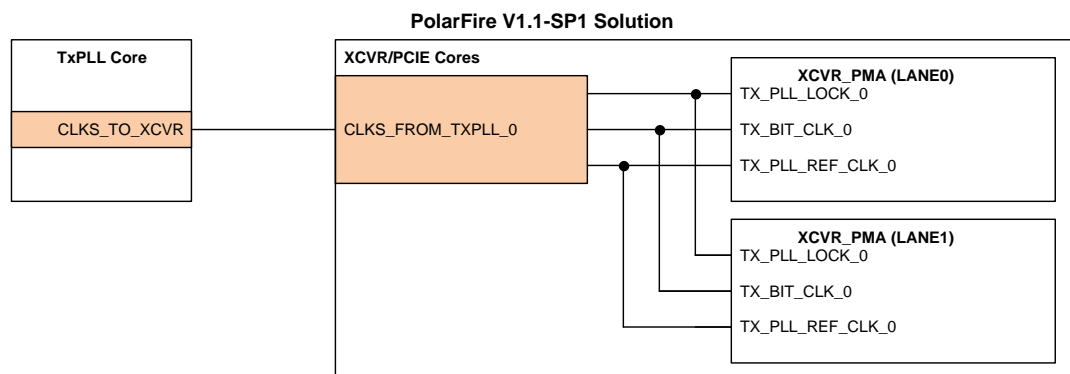| TxPLL Core		XCVR/PCIE Cores	
LOCK		LANE0_TX_PLL_LOCK_0	**XCVR_PMA (LANE0)** TX_PLL_LOCK_0
BIT_CLK		LANE0_TX_BIT_CLK_0	TX_BIT_CLK_0
REF_CLK_TO_LANE		LANE0_TX_PLL_REF_CLK_TO_LANE_0	TX_PLL_REF_CLK_0
		LANE1_TX_PLL_LOCK_0	**XCVR_PMA (LANE1)** TX_PLL_LOCK_0
		LANE1_TX_BIT_CLK_0	TX_BIT_CLK_0
		LANE1_TX_PLL_REF_CLK_TO_LANE_0	TX_PLL_REF_CLK_0
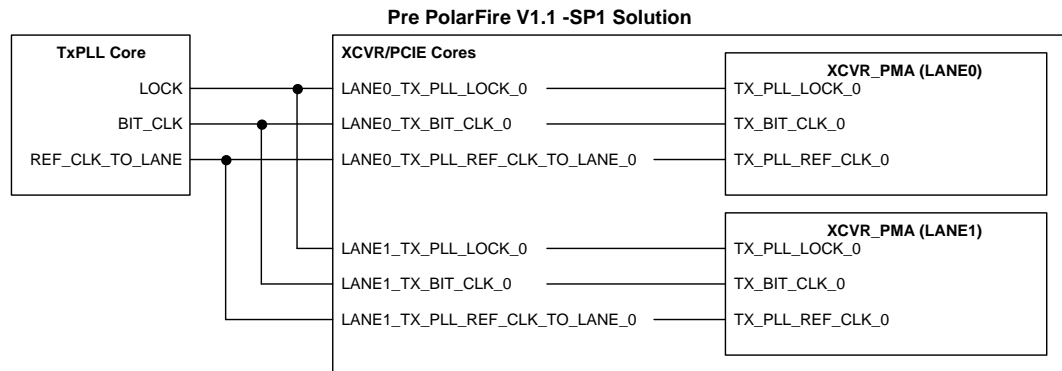
The signals {LOCK, BIT_LOCK, REF_CLK_TO_LANE} that were driven by TX_PLL will be disconnected.

- On the TX_PLL Core, these are replaced by the bus: CLKS_TO_XCVR
- The XCVR Core, now has just one bus connection from TX_PLL, since the XCVR clocks must be identical for all lanes (for PCIE there will be two bus connections since the PCIE Core has two PCIE controllers)

The user will therefore see the following design after update …

PolarFire V1.1 -SP1 Disconnected

TxPLL Core	XCVR/PCIE Cores	
CLKS_TO_XCVR	CLKS_FROM_TXPLL_0	**XCVR_PMA (LANE0)** TX_PLL_LOCK_0
		TX_BIT_CLK_0
		TX_PLL_REF_CLK_0
		XCVR_PMA (LANE1) TX_PLL_LOCK_0
		TX_BIT_CLK_0
		TX_PLL_REF_CLK_0

and must then connect the CLKS_TO_XCVR to the CLKS_FROM_TXPLL_0 bus ports (or to CLKS_FROM_TXPLL_TO_PCIE_0, CLKS_FROM_TXPLL_TO_PCIE_1 for the PCIE Core).

PolarFire V1.1-SP1 Solution

TxPLL Core	XCVR/PCIE Cores	
CLKS_TO_XCVR	CLKS_FROM_TXPLL_0	**XCVR_PMA (LANE0)** TX_PLL_LOCK_0
		TX_BIT_CLK_0
		TX_PLL_REF_CLK_0
		XCVR_PMA (LANE1) TX_PLL_LOCK_0
		TX_BIT_CLK_0
		TX_PLL_REF_CLK_0

o   Additional TX_PLL issues on upgrade.

- Consider the case of a design created in PolarFire v1.1, in which Core components were created using the "Configure Core" mechanism, and instantiated and connected together in a top level Smart Design (direct instantiation without creating Core components will not have this problem).

    1. Open the design PolarFire v1.1 SP1. All the core components are invalidated as expected.
    2. Right click on the TxPLL core component in the Design Hierarchy and replace the component core to the latest version. The core is upgraded and generated.
    3. Do the same for XCVR and XCVR_REF_CLK core components in the Design Hierarchy. (XCVR should be reconfigured and regenerated to account for the latest UI parameter changes.)

    Observed:

    o   In the Smart Design canvas where these core components have been instantiated, the TxPLL component instance doesn't go out of date. The new clock bus interface port "CLKS_TO_XCVR" is not exposed on this TxPLL component instance.

    Workaround:

    o   Delete the existing instance, re-instantiate the same TxPLL component from the Design Hierarchy to be able to see the updated port-list with the new clock bus interface port "CLKS_TO_XCVR".

4 Resolved Issues

The following table lists the customer-reported SARs resolved in Libero PolarFire v1.1 SP1. Resolution of previously reported "Known Issues and Limitations" is also noted in this table.

Customer SARs Resolved in PolarFire 1.1 SP1 (including previous release notes)

Customer Case #	Description
PF 1.0 Release Note	Derived constraints with brackets does not pass place and route
PF Release Note	RX_SLIP should be disabled for 8b10b
PF 1.1 Release Note	uPROM address boundaries not checked.
PF 1.1 Release Note	In 8b10b mode the RX_SLIP port should not be used
PF 1.1 Release Note	Auto Update for SPI not being programmed on device
493642-2268812377	Place and Route could not find legal location for DDR3 clock.
493642-2279438509	Fix TxPLL simulation model DIV_CLK signal
493642-2282462655	Need PolarFire-specific Tcl command Reference Guide
493642-2308416669	Cannot program Eval-Kit with GOLD License using Program Device in Libero
	Crash when files larger than 3.7GB created.
PF 1.0 Release Note	Should be able to disable both UEK1 and UEK2
PF 1.1 Release Note	TVS_Monitor information displayed after ISC_ENABLE
PF 1.0 Release Note	BSDL safe value must be updated
	Add IOSTD for DDR Interfaces
PF 1.0 Release Note	DRC rules for MPF200TS_ES device are incomplete
	Crash bringing up Reports Window (when simulation file > 3.7GB)
	Error msg "Instance 'PF_CCC_0/clkint_0 (GB)' must be placed and locked .." even though it is placed and locked
	REFCLK to dedicated PLL net not working in all cases
	Find integer solution for set of frequencies for CCC configuration automatically

4.1 Status of DDR3/DDR4 Memory Solutions

All DDR3 and DDR4 configurations offered by the DDR3 and DDR4 cores can be used to create designs, validate design through simulation as well as running place and route and verifying the overall timing of the design.

This release provides specific support on hardware for DDR3 16-bit and 32-bit memories, at up to 1333 Mbps. The DDR3 memory controller must be placed on the NORTH (NE/NW) DDR3 memory locations (HSIO banks).

You must upgrade the version of the DDR3 and DDR4 cores to the latest version available with this release; after upgrading the core version you must re-generate your design and run the design through the full implementation flow and timing verification flow.

See also Known Issues: DDR3/4 Section 5.3

5   Known Issues and Limitations

5.1   Design Initialization Clients

The Design and Memory Initialization tool must be run for all design changes. This requirement is not enforced by the Libero SoC PolarFire design flow manager in this release. Users should always re-generate the initialization clients every time they run the 'Generate FPGA Array Data' step in the design flow.

Failure to run the Design and Memory Initialization tool may result in a chip that will not work properly.

5.2   RAM Initialization

- RAM initialization at Power Up is only supported for the PolarFire Dual-Port Large SRAM, Two-Port Large SRAM, AHBLite Core, and Micro SRAM cores.
- RAM initialization at Power Up is not supported for RAMs inferred during Synthesis.
- The RAM initialization tool does not support the import of memory files with a space in the file path.

5.3   DDR3/4

- The DDR3 memory controller must be placed on the NORTH (NE/NW) DDR3 memory locations (HSIO banks). However, all DDR3 Core configurations will validate through simulation and post-place and route timing verification.
- Placement fails if DDR4 is configured using a bank group address width value of 1. Change the value to 2 (DDR4 Configurator > General > Bank Group Address Width).
- Full simulation may take about 30 minutes, depending on machine resources and the simulator used. A faster simulation mode will be provided in a future release.
- Multi-rank SDRAM is currently not supported.
- DBI (DDR4) is currently not supported.
- Four of the DDR3 presets are not working in simulation.

  o   DDR3-1333H (9-9-9) - 1 Gb x 16 - CL 5 - CWL 5

  o   DDR3-1333H (9-9-9) - 1 Gb x 16 - CL 6 - CWL 5

  o   DDR3-1333H (9-9-9) - 1 Gb x 16 - CL 7 - CWL 6

  o   DDR3-1333H (9-9-9) - 1 Gb x 16 - CL 8 - CWL 6

- Even though the DDR3 configuration GUI will allow specification of up to 8 DDR3 instances, only 6 DDR3 instances are physically possible

5.4   CCC

- Only the post-VCO feedback mode is available in this release.
- Bypass option on output clocks is not available in this release.
- In DLL Phase Generation Mode, the secondary output clocks are not producing the correct phase in simulations.

5.5 PCIe

- The AXI interface minimum clock frequency is 125 MHz. If the user would like the AXI4 to run slower, the CoreAXI4Interconnect uses a clock per interface to allow the PCIe to run at 125MHz while the rest of the design can run slower.

- For BFM simulation of AXI master or slave, the simulator may print out a warning message about AHB signals, such as "HRESP". The warning message can be ignored.

5.6 Transceiver

- Transceiver lanes may lose the LOCK signal after some simulation time as can be seen in the RX_VAL signal becoming de-asserted sometime after being asserted.

   Workaround: For all designs using the PF_XCVR macros, change the default resolution (Project > Project Settings > Vsim Commands > Resolution) from the default 1ps to 1fs. Note that switching to a finer simulation time step will incur some simulation runtime penalty.

5.7 TX_PLL

- In PF_TX_PLL simulation, the DIV_CLK frequency will not be responsive to the output divider setting.

- Libero flash bits settings for EXTPLL_CLK_SEL are wrong in XCVR Cascading for last TX_PLL on die.

5.8 I/O and I/O Bank Known Issues

- For FCG484/FCVG484/FCSG536 – I/O Bank 4 and Bank 5 must have the same VDDI, but I/O Editor and ChipPlanner do not enforce that requirement. Specifying different VDDI will fail during Place and Route. User must specify the same VDDI for both I/O banks.

- Multiple voltages in an I/O bank are not supported in this release.

5.9 Synplify Pro Warns About Unrecognized Part and Device Family

When Synplify Pro is invoked interactively in the Libero SoC PolarFire software, a warning message appears: "Unrecognized Speed Grade -1 specified for Package FBGA896…." This warning message can be ignored.

5.10 No EDIF Source File Import

Do not import an EDIF design source file into the Libero SoC PolarFire project. Import only HDL design source files, or mapped Verilog netlist (*.vm files) from Synthesis as design source files.

5.11 SmartDebug → Standalone flow

1. Export DDC file in Libero does not support bitstream option.

   Recommended flow for users is to Program the device using FlashPRO (windows only) or through Load Programming File option in Programming Connectivity and Interface dialog of SmartDebug (both Windows and Linux platforms).

Use Import Debug Data from DDC file option to import debug file contents to debug the device if the debug project is created using Construct Chain Automatically option. The other option is to import the DDC file during debug project creation after programming the device using FlashPRO/FPExpress/SmartDebug

- o DDC file export fails when bitstream information is included for export

2. Non Microsemi Devices in chain: Microsemi devices present in chain along with non-Microsemi devices cannot be debugged using standalone SmartDebug.

   Workaround: Users should use SmartDebug through Libero flow in order to debug Microsemi Devices

   - o Standalone SmartDebug: ID Code of Microsemi device cannot be read when non-Microsemi device is connected in chain

3. Device cannot be debugged if DDC file exported without FPGA Array Probe Points or FPGA Array Memory Blocks

   - o Standalone SmartDebug: DDC file exported without Probes do not show memory blocks

   - o Standalone SmartDebug: DDC file exported without memory blocks results in crash when Debug FPGA Array data is opened

4. Programmer selection defaults to the first programmer in the list when DDC file is used to create new debug project. This issue is seen when multiple FlashPRO programmers are connected to the machine.

   Workaround: Select the correct programmer after the debug project gets created from the Programmer drop-down menu

   - o Standalone SmartDebug: Programmer selection is not retained on doing DDC import in New Project

5. Switching of debug devices connected in chain: Debug Transceiver (for PolarFire devices) and Debug SERDES (for SmartFusion2/IGLOO2 devices) labels do not get updated when devices connected in JTAG chain are switched for debug through SmartDebug UI. The text of the label refers to the first device connected in chain.

   - o Standalone SmartDebug: Debug SERDES and Debug XCVR labels get interchanged for PF and SF2/IGLOO2 devices when connected in chain

6. Import Debug Data from DDC file and Load Programming File options in Programming Connectivity and Interface are mutually exclusive operations i.e. DDC file contents loaded using Import Debug Data option are lost when Programming file contents are loaded using the latter option and vice versa.

   - o Standalone SmartDebug: Import Debug Data from DDC and Load Programming File are seen as mutually exclusive operations in JTAG chain

7. Security settings exported in the DDC file do not get loaded into the debug project when PolarFire device is present in JTAG Chain and debug file contents are loaded using Import Debug Data from DDC file option in Programming Connectivity and Interface.
   Workaround: Import the DDC file during debug project creation in Import DDC dialog.

   - o Standalone SmartDebug: Autoconstruct issues when PolarFire device is present in chain

5.12 SmartDebug → Logical View

1. Logical view cannot be reconstructed for LSRAM/uSRAM for port widths of x1 inferred through RTL.

2. Logical view cannot be reconstructed for LSRAM/uSRAM configurations when a single net of output bus is used i.e. A_DOUT[0]/B_DOUT[0] for DPSRAM/uSRAM and RD[0] for TPSRAM and others are unused. The memories can be read/write using physical view.

3. Logical view cannot be reconstructed for LSRAM/uSRAM configurations inferred using IP Cores CoreAHBLtoAXI (Verilog flow), CoreFIFO (Verilog and VHDL flow).

4. Logical view cannot be reconstructed when HDL module inferring RAM blocks is instantiated in SmartDesign.

   o Logical View: Unable to construct Logical View for the SmartDesign with the RAM HDL Module Instantiation

5.13 SmartDebug → uPROM Debug

uPROM clients added through Device and Memory Initialization tool are not shown in Debug uPROM.

   o Debug UPROM: Clients added to the UPROM in Device and Memory Initialization tool is not shown in the Debug UPROM

5.14 Installation on Local Drive Only

This release is intended for installation only on a local drive. The Installer might report permission rights problems if the release is installed across a networked drive.

5.15 Installation

C++ installation error can be ignored. Required files will install successfully.

On some machines, the InstallShield Wizard displays a message stating:

The installation of Microsoft Visual C++ Redistributable Package (x86) appears to have failed. Do you want to continue the installation?

Click Yes and the software is installed successfully.

5.16 Antivirus Software Interaction

Many antivirus and HIPS (Host-based Intrusion Prevention System) tools will flag executables and prevent them from running. To eliminate this problem, users must modify their security setting by adding exceptions for specific executables. This is configured in the antivirus tool. Contact the tool provider for assistance.

Many users are running Libero SoC successfully with no modification to their antivirus software. Microsemi is aware of issues for some antivirus tool settings that occur when using Symantec, McAfee, Avira, Sophos, and Avast tools. The combination of operating system, antivirus tool version, and security settings all contribute to the end result. Depending on the environment, the operation of Libero SoC, ModelSim ME and/or Synplify Pro ME may or may not be affected.

All public releases of Libero are tested with several antivirus tools before they are released to ensure that they are not infected. In addition, Microsemi's software development and testing environment is also protected by antivirus tools and other security measures.

6   Download Libero SoC PolarFire v1.1 SP1 Software

Libero SoC PolarFire v1.1 SP1 is an incremental service pack and must be installed over Libero SoC PolarFire v1.1.

The following are available for download:

Libero SoC PolarFire v1.1 SP1 for Linux or Windows

Note: Installation requires administrative privileges.