CR0031
Characterization Report
RTG4 Characterization Report For PCIe

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About Microsemi

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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 1.0

Revision 1.0 is the first publication of this document.

2 RTG4 Characterization Report For PCI Express

The Microsemi RTG®4 FPGA families provide a fully embedded PCI Express® Gen1- x1/x2/x4 endpoint. This embedded PCI Express solution is part of the SERDES block module which supports 4 lanes of SERDES with data rates supported up to 2.5 Gbps. The RTG4 devices support up to 2 SERDES block modules with PCIE functionality for a total of 2 PCI Express interfaces. For more information on the RTG4 FPGA family, see https://www.microsemi.com/products/fpga-soc/radtolerant-fpgas/rtg4.

2.1 Scope of this Report

Complete testing and validation of specifications required by Gen1 PCI Express standard were conducted on the RTG4 FPGA devices. This report provides the user community a summary of both PCIe related device testing and characterization as well as results of the compliance testing conducted at PCISIG testing workshops. Comprehensive testing was done to characterize the PCIe electrical performance of the device. The testing analyzed voltage, temperature, and process variations for specific PCIe parameters and higher level testing was conducted to verify the link and protocol functionality of the RTG4 PCIe solution. This report serves as a reference to the specific testing used to provide high confidence that the devices will perform as expected in PCI Express systems.

2.2 PCISIG Compliance Testing

PCISIG is the industry organization chartered to develop and manage the PCI standards. The PCISIG Compliance Program offers the latest in PCI device testing, including the opportunity to test your system or Add-in Card with other members' PCI products. Completing testing at the PCISIG Compliance Workshop will enable devices to be added to the PCISIG Integrators Listing.

A traditional PCI Express system utilizes a CPU connected to a root device, which is responsible for configuring and enumerating all PCI Express endpoint devices within the system. A point-to-point PCIe system requires a switch device to grow the number of endpoint devices present with one root and one or more endpoint devices. An FPGA-based endpoint provides a high level of integration enabling high-performance, fully compliant PCI Express systems in a single device. The use of the FPGA-based endpoint add-in cards have become the de-facto means for testing PCIe Gen1 standard at PCI Express workshops.

2.3 Compliance Testing

There are four encompassing areas of PCI Express compliance testing for components tested on add-in cards:

Electrical Testing—Examines the device and add-in card signal quality for eye pattern, jitter, and 2.5 Gbps data rate analysis.

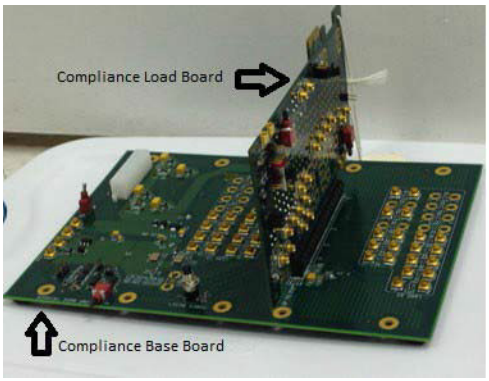
Configuration Space Testing (CV)—Examines the configuration space in PCI Express devices by verification of required fields and values.

Link and Transaction Protocol Testing (PTC)—Tests the device behavior for link-level protocol and device behavior for transaction-level protocol. Link and transaction layers are exercised for protocol boundary conditions. Tests include error injection and check error-handling capabilities.

2.3.1 Electrical Testing

PCI Express Electrical Testing was developed to verify product-level physical compliance to the PCI Express CEM specification(s). PCI Express Electrical Testing consists of a series of tests used to evaluate PCI Express products. A series of tests were performed on Microsemi boards in conjunction with the PCISIG compliance base board (CBB) and the compliance load board (CLB) to validate signal quality of TX, Ref Clock, and PLL Loop Bandwidth.

Figure 1 • **PCIe Compliance Test Channel**



Once data is collected from the test platforms, analysis software is used on the collected information to determine whether the device meets the specifications or not.

The test criteria are specified in the PCI Express Architecture PHY Electrical Test Considerations Revision 2.0.

PCIe Gen1 electrical tests conform to section 4.3 of the PCI_Express_Base_r2_1_04March09.pdf and the PCI_Express_CEM_r2.0.pdf.

2.3.2 Configuration Space Testing

The PCI Express Configuration Verifier (CV) test is a software application provided by PCISIG that runs on a Windows 7 32-bit PC and exercises access to the configuration space registers of the device under test. Its purpose is to check for compliance with the PCIe specification for configuration space registers (type 1-switch/bridge). A detailed description of tests performed can be found in the document PCI EXPRESS ARCHITECTURE CONFIGURATION SPACE TEST SPECIFICATION, REV. 2.0. The tests are conducted with the Add-in Card placed in a PCI Express slot in the PC. The test software accesses the Add-in Card and issues configuration read and write requests and checks for the correct response.

These specification documents are only available to PCISIG members at http://www.pcisig.com/specifications/pciexpress.

The tests check the following:

- Configuration space registers can be read
- Read-only registers retain their value when attempted to be written to
- Writable registers can be written to
- Registers have the correct default value after reset
- Capabilities lists are valid and correctly linked
- PCI Express 2.0, 1.1, and/or 1.0a specific fields and capabilities are present

The test program also performs functional stress tests to ensure the endpoint can re-train and re-link in an acceptable amount of time. It also tests to ensure the card can properly handle hundreds of cycles of link-up/link-down and all registers are operational (such as the endpoint firmware has not locked up). In summary, the CV test suite verifies that the PCI Express endpoint is truly functional in a PC and covers all aspects of hardware and operating system interaction. It shows that the card can be recognized by the PCI Express hardware and can be enumerated and configured by the operating system for access by software applications.

2.3.3 Link and Transaction Protocol Testing

The PCI Express Link and Transaction Layer protocol testing was developed to test the add-in card compliance to the Link and Transaction protocol specification requirements. The testing utilizes the E2969B Protocol Test Card 2 (PTC-2) and the test code from Agilent Technologies or the Teledyne LeCroy Protocol Test Card. Both PTC cards exercise all required tests that the PCISIG will conduct during its compliance workshops by using this Agilent hardware. The PTC-2 exercises specifications for the Transaction Layer and the Data Link Layer, and monitors the behavior of the device in response to

certain error conditions. The PTC card is simply attached to the PCI Express add-in card under test and performs all mandatory tests from the PCISIG.

Figure 2 • **Agilent PTC-2**

These vendors' test packages contain PTC test code that is compatible with, and requires any of the Agilent E2960B or LeCroy PTCG2 family software packages, available on the Agilent or LeCroy websites free of charge. During link testing, the following tests are run using the PTC card. All of the following tests must be passed in order to be included on the Integrators List.

Table 1 • **Link Tests Using PTC Card**

Bad CRC	Device detects, drops, and logs (DLLPs and TLPs)
Bad Sequence Number	Device detects, drops, and logs
Duplicate TLP	Device returns data once
Link Retrain	Device will retrain if continued no response
NAK Response	Device will resend after receiving NAK
Replay Count	Device will resend multiple times when no response
Replay Timers	Device will resend packet if no response
Replay TLP Order	Device replays TLPs in proper order
Reserved Fields	Device ignores reserved fields
Undefined Packet	Device ignores undefined packets

2.4 Microsemi Test Boards

Testing is performed on two types of boards which are dependent on the test requirements. Both boards are equipped with a test socket, which accommodates testing a variety of parts. The socket slightly contributes to attenuation and jitter, which will slightly degrade the testing results although the design of the boards minimizes this effect.

2.4.1 Signal Integrity Board (SI)

The SI board is equipped with a test socket and provides connections to vary power supply conditions. To ensure the integrity of the characterization measurements, special attention is given to the signal integrity of the high-speed serial channels. Detailed analysis ensures the board performs as designed. The transmitter (TX) and receiver (RX) signal paths for each SERDES are carefully routed to high-bandwidth SMP connectors to ensure good signal integrity and performance. The PCB channel is measured and de-embedded when performing tests.

2.5 Device Electrical Testing

PCI Express I/O electrical characterization testing was completed by Microsemi over device process, voltage, and temperature variations (PVT). Testing was conducted on a sample of devices representing process fluctuations across silicon fabrication. These devices were separated from a large sample and represented the worse-case corners to report the results. The results are correlated and presented in the data as worst-case. The testing procedures verify the device can achieve critical specification targets such as:

- Jitter
- Eye mask
- Different De-emphasis levels
- Reference Clock
- Voltage and Jitter margining
- Receiver Margining

The following PCIe electrical characterization tests were conducted on the clock configuration:

- PCI Express Transmitter testing RefClk was externally generated by an on-board oscillator on the PCISIG, PCIe CBB Compliance Board
- PCI Express Receiver and PLL testing RefClk were externally generated by a signal generator and connected through SMAs

The characterization was performed in accordance with PCI Express CEM specification that requires the add-in card be plugged into the PCISIG PCI Express compliance baseboard (CBB2) to perform PCIe measurements. The PCI Express CEM compliant test setup consists of a necessary compliance channel (Edge Finger Connector of an add-in card with 2" to 3" of trace to the silicon device, the PCI Express connector itself, and 2.5" to 3" of trace to the SMP connector). Device electrical tests were conducted on the signal integrity board, which has high-speed SMP connectors for bringing signals on and off the board. To build a necessary PCIe compliance channel per the PCIe CEM specification with the signal integrity board, a special setup was assembled. The setup uses the PCISIG compliance load board (CLB2) mated with a compliance baseboard (CBB2). This setup closely matches the correct PCIe channel as it is present between the device under test on the signal integrity board and the test equipment.

Testing was also conducted with the PCIe validation board. In this setup, the CBB provides the physical means to connect the validation board to the test equipment and provides the required PCIe add-in card channel. This test setup was used to provide a test platform at the PCISIG compliance workshop.

2.5.1 Electrical Testing Equipment/Software

- Agilent DSA91304A, 13GHz Real Time Scope or DSO93204A 32Ghz Real Time Scope
  - Agilent N5393C PCI Express Automation Test Application, Version 02.24 or newer
  - PCIe SIGTST 3.1.9 or newer
- BitifEye N5990A Test Automation Software Platform
  - PCI Express2 Application, Version 1.11.20101207 or newer
- Agilent J-BERT N4903B with A02 Option License

- Agilent N4916A De-Emphasis Signal Converter
- Agilent N6701A Power Supply Mainframe
  - Four individually controlled P/S Modules
- BertScope CR12500A, Clock Recovery Module and PLL Bandwidth S/W Application
- Silicon Thermal, Temperature Control Unit
  - Silicon Thermal Chiller CH400
  - Silicon Thermal Linear Power Supply PS190-L
  - Silicon Thermal Temperature Controller LB190-L
  - Silicon Thermal Head Adapter
- SMA-to-SMA cables
- SMA-to-SMP cables
- PCISIG, Compliance Base Board2 (CBB2) Fixture
- PCISIG, Compliance Load Board2 (CLB2) Fixture

2.5.2 Electrical Testing Environment

Device electrical testing was conducted by Microsemi using variations on power supply voltages and temperatures. Minimum voltage (Vmin) and maximum voltage (Vmax) were varied by +/–5% of the typical voltage (Vtyp) supply for the supplies related to the PCIe blocks of the device. The devices were also tested at the industrial temperature limits (–40°C to +125°C).

2.5.3 Testing Conditions

Table 2 • **Voltage and Temperature Matrix**

Voltage Dependencies	1.2 V VDD Device Range
CCC_xyz_PLL_VDDA	2.375 V 2.625 V
SERDES_x_PLL_VDDA	2.375 V 2.625 V
SERDES_x_L[0:3]VDDAPLL	2.375 V 2.625 V
SERDES_x_L[0:3]VDDAIO	1.14 V 1.26 V
SERDES_x_VDD	1.14 V 1.26 V
VDD (Core Supply)	1.14 V 1.26 V
Temperature	–55 °C –55 °C
	25 °C 25 °C
	125 °C 125 °C

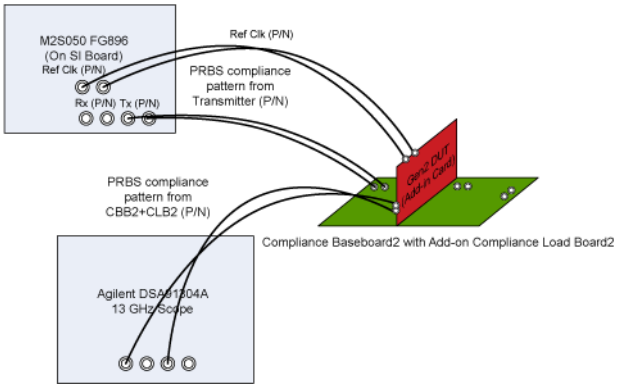
2.5.4 Transmit Compliance Testing

2.5.4.1 PCI Express Transmitter Setup

The PCIe specification requires a transmitter to send a defined compliance pattern. This compliance pattern is continually sent when not connected to a link partner, because an exit response from electrical idle is never detected. See the PCI Express specification for full details on the electrical compliance pattern. With this pattern, a series of tests are conducted to analyze the quality of the transmitter data eye. The testing produces direct and indirect measured data that is correlated to the PCIe specifications. For more information, see PCI EXPRESS ARCHITECTURE PHY TEST SPECIFICATION, REV. 2.0 for detailed procedures.

These specification documents are only available to PCISIG members at http://www.pcisig.com/specifications/pciexpress.

Figure 3 • **Transmitter Test Setup**



2.5.4.2 Results

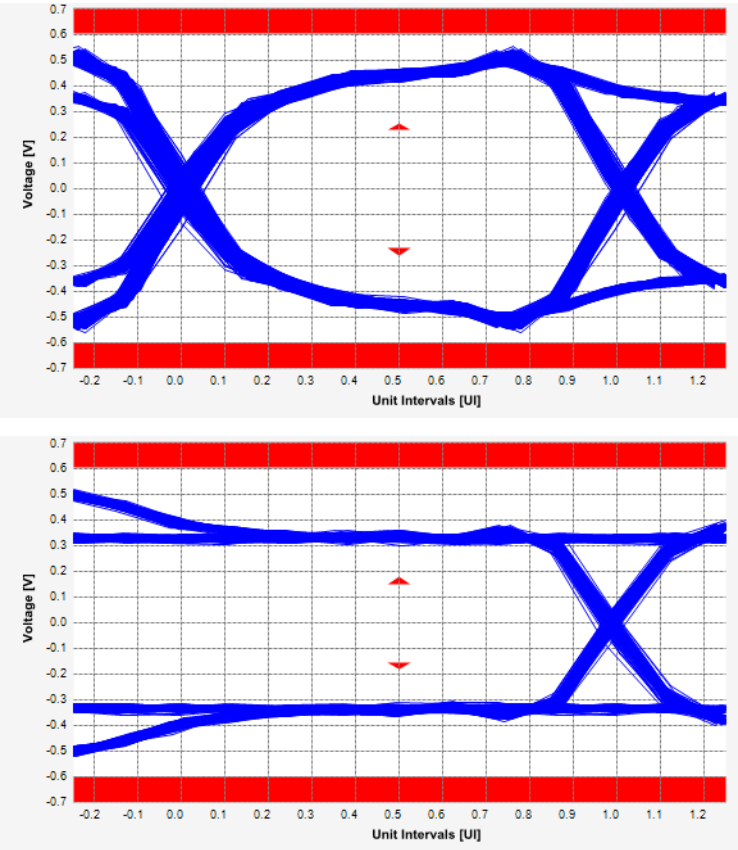
Table 3 • **Transmitter Compliance Test Results - Gen 1**

Tx Compliance test parameters	–55 Vmax	–55 Vmin	25 Vmax	25 Vmin	125 Vmax	125 Vmin	Units	Spec
Add-in Card Tx, Eye-Width (PCIE 2.0, 2.5 GT/s)	299.71	308.21	347.84	344.8	350.2	331.58	ps	VALUE >= 287.00
Add-in Card Tx, Median to Max Jitter (PCIE 2.0, 2.5 GT/s)	38.77	35.62	24.28	24.69	22.27	29.78	ps	VALUE <= 56.50
Add-in Card Tx, Peak Differential Output Voltage (NonTransition)(PCIE 2.0, 2.5 GT/s)	696.7	611.7	676.3	600.5	657.6	573.7	mV	360.0 mV <= VALUE <= 1.2000 V

Table 3 • **Transmitter Compliance Test Results - Gen 1 *(continued)***

Add-in Card Tx, Peak Differential Output Voltage (Transition)(PCIE 2.0, 2.5 GT/s)	962.4	822.2	939.7	797.8	886.2	758.2	mV	514.0 mV <= VALUE <= 1.2000 V
Add-in Card Tx, Unit Interval (PCIE 2.0, 2.5 GT/s)	400.019	400.016	400.01	400.011	400.011	400.013	ps	399.8800 <= VALUE <= 400.1200

Figure 4 • **Transmitter Eye Diagrams**



2.5.5 PLL Loop Bandwidth Testing

PLL bandwidth and peaking parameters are specified for 2.5. The Rx jitter for 2.5Gbps is inherently defined within the minimum eye width. The range specifies the allowable random and deterministic jitter components. The PLL bandwidth when measured with compliance pattern must be between 5 and 16 MHz if the peaking is less than 1 dB or must be between 8 and 16 MHz with a peaking of less than 3 dB. For 2.5 Gbps, the 3 dB point must fall between 1.5 and 22 MHz with peaking less than 3 dB.

2.5.5.1 PCI Express PLL Bandwidth Setup

The same PCI Express CEM Compliance Channel is applied to PCI Express PLL Bandwidth testing. The Ref CLK+/- is provided by the Tektronix CR125 Clock Recovery unit, and PCIe TX+/– lanes passing through both boards are connected to DATA_IN+/– of the CR125 unit. The CR125 DATA_OUT+/– must be terminated with 50 Ù terminators for RT4G150-FC1152 silicon to begin transmitting PCI Express Compliance Patterns upon power-up.

Figure 5 • **PLL Bandwidth Test Setup**

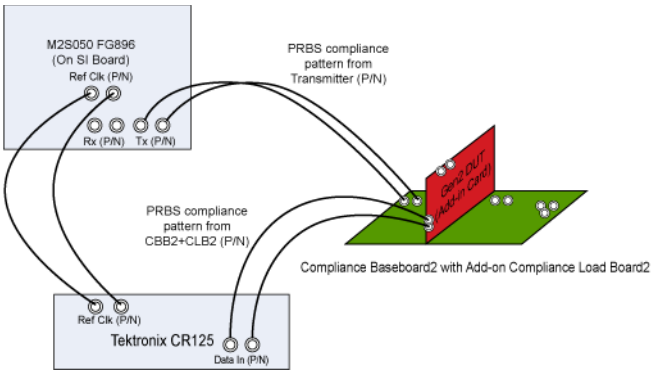


Table 4 • **PLL Bandwidth Specifications**

Category	Bandwidth Spec	Peaking Spec
PLL Bandwidth Gen 1	1.5 to 22 MHz	< 3.0 dB

Table 5 • **PLL Bandwidth Testing Results**

	–55		–55		–55		–55		25		-55		25		–55		125		125		125		125	
	Vmax		Vmax		Vmin		Vmin		Vmax		Vmax		Vmin		Vmin		Vmax		Vmax		Vmin		Vmin	
Test Corner / Device	PII loop bandwidth (MHz)	peaking (dB)	PII loop bandwidth (MHz)	peaking (dB)	PII loop bandwidth (MHz)	peaking (dB)	PII loop bandwidth (MHz)	peaking (dB)	PII loop bandwidth (MHz)	peaking (dB)	PII loop bandwidth (MHz)	peaking (dB)	PII loop bandwidth (MHz)	peaking (dB)	PII loop bandwidth (MHz)	peaking (dB)	PII loop bandwidth (MHz)	peaking (dB)	PII loop bandwidth (MHz)	peaking (dB)	PII loop bandwidth (MHz)	peaking (dB)	PII loop bandwidth (MHz)	peaking (dB)
Gen 1	13.36	0.29	12.02	0.34	13.43	0.33	11.79	0.21	12.79	0.21	12.55	0.3	13.09	0.3	12.48	0.36	11.88	0.39	11.63	0.25	12.07	0.32	11.74	0.24

2.5.6 PCI Express Receiver Testing

Receiver testing stresses the incoming signal to determine its robustness to operate in typical system environments with a degree of noise and signal fluctuations. The test setup impairs the signal to the receiver by adding jitter, and determines that it can run normally with a long-term bit error rate target of 10-12.

2.5.6.1 PCI Express Receiver Setup

The same PCI Express CEM Compliance Channel setup is used for the PCI Express Receiver testing. The JBERT and De-emphasis Box are interconnected together to provide a necessary generator for the PCI Express Receiver testing. The entire PCI Express CEM setup with an additional 7" of trace is calibrated to provide PCI Express Compliant Stressed Eye at the RX package balls of the RT4G150-FC1152 silicon under test. A 12 MHz CDR bandwidth was used to test the PCI Express Receiver Jitter Tolerance testing. The test equipment stresses the receiver by imposing sinusoidal noise, and monitors the bit error rate of the system.

Figure 6 • **Receiver Test Setup**

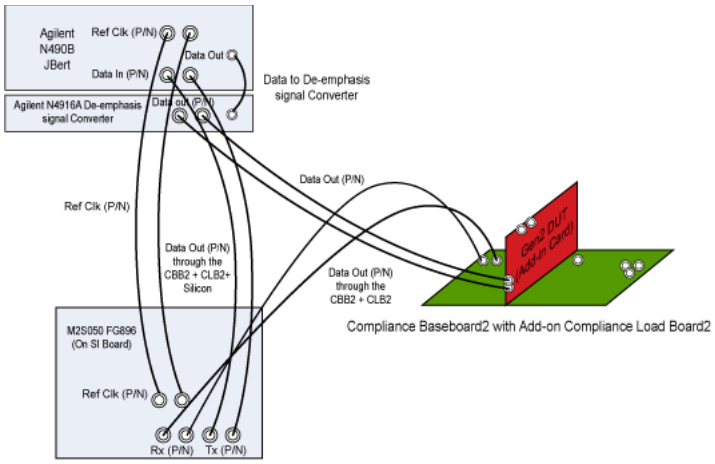
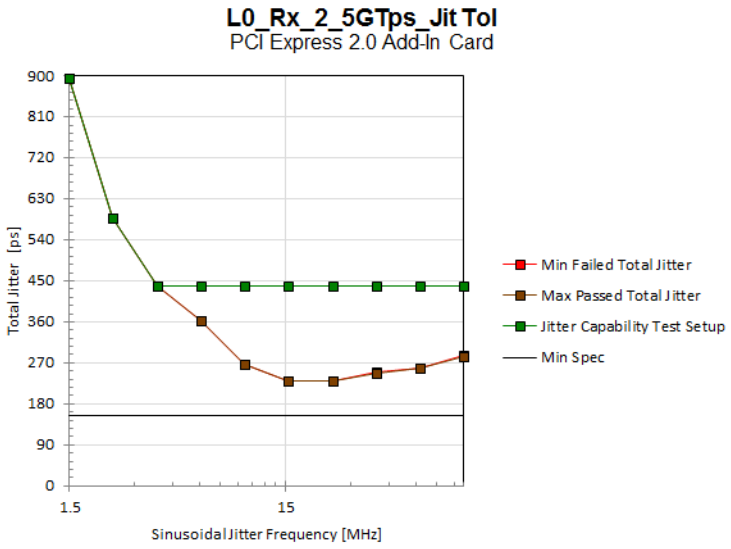


Table 6 • **RX JTOL Compliance Tests (GEN1)**

Conditions	125 °C Vmin	25 °C Vmin	-55 °C Vmin	125 °C Vmax	25 °C Vmax	-55 °C Vmax
BER Results	> 1e – 13	> 1e – 13	> 1e – 13	> 1e – 13	> 1e – 13	> 1e – 13

Figure 7 • **Typical Receiver Tolerance Test Plot**



Specification:

Total Jitter (peak - peak) >= 154.0 ps

Table 7 • **Jitter Test Properties**

Parameter	Value
Offline	False
Eye Height	238 mV
Frequency Mode	Equally Spaced Frequencies

Table 7 • **Jitter Test Properties *(continued)***

Frequency Scale	Logarithmic
Start Frequency	1.5 MHz
Stop Frequency	100 MHz
Number of Frequency Steps	10
Search algorithm	HysteresisUp
Jitter Step Size	2 ps
Show Min Failed Points	True
Random Jitter	5.4 ps
BER Mode	TargetBer
Target BER	1E – 9
Confidence Level	95%
Force retraining on each frequency	False
Link Training Lane Number	0
Data Rate Deviation	0 ppm
Link Training Mode	JBERT Link Training
Link Training Suite Settings File	C:\ProgramData\BitifEye\ValiFrame\Settings\PCI Express3\Pcie1_25G_M8020A_Loopback.txt
Default Link Training Lane Number for every Lane	Auto
Suppress Loopback Training Messages	False
Use CDR	True
CDR Loop Bandwidth	3.75 MHz
Peaking	1 dB
Sensitivity	Normal
Relax Time	1 s
Jitter Unit	Time

Table 8 • **Jitter Results**

Result	Sinusoidal Jitter Frequency (MHz)	Min Failed Total Jitter (ps)	Max Passed Total Jitter (ps)	Jitter Capability Test Setup (ps)	Min Spec (ps)	Margin (%)
pass	1.500	893.60	893.60	893.60	154.00	480.3
pass	2.392	588.60	588.60	588.60	154.00	282.2
pass	3.814	437.60	437.60	437.60	154.00	184.2
pass	6.082	363.60	361.60	437.60	154.00	134.8
pass	9.699	267.60	265.60	437.60	154.00	72.5

Table 8 • **Jitter Results *(continued)***

pass	15.466	231.60	229.60	437.60	154.00	49.1
pass	24.662	231.60	229.60	437.60	154.00	49.1
pass	39.327	249.60	247.60	437.60	154.00	60.8
pass	62.711	259.60	257.60	437.60	154.00	67.3
pass	100.000	285.60	283.60	437.60	154.00	84.2

2.6 Configuration (CV) Testing

2.6.1 Description of Test

PCIe CV requires installation of software provided to members of the PCISIG group. The testing involves installation of the PCIe validation board into a PCIe slot on a host PC with the testing software installed. The PCIe validation board requires a separate power supply from the PC PCIe slot. The standalone testing exercises all specific testing as required by the PCISIG configuration verification specification.Refer to PCIECV 2.0 Configuration User Guide (2/25/2013). For more information about the test procedure, see Appendix: PCIe Compliance Test Procedures, page 15.

Note: These specification documents are only available to PCISIG members at: http://www.pcisig.com/specifications/pciexpress.

2.6.1.1 Results

Example Configuration Testing

INFO PCIECVApp.exe ver 1.5.1.9

INFO DriverInterfaceDLL.dll ver 1.4.7.0

INFO ttpi.dll ver 1.4.9.0

INFO Max Bus Number value: 50

INFO Beginning PCIECV Test.

INFO TEST OPTION SELECTED: Test against either 1.1 or 2.0 Spec

INFO Virtual Function Detection Disabled.

INFO Test End Point was Selected.

INFO Device selected: Vendor ID= 11aa, Device ID= 11aa

Bus number= 0002, Device Number= 0000, Function= 0000

INFO Hot Reset (Secondary Bus Reset) chosen as the reset type.

INFO Running the test at the maximum supported speed.

INFO Run All Tests Selected

INFO Link Width chosen:x1.

INFO Test Summary

Total Number of Tests Run: 26

Number of Tests Passed: 26

Number of Tests Failed: 0

2.7 PTC Testing

2.7.1 Description of Test

The PCIe validation board is installed and connected to the Agilent PTC2 (E2969B) exerciser. The PTC2 and the PCIe validation board require separate power supplies. The PTC2 is connected by the USB port to the controller PC, which has the PTC software installed. The card must be in PTC mode to perform the correct add-in tests on the PCIe validation board. For more information about the test procedure, see Appendix: PCIe Compliance Test Procedures, page 15.

This section includes example screen shots of the PTC test results.

Figure 8 • **Gen 1 Agilent PTC Results**

Name	Description	Result
DLL_04_01_02	To check that receiver ignores the reserved fields of the received DLLPs (ReservedFieldsDLLPReceive).	Passed.
DLL_05_02_01	To check that the link transmitter starts REPLAY after receiving a Nak (ReplayNumTest,ReplayTimerTest,ReXmitOnNak).	Passed.
DLL_05_02_02	To check that if REPLAY_NUM overflows, link retraining is triggered (LinkRetrainOnRetryFail,LinkRetrainOnRetryFailNoAckNack)	Passed.
DLL_05_02_07	To check that the retry buffer does not changes in link retraining	Passed.
DLL_05_02_10	To check that the oldest unacknowledged TLP is sent first.	Passed.
DLL_05_02_15	To check that corrupt DLLPs are discarded (Corrupted DLLPs)	Passed.
DLL_05_02_16	To check that a DLLP with undefined encodings is dropped silently (UndefinedDLLPEncoding)	Passed.
DLL_05_02_17	To check that an Ack with unknown sequence number is reported as FATAL_ERROR (WrongSeqNumInAckDLLP).	Passed.
DLL_05_03_02	To check for wrong LCRC detection (BadLCRC).	Passed.
DLL_05_03_03	To check that a TLP with wrong sequence number is discarded, and any associated storage is freed (DuplicateTLPSeqNum)	Passed.
LINKUPCONFIG	To check for correct linkup behavior.	Passed.
TDTRANS11_2_REQCOMPL_NOAER1	To test UR handling in devices that do not implement AER.	Passed.
TDTRANS11_3_REQCOMPL_AER1	To test UR handling in devices that implement AER.	Passed.
TDTRANS11_4_REQCOMPL_AER2	To test UR handling in devices that implement AER.	Passed.
TDTRANS11_5_REQCOMPL_NOAER1	To test UR handling in devices that do not implement AER.	Passed.
BadLCRC	To check handling TLPs with bad CRC	Passed.
CorruptedDLLPs	To check handling DLLPs with bad CRC	Passed.
DuplicateTLPSeqNum	To check handling duplicate TLPs	Passed.
LinkRetrainOnRetryFail	To check link retraining after replay	Passed.
LinkRetrainOnRetryFailNoAckNack	To check link retraining after replay	Passed.
ReplayNumTest	To check replaying transactions	Passed.
ReplayTimerTest	To check the replay timer	Passed.
ReplayTLPOrder	To check for correct TLP replay order	Passed.
ReservedFieldsDLLPReceive	To check reserved fields in an ACK DLLP	Passed.
ReXmitOnNak	To check retransmission of NAKed transaction	Passed.
UndefinedDLLPEncoding	To check that DLLPs with undefined encoding are silently dropped	Passed.
WrongSeqNumInAckDLLP	To check that ACK DLLPs with invalid sequence number are dropped	Passed.
RequestCompletion11	To check Basic Request and Completion handling	Passed.

2.8 Conclusion

The test results demonstrate that the capabilities of the RTG4 PCIe solution systems require high reliability devices to be robust. This report provides a baseline summary of the thorough testing performed by Microsemi to assure users that the device meets the performance and functional requirements in their customized PCI Express system.

3 Appendix: PCIe Compliance Test Procedures

This section describes the PCIeCV and PTC-2 test procedures.

3.1 Configuration (PCIeCV) Test

1. Power down the RTG4 end point board and shut down the host PC.
2. Connect the RTG4 end point edge connector to the host PC directly or via a PCIe extension cable.
3. Power up the end point board and then Power up the host PC.
4. Wait for the PC to boot up and to load operating system.
5. See the enumeration of the end point in the **Device Manager**.
   If successful enumeration is not seen, then start from step 1.
6. Close **Device Manager** and start the PCIeCV application.
7. Select the appropriate test options in the application according to the device configuration and click **run all tests**.
8. Click **Exit**.
9. Save the log files for future reference from the Logs folder in the PCIeCV installation directory.
10. Shut down the PC before powering down the end point board.

3.2 PTC-2 Test

1. Power down the RTG4 end point board and host Exerciser capable of running the PTC-2 tests from a vendor such as Keysight and Teledyne Lecroy.
2. Connect the RTG4 end point edge connector to the back plane of the Exerciser either directly or via a PCIe extension cable.
3. Power up the end point board and then power up the back plane and the Exerciser.
4. Once the Exerciser powers up, start the Agilent Protocol Suite/Teledyne PCIe protocol suite software in the host PC that is connected to the Exerciser.
5. The software prompts the user to select a new session and then connects to the Exerciser hardware. Once connected, the user can now run all the PCIe protocol compliance tests on that end point
6. In the **Settings** tab, change the supported data rate to 2.5 GT/s and click **Apply** to confirm the changes.
7. In the **Protocol Tests** tab, select all the tests and click the **Play** button on the menu bar to start the tests.
8. Once all the tests finish, a HTML report is generated, which can be saved to a file.
9. Power down the RTG4 end point board and detach from the Exerciser back plane.