TU0565
Tutorial
Low Power RTG4 FPGA - Libero SoC v11.9 SP1
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1 Revision History

The revision history describes the changes that were implemented in the document. The changes are listed by revision, starting with the most current publication.

1.1 Revision 2.0
Updated the document for Libero SoC v11.9 SP1.

1.2 Revision 1.0
The first publication of this document.
2 Low Power RTG4 FPGA

RTG4™ FPGAs are designed to meet the need of low power. RTG4 devices exhibit lower power consumption in static and dynamic modes. The static mode is achieved by powering-down the fabric CCC. This tutorial describes how to:

• Measure the total dynamic power using Microsemi Power Estimator and SmartPower.
• Measure the total dynamic power on the board.
• Measure the total static power using Power Estimator and SmartPower.
• Measure the total static power on the board.

The following functionalities are described in the subsequent sections:

• Creating a New Project Using Libero® SoC
• Creating the SmartDesign
• Importing and Deriving Constraint Files
• Generating Power Report using Smart Power Tool
• Obtaining Resource Utilization Report
• Generating the Programming File and Programming the Board
• Measuring On-Board Power
• Measuring the Low Power Using Power Estimator Tool

2.1 Design Requirements

The following table lists the design requirements to run the low power RTG4 FPGAs tutorial.

Table 1 • Design Requirements

<table>
<thead>
<tr>
<th>Design Requirements</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Hardware Requirements</strong></td>
<td></td>
</tr>
<tr>
<td>RTG4 FPGA Development Kit:</td>
<td>Rev B or later</td>
</tr>
<tr>
<td>12 V adapter</td>
<td></td>
</tr>
<tr>
<td>USB A to mini-B cable</td>
<td></td>
</tr>
<tr>
<td>Host PC or laptop</td>
<td>Windows 64-bit Operating System</td>
</tr>
<tr>
<td>Multimeter/DVM</td>
<td>Any</td>
</tr>
<tr>
<td><strong>Software Requirements</strong></td>
<td></td>
</tr>
<tr>
<td>Libero SoC</td>
<td>v11.9 SP1</td>
</tr>
<tr>
<td>FlashPro Programming Software</td>
<td>v11.9 SP1</td>
</tr>
</tbody>
</table>

2.2 Prerequisites

1. Download and extract the design files from the following link: [http://soc.microsemi.com/download/rsc/?f=rt4g_tu0565_lowpower_liberov11p9sp1_df](http://soc.microsemi.com/download/rsc/?f=rt4g_tu0565_lowpower_liberov11p9sp1_df)
   The design file consists of Libero SoC project, VHDL files, RTG4 power estimator, and programming files (*.stp). Refer to the Readme.txt file included in the design file for the directory structure and description.

2. Connect the power supply cable to the J9 connector on the board.
3. Connect the USB A to mini B cable to J47 connector on the board.
4. Connect the jumpers to the RTG4 Evaluation Kit board, as listed in the following table.

<table>
<thead>
<tr>
<th>Table 2 • Jumper Settings</th>
</tr>
</thead>
<tbody>
<tr>
<td>Jumper</td>
</tr>
<tr>
<td>J16</td>
</tr>
<tr>
<td>J17</td>
</tr>
<tr>
<td>J19</td>
</tr>
<tr>
<td>J21</td>
</tr>
<tr>
<td>J23</td>
</tr>
<tr>
<td>J26</td>
</tr>
<tr>
<td>J27</td>
</tr>
<tr>
<td>J28</td>
</tr>
<tr>
<td>J32</td>
</tr>
<tr>
<td>J33</td>
</tr>
<tr>
<td></td>
</tr>
</tbody>
</table>

### 2.3 Demo Design

The low power design file consists of a 50 MHz oscillator, a fabric CCC (FCCC), and a fabric logic block. The FCCC is configured to provide a 80 MHz clock to the fabric logic. The 50 MHz oscillator is the reference clock source for FCCC. The lock signal is used as the reset signal to the fabric logic. The fabric logic has 4464 stages of 8-bit loadable up-counters, 252 stages of 16-bit shift registers, 55 LSRAM blocks, 56 μSRAM blocks, and 42 math blocks. It also has an LED driver block, which is connected to a set of LEDs to monitor the state of the fabric while entering and exiting low power mode.

The following figure illustrates the block diagram of the design.

**Figure 1 • Design Block Diagram**
2.3.1 Introduction

The demo design files are available at
http://soc.microsemi.com/download/rsc/?f=rtg4_low_power_liberov11p9sp1_df

The demo design includes:

- Libero
- Programming files
- Source files
- Readme file

The following figure illustrates the top-level structure of the design files. For further details, refer to the Readme.txt file.

Figure 2 • Design Files Top-Level Structure

2.3.2 Extracting the Design Files

Extract the rtg4_low_power_liberov11p9sp1_df.rar file to the <C:\ or D:\>Microsemi_prj folder in the local system. Verify that all files are in the directory as mentioned in the Readme.txt file.
2.4 Creating a New Project Using Libero SoC

This section describes how to create a new project using Libero SoC.

1. Go to Start > Programs > Microsemi > Libero SoC v11.9 SP1 > Libero SoC v11.9 SP1. The Libero SoC Project Manager window is displayed, as shown in the following figure.

Figure 3 • Libero SoC Project Manager

2. Create a new project using one of the following options:
   • Click New... in the Projects panel on the Start Page.
   • In the Libero SoC menu, go to Project > New Project.

The New Project-Project Details window is displayed, as shown in the following figure.
3. Enter the following information in the **New Project - Project Details** window.
   - **Project name**: RTG4_Standby
   - **Project location**: <C:\ or D:\>Microsemi_prj\RTG4_Low_Power_tutorial
   - **Preferred HDL type**: VHDL
   - **Enable block creation**: Not selected

**Figure 4 • New Project - Project Details**

4. Click **Next**. The **New Project - Device Selection** window is displayed.
5. Select the following values from the drop-down lists under **Part filters**.
   - **Family**: RTG4
   - **Die**: RT4G150
   - **Package**: 1657 CG
   - **Speed**: STD
   - **Core voltage**: 1.2
   - **Range**: MIL

**Figure 5 • New Project - Device Selection**

6. Select the **RT4G150-CG1657M** device from the list and the associated supported details for various features are listed in the respective columns.

7. Click **Finish**. The **New Project Information** window is displayed.
8. Click **Use Enhanced Constraint Flow** in the **New Project Information** window. The **Design Flow** window is displayed.

**Figure 6 • New Project Information**

![New Project Information](image)

2.5 **Creating the SmartDesign**

This section describes how to create SmartDesign and generate the SmartDesign component.

1. In the **Design Flow** window, expand **Create Design**, as shown in the following figure.
2. Right-click **Create SmartDesign** and click Run. The **Create New SmartDesign** dialog box is displayed.

**Figure 7 • Creating SmartDesign**

![Creating SmartDesign](image)
3. Enter the **Name** as **RTG4_Standby** and click **OK**. A new SmartDesign canvas is displayed.

*Figure 8 • Creating New SmartDesign*

![Creating New SmartDesign](image)

Now you can add different macros and IP cores to the SmartDesign canvas as required for your design.

4. Click the **Catalog** tab and expand **Clock & Management** to add an RTG4 CCC to the canvas, as shown in the following figure.

*Figure 9 • Clock and Management*

![Clock and Management](image)

5. Drag and drop the **RTG4 Clock Conditioning Circuit (CCC)** to the SmartDesign canvas.
6. Double-click the **RTG4 Clock Conditioning Circuit (CCC)** component in the SmartDesign canvas. The **RTG4 CCC Configurator** window is displayed, as shown in the following figure.

**Figure 10 • Configuring Fabric CCC**

![Configuring Fabric CCC](image)

**Note:** This design uses an FCCC to generate a 80 MHz internal clock for the fabric. The FCCC reference clock is the 50 MHz oscillator.
7. Click the **PLL Options** tab, select the **Expose PLL_ARST_N and PLL_POWERDOWN_N signals** check box, as shown in the following figure.

*Figure 11 • Configuring PLL Power-Down Signals*

8. Click **OK**.
9. Click the **IP Catalog** tab and expand **Macro Library** and select the **RCOSC_50MHZ** macro, which is the 50 MHz oscillator macro.
10. Drag and drop the **RCOSC_50MHZ** component to the SmartDesign canvas.
11. Right-click **Create HDL** under **Create Design** in the **Design Flow** tab and click **Import File...** to import the source files for the user fabric logic, as shown in the following figure.

*Figure 12 • Importing HDL Source Files*
12. Browse to `<Download folder> \RTG4_Low_Power_tutorial\Source_files\VHDL` and select all the VHDL files available in the folder, and click Open. The files are listed in the Design Hierarchy tab, as shown in the following figure.

*Figure 13* • Listing the Imported Files in the Design Hierarchy Tab

![Design Hierarchy](image)

13. Drag and drop the **Fabric Logic** and the reset_synchronizer_0 component from Design Hierarchy into the **SmartDesign** canvas, as shown in the following figure.

*Figure 14* • Adding Components into SmartDesign Canvas

![SmartDesign Canvas](image)
2.5.1 Connecting Components and Generating SmartDesign

The SmartDesign tool in Libero SoC has a connection mode that allows components to be connected using a drag and drop mechanism.

To connect the components:

1. Switch to connection mode in SmartDesign by clicking Connection Mode option in toolbar, as shown in the following figure.

![Figure 15 • SmartDesign Canvas Connection Mode](image)

2. To connect ports in the SmartDesign canvas, drag and drop the CLKOUT of the RCOSC_50MHZ_0 component to the RCOSC_50MHZ port of the RTG4FCCC_0 component. You can also connect the ports by selecting the ports while holding down the Ctrl key on your keyboard, right-clicking any of the selected ports, and click Connect.

3. Connect other components in the SmartDesign canvas as listed in the following table.

<table>
<thead>
<tr>
<th>From</th>
<th>To</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTG4FCCC_0: PLL_POWERDOWN_N</td>
<td>RTG4FCCC_0: PLL_ARST_N</td>
</tr>
<tr>
<td>RTG4FCCC_0: GL0</td>
<td>Fabric_Logic_0: CLK</td>
</tr>
<tr>
<td>RTG4FCCC_0: LOCK</td>
<td>Fabric_Logic_0: RST</td>
</tr>
<tr>
<td>RTG4FCCC_0:GL0</td>
<td>reset_synchronizer_0:clock</td>
</tr>
<tr>
<td>RTG4FCCC_0:LOCK</td>
<td>reset_synchronizer_0:reset</td>
</tr>
<tr>
<td>reset_synchronizer_0:reset_sync</td>
<td>Fabric_Logic_0:LD</td>
</tr>
</tbody>
</table>

4. To exit from Connection Mode, disable the Release Connection mode by clicking the button in SmartDesign canvas.

5. Right-click any of the following ports and click Promote to Top Level to promote the ports:
   - RTG4FCCC_0: PLL_POWERDOWN_N
   - Fabric_Logic_0: LD
   - Fabric_Logic_0: DIN[15:0]
   - Fabric_Logic_0: DOUT[15:0]
   - Fabric_Logic_0: LED_1
   - Fabric_Logic_0: LED_2
   - Fabric_Logic_0: LED_3
   - Fabric_Logic_0: LED_4

The SmartDesign canvas appears as shown in the following figure.
6. Drag and drop the components to the required location or right-click the Auto Arrange icon on the toolbar to improve the appearance of the canvas.

**Figure 16 • SmartDesign Canvas**

7. Go to File > Save RTG4_Standby to save the design.
8. Generate the design by selecting SmartDesign > Generate Component. A message appears in the Libero log window, confirming the successful generation of the low power RTG4 FPGAs design.
9. Go to File > Close RTG4_Standby to close the design.

### 2.6 Importing and Deriving Constraint Files

This section describes how to import a physical design constraint (PDC) file to assign I/O attributes and pins for the layout and how to derive timing constraints to meet the timing requirements.

1. In the Design Flow tab, expand Constraints and click Manage Constraints, as shown in the following figure. The Constraint Manager window is displayed.

**Figure 17 • Manage Constraints**

2. In the Constraint Manager window, click the I/O Attributes tab and click Import to import the *.PDC file, as shown in the following figure.

**Figure 18 • Import Constraints**

3. Select the Place and Route checkbox to use the imported PDC file during place and route.
4. Browse to the location <Download folder>RTG4_Low_Power_tutorial\Source_files in your local system, select the user.pdc file, and click Open. The PDC file is imported for this design.

5. Click the Timing tab and click Derive Constrains, as shown in the following figure.

**Figure 20 • Derive Constraints**

6. Press Yes, when asked to associate the derived constraints (*.SDC) files to Synthesis; place and route; timing; and verification tools. The timing constrains are derived for the design.

8. Run Place and Route from Libero Design flow.

### 2.7 Generating Resource Utilization Report

This section describes how to generate the resource utilization report for the design. Resource utilization report shows the used resources out of total resources available in this design.

1. Click Design from the menu bar and click Reports, as shown in the following figure. The Project Reports window is displayed.

**Figure 21 • Opening Reports**

2. Click RTG4_Standby_compile_netlist_resources.xml under Synthesize, as shown in the following figure.

**Figure 22 • Resource Utilization Report**
The Resource Usage report shows the strategies of Type, Used, Total, and Percentage.

Figure 23 • Resource Usage

<table>
<thead>
<tr>
<th>Type</th>
<th>Used</th>
<th>Total</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>4LUT</td>
<td>85957</td>
<td>151824</td>
<td>56.62</td>
</tr>
<tr>
<td>OFF</td>
<td>81031</td>
<td>151824</td>
<td>53.37</td>
</tr>
<tr>
<td>I/O Register</td>
<td>0</td>
<td>2160</td>
<td>0.00</td>
</tr>
<tr>
<td>User I/O</td>
<td>720</td>
<td>720</td>
<td>5.28</td>
</tr>
<tr>
<td>– Single-ended I/O</td>
<td>38</td>
<td>720</td>
<td>5.28</td>
</tr>
<tr>
<td>– Differential I/O Pairs</td>
<td>0</td>
<td>380</td>
<td>0.00</td>
</tr>
<tr>
<td>RAM64x18</td>
<td>565</td>
<td>210</td>
<td>26.67</td>
</tr>
<tr>
<td>RAM1K18</td>
<td>55</td>
<td>209</td>
<td>26.32</td>
</tr>
<tr>
<td>MACC</td>
<td>42</td>
<td>452</td>
<td>9.09</td>
</tr>
<tr>
<td>H-Chip Global</td>
<td>4</td>
<td>48</td>
<td>8.33</td>
</tr>
<tr>
<td>CCC</td>
<td>1</td>
<td>8</td>
<td>12.50</td>
</tr>
<tr>
<td>RCOSC_50MHZ</td>
<td>1</td>
<td>1</td>
<td>100.00</td>
</tr>
<tr>
<td>SERDESIF Blocks</td>
<td>0</td>
<td>6</td>
<td>0.00</td>
</tr>
<tr>
<td>FDDR</td>
<td>0</td>
<td>2</td>
<td>0.00</td>
</tr>
<tr>
<td>GRESET</td>
<td>1</td>
<td>1</td>
<td>100.00</td>
</tr>
</tbody>
</table>

Figure 24 • I/O Resource Usage

<table>
<thead>
<tr>
<th>I/O Function</th>
<th>w/o register</th>
<th>w/ register</th>
<th>w/ DDR register</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input I/O</td>
<td>18</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Output I/O</td>
<td>20</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Bidirectional I/O</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Differential Input I/O Pairs</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>Differential Output I/O Pairs</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Note: These values must be entered in the Power Estimator Excel sheet to measure the total power.

2.8 Generating Power Report Using Smart Power Tool

This section describes how to generate the power report for the design. Power report includes total power, static power, dynamic power, and power breakdown by rail, by clock, and by type.

- On the Design Flow tab, expand Implement Design, right-click Verify Power and select Run, as shown in the following figure. It runs Synthesize and Place and Route.

Figure 25 • Power Report
The following figure shows a sample generated power report.

**Figure 26 • Generated Power Report**

<table>
<thead>
<tr>
<th>Power Summary</th>
<th>Power (mW)</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Power</td>
<td>2470.850</td>
<td>100.0%</td>
</tr>
<tr>
<td>Static Power</td>
<td>203.220</td>
<td>8.1%</td>
</tr>
<tr>
<td>Dynamic Power</td>
<td>2270.610</td>
<td>91.9%</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Breakdown by Rail</th>
<th>Power (mW)</th>
<th>Voltage (V)</th>
<th>Current (mA)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rail VDD</td>
<td>2422.855</td>
<td>1.200</td>
<td>2019.046</td>
</tr>
<tr>
<td>Rail VODI 2.5</td>
<td>31.474</td>
<td>2.500</td>
<td>12.550</td>
</tr>
<tr>
<td>Rail VDDPLL</td>
<td>13.200</td>
<td>3.300</td>
<td>4.000</td>
</tr>
<tr>
<td>Rail VPP</td>
<td>3.300</td>
<td>3.300</td>
<td>1.600</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Breakdown by Clock</th>
<th>Power (mW)</th>
<th>Percentage</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTG4FCCC_0/CCC_INST_INST_CCC_IP:GLO (clocks)</td>
<td>1262.977</td>
<td>55.9%</td>
</tr>
<tr>
<td>RTG4FCCC_0/CCC_INST_INST_CCC_IP:GLO (register outputs)</td>
<td>458.854</td>
<td>21.5%</td>
</tr>
<tr>
<td>RTG4FCCC_0/CCC_INST_INST_CCC_IP:GLO (primary inputs)</td>
<td>0.090</td>
<td>0.0%</td>
</tr>
<tr>
<td>RTG4FCCC_0/CCC_INST_INST_CCC_IP:GLO (combinational outputs)</td>
<td>508.631</td>
<td>22.5%</td>
</tr>
<tr>
<td>RCOSC_50MHZ_0/0:CLKOUT (clocks)</td>
<td>0.090</td>
<td>0.0%</td>
</tr>
<tr>
<td>RCOSC_50MHZ_0/0:CLKOUT (register outputs)</td>
<td>0.090</td>
<td>0.0%</td>
</tr>
</tbody>
</table>

## 2.9 Generating the Programming File and Programming the Board

This section describes how to generate the programming file for the design and how to program the RTG4 development kit board.

1. On the **Design Flow** tab in Libero SoC, expand **Program Design** and double-click **Generate Bitstream** to generate the programming file.
2. Board setup for running the demo on the RTG4 Development Kit board is shown in the following figure.

**Figure 27 • Board Setup**

3. Power-up the board by turning the power switch on.

Note: Do not interrupt the programming sequence. It may damage the device or programmer.
5. A green tick mark appears next to **Program Design** in the **Design Flow** tab, indicating that programming is completed successfully. The following message is displayed in the Reports, as shown in the following figure.

![Figure 28 • Final Report](image)

6. Save the project by selecting **Project > Save**.

7. Exit the Libero SoC by selecting **Project > Exit**.

### 2.10 Power Measurement

#### 2.10.1 On-Board Power Measurement

For applications that require current measurement, a high-precision operational amplifier circuitry (U5 with gain 5) is provided on the board to measure the output voltage at test point TP16.

The following steps describe how to measure the core power:

1. Measure the output voltage (V) at **TP16**.
2. Measure the core voltage (V) at **TP14**. Therefore, the consumed core power is calculated using the following formula: 
   \[ P = V \times V \times 4 \]
   Multimeter or DVM is used to measure output voltage and core voltage.
3. Connect the positive terminal of a standard digital voltmeter (DVM)/multimeter to **TP16** and the negative terminal to **TP8**. Note the digital voltmeter/multimeter reading.
4. Connect the positive terminal of a standard digital voltmeter (DVM)/multimeter to **TP14** and the negative terminal to **TP8**. Note the digital voltmeter/multimeter reading.
5. Calculate the power values using the equations.

#### 2.10.1.1 Total Core Power (Dynamic and Static)

To calculate total power:

1. Reset the board by pressing and releasing the **Reset** button (that is, **SW7 DEVRST**).
2. Observe the pattern of LEDs 1, 2, 3, and 4 after resetting the board.
3. If LEDs blink, measure the power else change the position of DIP slide switch (PIN: SW5-1, DIP switch) and measure the power.
2.10.1.2 Static Power

To calculate static power:

1. Observe the pattern of LEDs 1, 2, 3, and 4.
2. If LEDs blink, change the position of DIP slide switch (PIN: SW5-1, DIP switch).
3. Measure the power.

The following table lists the power measurements on the board:

<table>
<thead>
<tr>
<th>Measurement</th>
<th>V (TP16) (mV)</th>
<th>V (TP14) (mV)</th>
<th>Power (mW) = V(TP16) × V (TP14) × 4</th>
</tr>
</thead>
<tbody>
<tr>
<td>Total Power</td>
<td>542</td>
<td>1197</td>
<td>2595</td>
</tr>
<tr>
<td>Static Power</td>
<td>70</td>
<td>1202</td>
<td>336</td>
</tr>
</tbody>
</table>

2.10.2 Measuring Power Using Power Estimator Tool

The following steps describe how to use power estimator to calculate total power, dynamic power, and static power.

1. Download the **Power Estimator** spreadsheet and user guide from:
   - RTG4 Power Estimator
   - RTG4 Power Estimator User Guide
2. Or open the power estimator spreadsheet from `<Download folder>\Source_file\RTG4_power_calculator.xls` and go to the **Summary** worksheet that provides the device settings and power summary.
3. Reset the RTG4_power_calculator by pressing **Reset to Defaults**, as shown in the following figure.

![Reset to Defaults](image)

4. Change the device settings by selecting from the respective drop-down lists, as shown in the following figure:
   - **Device**: RT4G150
   - **Package**: 1657 CG
   - **Range**: Military
Refer to Generating Resource Utilization Report, page 15 for getting resource utilization for punching values to power estimator.

5. Click the Clock worksheet and enter the following information in the sheet.
   - Name: System
   - Clock Frequency (MHz): 80
   - Fanout: Number of DFF in the resource utilization report
   - Global Enable Rate: 100

6. Click the Logic worksheet and enter the following information in the sheet.
   - Name: System
   - Clock Frequency (MHz): 80
   - Number of Registers: Number of DFF in the resource utilization report
   - Number of LUTs: Number of LUTs in the resource utilization report
   - Fanout: 3
   - Toggle Rate: 12.5

7. Click the LSRAM worksheet and enter the following information in the sheet.
   - Name: System
   - Number of LSRAM Blocks: Number of LSRAM blocks in the resource utilization report
   - PORT A and B
     - Clock Frequency (MHz): 80
     - Write Rate: 12.5%
     - Enable Rate: 12.5%

8. Click the uSRAM worksheet and enter the following information in the sheet.
   - Name: System
   - Number of uSRAM Blocks: Number of uSRAM blocks in the resource utilization report
   - PORT A and B
     - Read Clock Frequency (MHz): 80
     - Enable Rate: 12.5%
   - PORT C
     - Write Clock Frequency (MHz): 80
     - Enable Rate: 12.5%

9. Click the Math Block worksheet and enter the following information in the sheet.
   - Name: System
   - Clock Frequency (MHz): 80
   - Number of Math Blocks: Number of math blocks in the resource utilization report
   - Data Toggle Rate: 12.5%

10. Click the I/O worksheet and enter the following information in the sheet.
    - Name: System
    - Bank Type: MSIO
    - I/O Standard: LVCMOS25
    - ODT: No ODT
    - Output Drive (mA): 2
    - Output Load (pF): 5
• Clock (MHz): 80
• Data Rate: Data
• Toggle Rate: 12.5%
• Output Enable: 50%

11. Click the CCC worksheet and enter the following information in the sheet.
   • Name: system
   • Reference Clock Frequency (MHz): 50
   • PLL Output Clock Frequency (MHz): 80
   • Output1 Frequency (MHz): 80

12. Click the Summary worksheet to get the total power. The Power Summary section is populated with the total power consumed during active mode, as shown in the following figure.

Figure 31 • Power Summary

The Modes and Scenarios section displays the total power in both active, as well as static modes as shown in the following figure.

Figure 32 • Modes and Scenarios


2.10.2.1 Summary of Power Measurement

Based on different methods of power measurement, the values of total power, dynamic, and static power are shown in the following table.

Table 5 • Summary of Power Measurement

<table>
<thead>
<tr>
<th>Power Measurement Method</th>
<th>Total Power (mw)</th>
<th>Dynamic Power (mw)</th>
<th>Static Power (mw)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Power Estimator</td>
<td>2279</td>
<td>2099</td>
<td>187.14</td>
</tr>
<tr>
<td>Smart Power</td>
<td>2470.830</td>
<td>2270.610</td>
<td>200.220</td>
</tr>
<tr>
<td>On Board</td>
<td>2595</td>
<td>2259</td>
<td>336</td>
</tr>
</tbody>
</table>
2.11 Conclusion

This tutorial demonstrates the low power capability of RTG4 FPGAs. PLL power-down signal can be used for switching between normal and standby mode. The smart power tool in Libero SoC and power estimator tool provide initial power values of the design, and the power values are aligned with the onboard power.