AN36 Handling Air Cavity Surface-mount LGA Package

Use of air cavity surface mount scalable Land Grid Array (LGA) package now constitutes a major portion of packaged high performance RF IC applications. The scalable LGA with exposed thermal paddle is a compact, reliable, and inexpensive package with excellent RF and thermal characteristics. However, due to the small size and tight assembly tolerance of this package, proper handling and assembly is required to optimize reliability and performance. In this document, LGA package will be referred to as "LGA package" or "LGA".

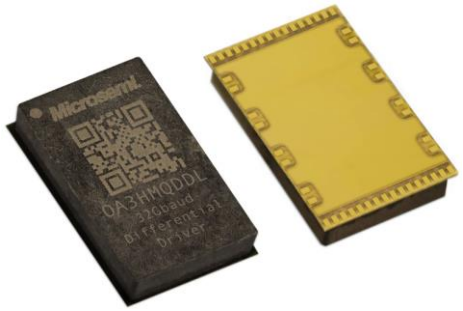


Figure 1. Typical LGA package[(a)] (left = top view, right = bottom view)

Handling Air Cavity LGA

Handle LGAs only in a clean, ESD-safe environment. Use an air ionizer, anti-static mats, conducing wrist straps, and relative humidity control. Tweezers or vacuum pick-up tools are suitable for handling; do not handle LGAs with bare hands, as this can contaminate the package lands and interfere with solder reflow. Do not manually handle or flex the LGA package. Too much pressure applied to the top and bottom of the LGA package surfaces may cause micro-cracks on the components inside the LGA package, which may lead to reliability issues. Figure 2 shows a cross section example of a typical air cavity LGA package along with its internal circuit components.

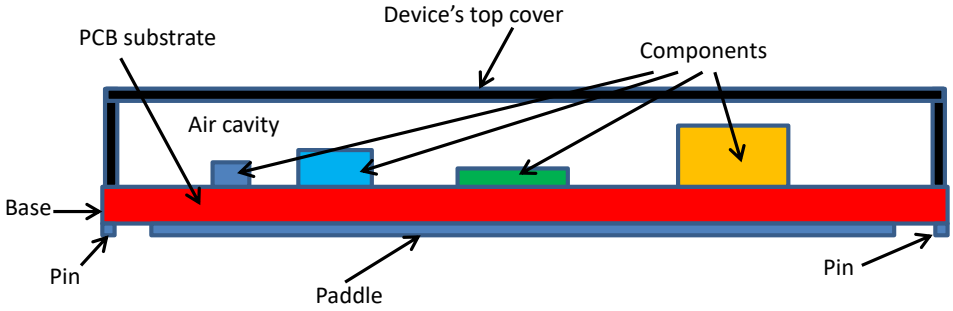


Figure 2. Cross section of a typical air cavity LGA package (bond wirings not shown)

Maintain LGAs in the original packaging until ready for use. Small, thin LGA packages are susceptible to moisture-related cracking during assembly if the parts are allowed to absorb an appreciable amount of moisture; maintain the parts in a low humidity environment if possible, refer to J-STD-0033C for recommended guideline. If the parts arrive packaged with desiccant packets, keep the packaging tight by folding or taping it to extend the effectiveness of the desiccant. Full evacuation is not recommended to reseal the moisture-barrier bag (MBB), as it will impede desiccant and humidity indicator card (HIC) performance and possibly lead to MBB puncture. Refer to product datasheet for the component's respective MSL. If cleaning the bottom of the LGA is needed (e.g., debris), contact factory for recommendation.

© 2017 Microsemi Corporation

Board Design[b]

LGA package with exposed paddle (EP) depends upon good thermal contact between the paddle and the PC board heatsink to maintain a safe operating temperature on the LGA device. The heatsink is integrated into the PC board as a top thermal pad and an array of thermal vias connecting to one or more ground planes, which act as heat spreaders. This is shown schematically in the side view illustration in Figure 3.

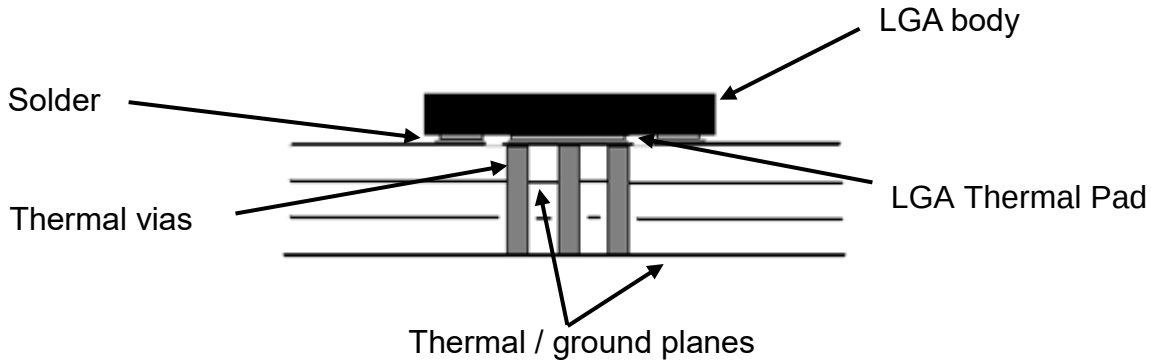


Figure 3. LGA Side View

The recommended package land layout is provided in the individual product datasheets. Use of small or filled vias under the thermal paddle prevents wicking of solder from under the part; open vias larger than .010" - .012" in diameter will wick solder away from the PC board thermal pad and should be avoided.

Solder Attach

The need for good solder attachment of the exposed thermal paddle adds some requirements to the solder paste / attach / reflow process[c,d]. Based on internal Microsemi investigation for acceptable thermal heat transfer on the paddle, it is recommended to have soldered area coverage of ≥ 50% under the thermal paddle; use a screen print that fills about 60-80% of the PC board land area. For larger LGA package sizes, solder dam on the paddle section is required; refer to their respective product datasheet and Microsemi application note, AN34[e], "QFN Paddle Landing Layout Pattern Recommendations" for more information. For acceptable electrical connection on the I/O solder pads (a.k.a. lands), there is a similar requirement; it is recommended to have a minimum soldered area coverage of ~60% on the I/O solder pad, per IPC-610 standard[f], "Acceptability of Electronic Assemblies".

Printed paste thickness can be adjusted to achieve complete solder filling of the thermal paddle area after reflow while avoiding excess solder or shorts in the I/O pad areas. The part should stand off of the PC board about .001" - .002" to provide strain relief from thermal mismatch-related stress while still providing a good heatsink for the thermal paddle.

Parts should be placed using automated placement equipment. Reflow is performed using a programmable convection heat ramp / soak. Manual reflow is not recommended due to the difficulty of controlling the temperature profile.

Microsemi LGAs are Pb-free and compatible with either Sn/Pb or Pb-free assembly techniques. After paste print and part placement, solder attach is achieved by ramping the part to pre-heat, thermal soak, solder reflow, and then cool as shown in figure 4. Use of a no-clean (NC) flux is required, as removal of all flux under the LGA is very difficult. Microsemi recommend uses of SAC305, type 3 or type 4 solder paste. The maximum peak reflow temperature should be ≤ 250°C. Please consult with

© 2017 Microsemi Corporation

the solder paste manufacturer for the optimum solder reflow profile to use for your PCB assembly. For more soldering info, please refer to IPC/JEDEC J-STD-020E[g].

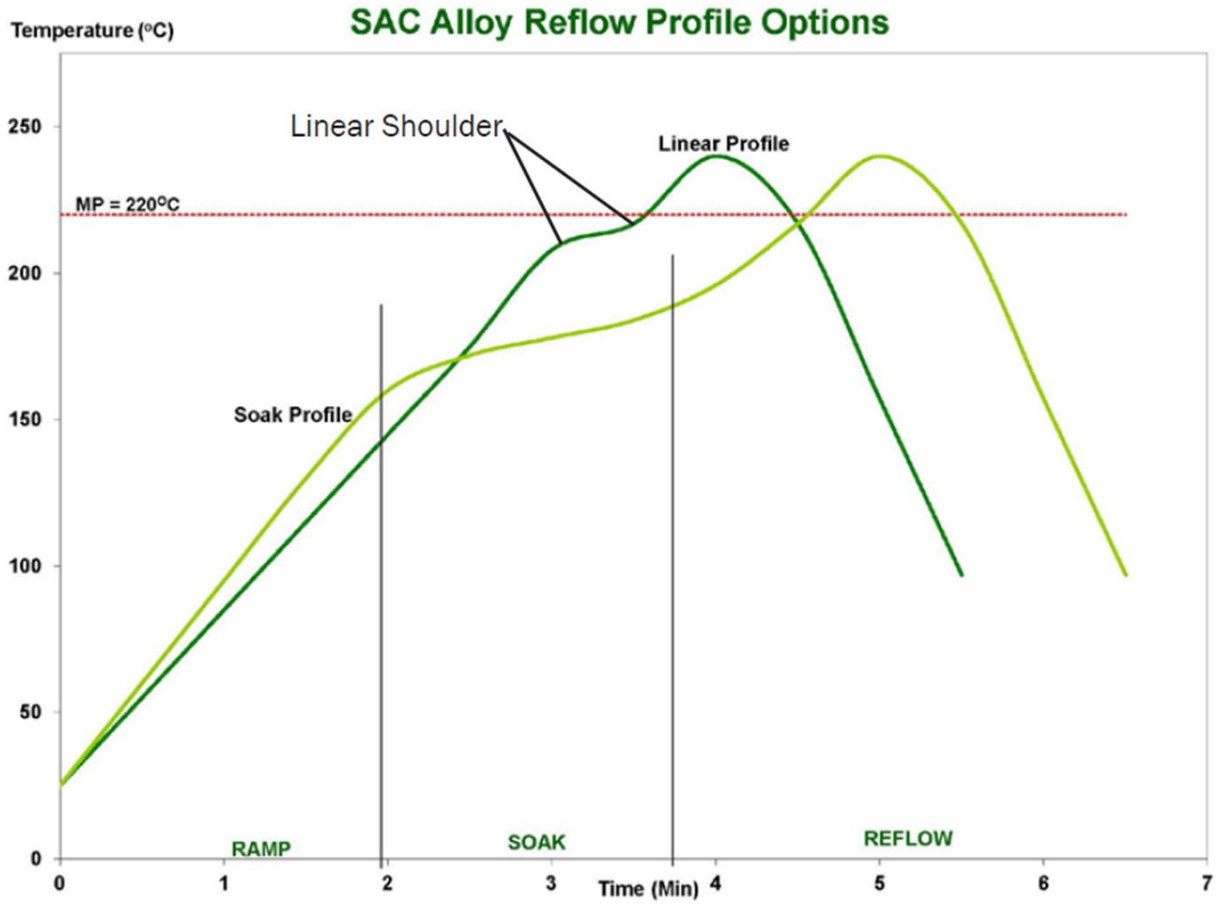


Figure 4. Typical solder reflow profile for SAC305 type of solder paste (courtesy of Indium Corp.)

Thermal Considerations

Electrical performance and reliability of the LGA are highly dependent upon the PC board heatsink design[h,i]. Efficient removal of heat from the exposed paddle is required to maintain the device below the absolute maximum operating temperature as specified in the product datasheet.

To estimate the device channel or junction temperature (T_J) a thermal model is constructed as shown in Figure 5.

© 2017 Microsemi Corporation

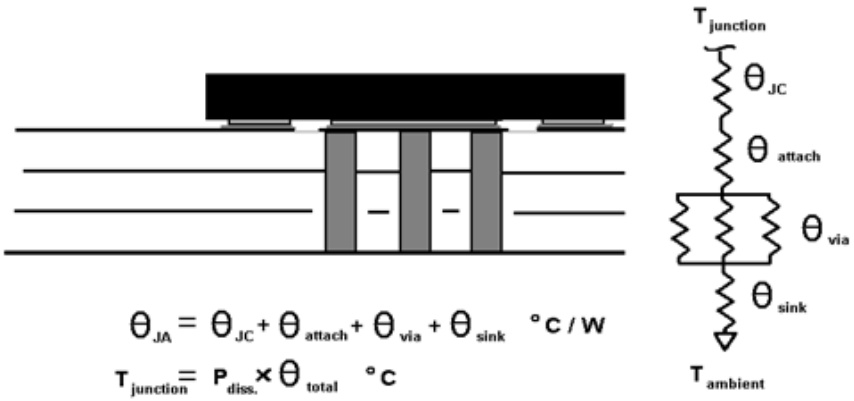


Figure 5. PC board heatsink thermal model

Each thermal resistance is estimated or calculated, and then combined together to calculate the total thermal resistance from the device junction to ambient: The device thermal resistance, Θ_{JC} is provided on the product datasheet. Θ_{attach} is calculated from the thermal conductivity, attach area, and thickness of the solder attach; Θ_{attach} = thickness / (cond. x area), (eq. 1).

Similarly, Θ_{via} is calculated using the thermal conductivity of the copper wall, the cross-sectional area and the height of one via. Combine the result for n vias in parallel by dividing the resulting thermal resistance for a single via by n.

Finally, the thermal resistance of the PC board to an additional heat sink, Θ_{sink}, is estimated. The total thermal resistance to ambient, Θ_{JA} is the series / parallel combination of each of the thermal resistances shown in *Figure 3*.

Typical values of Θ_{JA} range from ~ 20 - 30ºC / W, depending upon the IC size and material, the number and diameter of thermal vias, and the size, thickness and number of thermal ground planes in the PC board. Typical absolute maximum junction temperatures, T_j are 125-150ºC.

For example, a LGA may dissipate 1W to a PC board backside maintained at 85ºC and still readily meet the requirement to remain below 125ºC (85ºC + 30ºC/W x 1W = 115ºC).

Accurate knowledge of Θ_{JC} is especially important for LGA devices which dissipate 2 watts or more; for these devices, an ambient temperature of 60ºC at the board backside can easily lead to T_j ~ 125ºC or more. In these cases, careful consideration of the thermal environment is required, and an additional heatsink may be needed below the PC board to maintain a more stable ambient for higher power dissipation.

© 2017 Microsemi Corporation

Example, calculate the junction temperature of the device soldered onto a PCB:

Parameter	Description	Assumption	Calculation
Θ_{JC}	IC thermal resistance	30 ºC/W from datasheet	-
Θ_{attach}	Solder joint thermal resistance	Thermal conductivity (K) of SN63 = 50 W/m-ºK, area is 0.0094 x 0.01624 m, solder joint thickness (l) = 0.000051 m	Area = 0.0094 m x 0.01624 m = 0.000153 m^2, Θ_{attach} = length/(K*Area) = 0.0067 ºC/W
Θ_{via}	Vias hole thermal resistance	Thermal conductivity (K) of copper = 401 W/m-ºK, via outer radius = 0.000152 m, via inner radius = 0.000135 m, via length = 0.000254 m, 10 via's – copper filled	A = $\pi*(r_o^2-r_i^2)$ = $1.533x10^{-8}$ m^2 Θ_{via} = length/(K*Area) = 41.3 ºC/W (for each via), Since there are 10 via's in parallel, the equivalent resistance is $1/10^{th}$, or Θ_{via} = 4.13 ºC/W
$\Theta_{sink/PCB}$	Heatsink/PCB thermal resistance	Thermal conductivity (K) of Roger RO4350 = 0.69 W/m-ºK, area is 0.015 x 0.021 m, length (thickness) = 0.000254 m	Area = 0.015 m x 0.021 m = 0.000315 m^2, $\Theta_{sink/PCB}$ = length/(K*Area) = 1.169 ºC/W
Θtotal or Θ_{JA}	Sum of thermal resistance	Θtotal = Θ_{JC} + Θ_{attach} + Θ_{via} + $\Theta_{sink/PCB}$	Θtotal = 30 + 0.0067 + 4.13 + 1.169 = 35.3 ºC/W
Pdevice	Power dissipation of device	1 W (based on V and I)	-
Tambient	Operating ambient temperature	85 ºC	-
Tjunction or TJ	Calculated junction temperature at device	Tjunction = (Θtotal * Pdevice) + Tambient	Tjunction = (35.3 * 1) + 85 = 120.3 ºC

Board Rework

When removing a LGA device from the board, it is recommended that localized heating is used: apply heat at the same time to both top and bottom sides of the PCB. The maximum body temperature of any surface mount components on the board should not exceed 200 ºC, except for a component to be removed; (do not exceed 250 ºC on air cavity LGA device during the rework process). This method will minimize moisture related component damage. If any component temperature exceeds 200 ºC during rework, the board must be pre-baked dry prior to rework. For more information, refer to Microsemi's application note, AN35[j], "Basic De-soldering Process for QFN SMT Devices", and IPC/JEDEC J-STD-033C[k], "Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices".

It is recommended to use heat shield tape on top of the air cavity LGA package lid during the rework process, (do not cover up the device's solder pins and paddle). This will help prevent heat from damaging the sensitive components inside the LGA package and its package lid during the de-soldering process. Figure 6 shows an example of heat shield tape.

© 2017 Microsemi Corporation

Figure 6. Example of heat shield tape

References:

[a] JEDEC Publication 95, Design Guide 4.25, Design Requirements for Outlines of Solid State and Related Products – Fine-pitch, Land Grid Array Package, Square and Rectangular

[b] "Surface Mount Requirements for Land Grid Array Package", Amkor Technology, Inc., Sept. 2002

[c] "Application Notes for Surface Mount Assembly of Amkor's Thermally / Electrically Enhanced Leadframe Based Packages", Amkor Technology, December, 2001

[d] "Board Level Assembly and Reliability Considerations for QFN Type Packages", Amkor Technology

[e] Application Note: "AN34, QFN Paddle Landing Layout Pattern Recommendations", Microsemi

[f] IPC-A-610: Acceptability of Electronic Assemblies

[g] IPC/JEDEC J-STD-020E: Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices

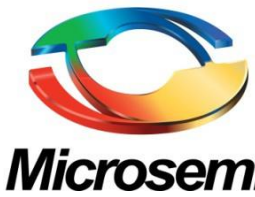
[h] JESD51-3: Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

[i] JESD51-7: High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages

[j] Application Note: "AN35, Basic De-soldering Process for QFN SMT Devices", Microsemi

[k] IPC/JEDEC J-STD-0033C: Handling, Packing, Shipping and Use of Moisture/Reflow Sensitive Surface Mount Devices, February 2012

© 2017 Microsemi Corporation



Microsemi Corporate Headquarters
One Enterprise, Aliso
Viejo, CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail:
sales.support@microsemi.com

© 2017 Microsemi Corporation. All rights reserved. Microsemi and the Microsemi logo are trademarks of Microsemi Corporation. All other trademarks and service marks are the property of their respective owners.

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.

Microsemi makes no warranty, representation, or guarantee regarding the information contained herein or the suitability of its products and services for any particular purpose, nor does Microsemi assume any liability whatsoever arising out of the application or use of any product or circuit. The products sold hereunder and any other products sold by Microsemi have been subject to limited testing and should not be used in conjunction with mission-critical equipment or applications. Any performance specifications are believed to be reliable but are not verified, and Buyer must conduct and complete all performance and other testing of the products, alone and together with, or installed in, any end-products. Buyer shall not rely on any data and performance specifications or parameters provided by Microsemi. It is the Buyer's responsibility to independently determine suitability of any products and to test and verify the same. The information provided by Microsemi hereunder is provided "as is, where is" and with all faults, and the entire risk associated with such information is entirely with the Buyer. Microsemi does not grant, explicitly or implicitly, to any party any patent rights, licenses, or any other IP rights, whether with regard to such information itself or anything described by such information. Information provided in this document is proprietary to Microsemi, and Microsemi reserves the right to make any changes to the information in this document or to any products and services at any time without notice.